Method and Apparatus for a Semiconductor Device with a High-k Gate Dielectric

ABSTRACT OF THE DISCLOSURE

A process and apparatus for a high gate dielectric MOS transistor is described. A substrate is provided, a high-k gate dielectric material is deposited over the substrate, a gate electrode layer is deposited over the dielectric material and a patterning step is performed creating sidewalls of the electrode and dielectric and removing a portion of the substrate. Sidewall material is deposited over the patterned gate electrode and dielectric creating protective sidewalls on the patterned gate electrode and dielectric that extends beneath the bottom of the dielectric. In alternative embodiments a channel material is deposited beneath the high-k gate dielectric and the patterning step removes at least a portion of the channel material beneath the high-k gate dielectric. In alternative embodiments the channel material is counter-doped.

(FIG . 7)