STRAINED CHANNEL FIELD EFFECT TRANSISTOR
USING SACRIFICIAL SPACER

ABSTRACT

A field effect transistor (FET) (10) is provided which includes a gate stack (29), a pair of first spacers (32) disposed over sidewalls of the gate stack (29) and a pair of semiconductor alloy regions (39) disposed on opposite sides of and spaced a first distance from the gate stack (29). Source and drain regions (24) of the FET (10) are at least partly disposed in the semiconductor alloy regions (39); and spaced a second distance from the gate stack (29) by a corresponding spacer of the pair of first spacers (32), which may be different from the first distance. The FET (10) may also include second spacers (34) disposed on the first spacers (32), and silicide regions (40) at least partly overlying the semiconductor alloy regions (39), wherein the silicide regions (40) are spaced from the gate stack (29) by the first and second spacers (32, 34).

Fig. 1.