CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:

forming at least one strained first fin in a layer of strained semiconductor material overlying an insulating layer on a base substrate, the at least one strained first fin having a first length below a critical length Lc below which the strained semiconductor material of the at least strained first fin relaxes upon subsequently conducting a heat treatment between 950°C and 1250°C;

after forming the at least one strained first fin, conducting the heat treatment between 950°C and 1250°C, the heat treatment causing relaxation of stress within the at least one strained first fin so as to form at least one relaxed first fin; and

forming at least one strained second fin in the layer of strained semiconductor material;

wherein the at least one strained second fin has a second length above the critical length Lc such that the at least one strained second fin does not relax while conducting the heat treatment at the temperature or temperatures between 950°C and 1250°C, or the at least one strained second fin is formed after conducting the heat treatment.

2. The method of claim 1, wherein the at least one relaxed first fin has a first lattice constant, and the at least one second strained fin has a second lattice constant different from the first lattice constant, and wherein the method further comprises:

forming an n-type field effect transistor comprising one fin selected from the at least one relaxed first fin and the at least one strained second fin, the one fin having the highest lattice constant among the first lattice constant and the second lattice constant; and

forming a p-type field effect transistor comprising another fin selected from the at least one relaxed first fin and the at least one strained second fin, the another fin having the lowest lattice constant among the first lattice constant and the second lattice constant.

3. The method of claim 2, wherein the layer of strained semiconductor material is in a state of tensile stress prior to forming the at least one strained first fin in the layer of strained

semiconductor material and prior to forming the at least one strained second fin in the layer of strained semiconductor material.

4. The method of claim 3, wherein the layer of strained semiconductor material comprises a tensile strained silicon layer prior to forming the at least one strained first fin in the layer of strained semiconductor material and prior to forming the at least one strained second fin in the layer of strained semiconductor material.

5. The method of any one of claims 1 through 4, further comprising forming the at least one strained second fin to have a length of at least 1 μm, and forming the at least one strained first fin to have a length less than 1 μm.

6. The method of claim 4, wherein conducting the heat treatment comprises performing the heat treatment in an inert atmosphere for a time of between 5 minutes and 10 hours.

7. The method of any one of claims 2 through 4, further comprising the following actions performed after conducting the heat treatment and prior to forming the p-type field effect transistor comprising the another of the at least one relaxed first fin and the at least one strained second fin:

depositing an epitaxial silicon germanium alloy on the another of the at least one relaxed first fin and the at least one strained second fin;

performing an oxidation condensation process to introduce germanium atoms into the another of the at least one relaxed first fin and the at least one strained second fin and to form a silicon oxide layer over a surface of the another of the at least one relaxed first fin and the at least one strained second fin; and

removing the silicon oxide layer.

8. The method of claim 7, further comprising masking the one of the at least one relaxed first fin and the at least one strained second fin before depositing the epitaxial silicon germanium alloy over the another of the at least one relaxed first fin and the at least one strained second fin.

9. The method of claim 1, wherein the layer of strained semiconductor material is in a state of compressive stress prior to forming the at least one strained first fin in the layer of strained semiconductor material and prior to forming the at least one strained second fin in the layer of strained semiconductor material.

10. The method of claim 9, wherein the layer of strained semiconductor material comprises a compressively strained silicon-germanium layer prior to forming the at least one strained first fin in the layer of strained semiconductor material and prior to forming the at least one strained second fin in the layer of strained semiconductor material.

11. The method of claim 9, further comprising forming the at least one strained second fin to have a length of at least 1 μm, and forming the at least one relaxed first fin to have a length less than 1 μm.

12. The method of any one of claims 9 through 11, wherein conducting the heat treatment comprises performing the heat treatment in an inert atmosphere for a time of between 10 hours and 1 minute.

13. The method of claim 1, wherein conducting the heat treatment further comprises increasing a density of the insulating layer.

14. The method of claim 13, wherein the at least one relaxed first fin has a first lattice constant after conducting the heat treatment, and the at least one strained second fin has a second lattice constant different from the first lattice constant, the method further comprising:

forming an n-type field effect transistor comprising one fin selected from the at least one relaxed first fin and the at least one strained second fin, the one fin having the highest lattice constant among the first lattice constant and the second lattice constant; and

forming a p-type field effect transistor comprising another fin selected from the at least one relaxed first fin and the at least one strained second fin, the another fin having the lowest lattice constant.

15. The method of claim 14, wherein the layer of strained semiconductor material comprises a tensile strained silicon layer, the method further comprising the following actions performed after conducting the heat treatment and prior to forming the p-type field effect transistor comprising the another of the at least one relaxed first fin and the at least one strained second fin:

depositing an epitaxial silicon germanium alloy on the another of the at least one relaxed first fin and the at least one strained second fin;

performing an oxidation condensation process to introduce germanium atoms into the another of the at least one relaxed first fin and the at least one strained second fin and form a silicon oxide layer over a surface of the another of the at least one relaxed first fin and the at least one strained second fin; and

removing the silicon oxide layer.

16. The method of claim 15, wherein depositing the epitaxial silicon germanium alloy on the another of the at least one relaxed first fin and the at least one strained second fin comprises depositing the epitaxial silicon germanium alloy on the at least one relaxed first fin, and wherein the method further comprises masking the at least one strained second fin before depositing the epitaxial silicon germanium alloy on the at least one relaxed first fin.

17. The method of claim 1, further comprising implanting ions into the insulating layer prior to forming the at least one strained first fin and reducing a viscosity of the insulating layer using the implanted ions.

18. The method of claim 17, wherein the at least one relaxed first fin has a first lattice constant after conducting the heat treatment, and the at least one strained second fin has a second lattice constant different from the first lattice constant, the method further comprising:

forming an n-type field effect transistor comprising one fin selected from the at least one relaxed first fin and the at least one strained second fin, the one fin having the highest lattice constant among the first lattice constant and the second lattice constant; and

forming a p-type field effect transistor comprising another fin selected from the at least one relaxed first fin and the at least one strained second fin, the another fin having the lowest lattice constant among the first lattice constant and the second lattice constant.

19. The method of claim 18, wherein the layer of strained semiconductor material comprises a tensile strained silicon layer, the method further comprising the following actions performed after conducting the heat treatment and prior to forming the p-type field effect transistor comprising the another of the at least one relaxed first fin and the at least one strained second fin:

depositing an epitaxial silicon germanium alloy on the another of the at least one relaxed first fin and the at least one strained second fin;

performing an oxidation condensation process to introduce germanium atoms into the another of the at least one relaxed first fin and the at least one strained second fin and form a silicon oxide layer over a surface of the another of the at least one relaxed first fin and the at least one strained second fin; and

removing the silicon oxide layer.

20. The method of claim 19, further comprising masking the one fin of the at least one relaxed first fin and the at least one strained second fin before depositing the epitaxial silicon germanium alloy on the another fin of the at least one relaxed first fin and the at least one strained second fin.

21. A method of fabricating a semiconductor device, comprising:

forming at least one strained first fin in a layer of strained semiconductor material overlying an insulating layer on a base substrate, the at least one strained first fin having a first length less than 1 μm and below a critical length Lc below which the strained semiconductor material of the at least strained first fin relaxes upon subsequently conducting a heat treatment;

after forming the at least one strained first fin, conducting the heat treatment between 950°C and 1250°C in an inert atmosphere for a time of between 5 minutes and 10 hours, the heat treatment causing relaxation of stress within the at least one strained first fin so as to form at least one relaxed first fin; and

forming at least one strained second fin having a second length of at least 1 μm in the layer of strained semiconductor material;

wherein the second length of the at least one strained second fin is above the critical length Lc such that the at least one strained second fin does not relax while conducting the heat treatment between 950°C and 1250°C, or the at least one strained second fin is formed after conducting the heat treatment.