regions lying below the carrier plate. In order to improve the polishing agent distribution, US 2006-178089 A discloses a carrier plate having a multiplicity of round openings through which the polishing agent reaches the lower polishing pad.

The teaching of EP 1 676 672 A1 includes improving the supply of polishing agent to the lower polishing plate by at least 15% of the area of the carrier plate being occupied by holes that provide for the polishing agent a passage to the lower polishing plate.

However, these additional "polishing agent cutout" in the circular carrier plates reduce the area moment of inertia thereof and, as a consequence thereof, also the resistance thereof to torsion. That is disadvantageous since the risk of carrier plate warping is thereby increased. The warping of the carrier plate can lead to pad damage, reduced pad lifetime, particle generation, polishing scratches through to wafer fracture and damage to the installation.

On account of the further increasing surface area in semiconductor wafers of future generations, for example having a diameter of 450 mm, the uniform polishing agent distribution (application of polishing agent) can be realized only to a limited extent during the polishing process in accordance with the prior art.

The objective of the present invention emerges from this problem area. Embodiments~~The aim~~ of the invention seek~~is~~ to ensure the uniform application of polishing agent to the polishing pad surfaces during the simultaneous double-side polishing of semiconductor wafers, without impairing the stability of the carrier plate.
According to an aspect of the present invention, there is provided~~The object of the invention is achieved by means of~~ a method for the simultaneous double-side polishing of at least one wafer composed of semiconductor material which is situated in a

suitably dimensioned cutout in a carrier plate and which has a front side and a rear side, and the double-side polishing is effected between an upper polishing plate covered with a first polishing pad and a lower polishing plate covered with a second polishing pad, with a polishing agent being supplied, wherein the surfaces of the first (upper) and of the second (lower) polishing pad are in each case interrupted by at least one channel-shaped depression running spirally from the center to the edge, wherein the polishing pad surface has three spiral channel-shaped depressions arranged circularly around the midpoint of the polishing pad in the polishing pad surface, the distance W between whose turns becomes continuously greater from the inner portion toward the outer portion, and each of the three spiral channel-shaped depressions merges into a circular form enclosing the three spirals in the edge region of the polishing pad, without there being a connection between the three circular channels, and the outer edge region is formed by the ring-shaped area in the outer third of the polishing pad surface.

The method according to the invention and preferred embodiments will be described and explained in detail, by means of figures 1 to 2.

Figure 1 shows spiral forms used in the method according to the invention: (a) logarithmic spiral, (b) Archimedes' spiral, (c) Fermat's spiral, (d) triple spiral.

Figure 2 shows a preferred embodiment of the carrier plate (1) modified according to the invention with the segmented polishing agent passages (2) interrupted by the three webs (4), and the suitably dimensioned cutouts (3) for the wafers (5) composed of semiconductor material, wherein the cutouts (3) for the wafers (5) composed of semiconductor material are surrounded by the segmented polishing agent passages (2) at a distance A. In this preferred embodiment, the webs (4) are arranged such that the respective centers of the three webs (4) are at an angle of 120° with respect to one another.

The process according to the invention includes not just a partial aspect restricted to a specific technical component or an individual process-technological aspect (e.g. of individual process parameters), but encompasses associated process features. These process features are subdivided into

Patent Claims:

1. A method for the simultaneous double-side polishing of at least one wafer (5) composed of semiconductor material which is situated in a suitably dimensioned cutout (3) in a carrier plate (1) and which has a front side and a rear side, and the double-side polishing is effected between an upper polishing plate covered with a first polishing pad and a lower polishing plate covered with a second polishing pad, with a polishing agent being supplied, wherein the surfaces of the first (upper) and of the second (lower) polishing pad are in each case interrupted by at least one channel-shaped depression running spirally from the center to the edge.

2. The method as claimed in claim 1, wherein the at least one channel-shaped depression running spirally in the polishing pad surface has at least three turns.

3. The method as claimed in either of claims 1 and 2, wherein the distance W between the turns of the at least one channel-shaped depression running spirally in the polishing pad surface is constant from the inner portion toward the outer portion.

4. The method as claimed in either of claims 1 and 2, wherein the distance W between the turns of the at least one channel-shaped depression running spirally in the polishing pad surface becomes continuously greater from the inner portion toward the outer portion.

5. The method as claimed in either of claims 1 and 2, wherein the distance W between the turns of the at least one channel-shaped depression running spirally in the polishing pad surface becomes continuously smaller from the inner portion toward the outer portion.

6. The method as claimed in either of claims 1 and 2, wherein the polishing pad surface has three spiral channel-shaped depressions arranged circularly around the midpoint of the polishing pad in the polishing pad surface, the distance W between whose turns becomes continuously greater from the inner portion toward the outer portion, and each of the three spiral channel-shaped depressions merges into a circular form enclosing the three spirals in the edge region of the polishing pad, without there being a connection between the three circular channels, and the outer edge region is formed by the ring-shaped area in the outer third of the polishing pad surface.

7. The method as claimed in any of claims 1 to 6, wherein the width of the at least one channel-shaped depression running spirally in the polishing pad surface becomes continuously greater from the inner portion toward the outer portion.

8. The method as claimed in any of claims 1 to 7, wherein the depth of the at least one channel-shaped depression running spirally in the polishing pad surface becomes continuously greater from the inner portion toward the outer portion.

9. The method as claimed in any of claims 1 to 8, wherein at least one suitably dimensioned circular cutout (3) in the carrier plate (1) is surrounded by three segmented cutouts (2) which have an identical size (relative to the area) and are separated from one another by the webs (4), with a distance among one another of in each case at most 110°, in a ring-shaped manner at a distance A from the circular cutout (3).

10. The method as claimed in any of claims 1 to 9, wherein an inherent rotation of the semiconductor wafer (5) within the

suitably dimensioned cutout (3) in the carrier plate (1) is possible.

11. The method as claimed in any of claims 1 to 9, wherein an inherent rotation of the semiconductor wafer (5) within the suitably dimensioned cutout (3) in the carrier plate (1) is prevented by the semiconductor wafer being fixed in the cutout (3).

12. The method as claimed in any of claims 1 to 11, wherein the polishing agent supply is effected on the front side and the rear side of the semiconductor wafer (5) in a pressurized manner through openings present both in the upper and in the lower polishing plate and also in the upper and in the lower polishing pad, and wherein nozzles for the polishing agent supply can be integrated in the openings in the polishing plate.

13. The method as claimed in claim 12, wherein the orientation of the openings of the nozzles integrated in the polishing plate for the polishing agent supply or the openings in the polishing plate and/or in the polishing pad, relative to the polishing pad surface, lies in an angular range of from 45° to less than or equal to 90°.

14. The method as claimed in claim 13, wherein the quantity of the polishing agent emerging from the openings into the working gap per unit time in an inner circular region of the polishing pad is higher than the quantity that emerges in the same time from the openings situated in the outer ring-shaped region.

15. The method as claimed in any of claims 1 to 14, wherein the front side of the at least one wafer (5) composed of

semiconductor material is polished at the upper polishing pad.

PATENT CLAIMS

1. A method for the simultaneous double-side polishing of one or more wafer composed of semiconductor material which is situated in a cutout in a carrier plate and which has a front side and a rear side, and the double-side polishing is effected between an upper polishing plate covered with a first polishing pad and a lower polishing plate covered with a second polishing pad, with a polishing agent being supplied, wherein the surfaces of the first (upper) and of the second (lower) polishing pad are in each case interrupted by one or more channel-shaped depression running spirally from the center to the edge,
wherein the polishing pad surface has three spiral channel-shaped depressions arranged circularly around the midpoint of the polishing pad in the polishing pad surface, the distance W between whose turns becomes continuously greater from the inner portion toward the outer portion, and each of the three spiral channel-shaped depressions merges into a circular form enclosing the three spirals in the edge region of the polishing pad, without there being a connection between the three circular channels, and the outer edge region is formed by the ring-shaped area in the outer third of the polishing pad surface.

2. The method as claimed in claim 1, wherein the one or more channel-shaped depression running spirally in the polishing pad surface has three or more turns.

3. The method as claimed in either of claims 1 and 2, wherein the width of the one or more channel-shaped depression running spirally in the polishing pad surface becomes continuously greater from the inner portion toward the outer portion.

4. The method as claimed in either of claims 1 and 2, wherein the depth of the one or more channel-shaped depression running spirally in the polishing pad surface becomes continuously greater from the inner portion toward the outer portion.

5. The method as claimed in either of claims 1 and 2, wherein one or more circular cutout in the carrier plate is surrounded by three segmented cutouts which have an identical size (relative to the area) and are separated from one another by the webs, with a distance among one another of in each case at most 110°, in a ring-shaped manner at a distance A from the circular cutout.

6. The method as claimed in either of claims 1 and 2, wherein an inherent rotation of the semiconductor wafer within the cutout in the carrier plate is possible.

7. The method as claimed in either of claims 1 and 2, wherein an inherent rotation of the semiconductor wafer within the cutout in the carrier plate is prevented by the semiconductor wafer being fixed in the cutout.

8. The method as claimed in either of claims 1 and 2, wherein the polishing agent supply is effected on the front side and the rear side of the semiconductor wafer in a pressurized manner through openings present both in the upper and in the lower polishing plate and also in the upper and in the lower polishing pad, and wherein nozzles for the polishing agent supply can be integrated in the openings in the polishing plate.

9. The method as claimed in claim 8, wherein the orientation of the openings of the nozzles integrated in the polishing plate for the polishing agent supply or the openings in either or both of the polishing plate and the polishing pad, relative to the polishing pad surface, lies in an angular range of from 45° to less than or equal to 90°.

10. The method as claimed in claim 9, wherein the quantity of the polishing agent emerging from the openings into the working gap per unit time in an inner circular region of the polishing pad is higher than the quantity that emerges in the same time from the openings situated in the outer ring-shaped region.

11. The method as claimed in either of claims 1 and 2, wherein the front side of the one or more wafer composed of semiconductor material is polished at the upper polishing pad.