

SUBSTRATE FOR INTEGRATED CIRCUIT DEVICES INCLUDING MULTI-LAYER GLASS CORE AND METHODS OF MAKING THE SAME

FIELD OF THE INVENTION

The disclosed embodiments relate generally to substrates for integrated circuit
5 devices, and more particularly to a substrate having a multi-layer glass core.

BACKGROUND OF THE INVENTION

An integrated circuit (IC) die may be disposed in a package to support the die, as well as to aid in forming electrical connections between the die and a next-level component, such as a motherboard, mainboard, or other circuit board. The package
10 typically includes a substrate to which the die is both mechanically and electrically coupled. For example, the IC die may be coupled to the substrate by an array of interconnects in a flip-chip arrangement, with a layer of underfill disposed around the interconnects and between the die and substrate. Each of the interconnects may comprise a terminal on the die (e.g., a bond pad, a copper pillar or stud bump, etc.) that is
15 electrically coupled (e.g., by reflowed solder) to a mating terminal (e.g., a pad, pillar, stud bump, etc.) on the substrate. Alternatively, by way of further example, the IC die may be attached to the substrate by a layer of die attach adhesive, and a plurality of wire bonds may be formed between the die and substrate.

The IC die is disposed on one side of the substrate, and a number of electrically
20 conductive terminals are formed on an opposing side of the substrate. The terminals on the opposing side of the substrate will be used to form electrical connections with the next-level component (e.g., a circuit board), and these electrical connections can be used to deliver power to the die and to transmit input/output (I/O) signals to and from the die. The electrically conductive terminals on the substrate's opposing side may comprise an array
25 pins, pads, lands, columns, bumps etc., and these terminals may be electrically coupled to a corresponding array of terminals on the circuit board or other next-level component. The terminals on the package substrate's opposing side may be coupled to the next-level board using, for example, a socket (and retention mechanism) or by a solder reflow process.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a schematic diagram showing a plan view of one embodiment of a substrate having a multi-layer glass core.

FIG. 1B is a schematic diagram showing a cross-sectional elevation view of the substrate having a multi-layer glass core shown in FIG. 1A, as taken along line B-B of FIG. 1A.

FIG. 1C is a schematic diagram showing a portion of the cross-sectional elevation
5 view of FIG. 1B and illustrating another embodiment of the substrate having a multi-layer glass core.

FIG. 1D is a schematic diagram showing a portion of the cross-sectional elevation view of FIG. 1B and illustrating a further embodiment of the substrate having a multi-layer glass core.

10 FIG. 1E is a schematic diagram showing a portion of the cross-sectional elevation view of FIG. 1B and illustrating yet another embodiment of a substrate having a multi-layer glass core.

FIG. 1F is a schematic diagram showing a portion of the cross-sectional elevation view of FIG. 1B and illustrating yet a further embodiment of a substrate having a multi-
15 layer glass core.

FIG. 1G is a schematic diagram showing a portion of the cross-sectional elevation view of FIG. 1B and illustrating another alternative embodiment of a substrate having a multi-layer glass core.

FIG. 2 is a schematic diagram showing a cross-sectional elevation view of an
20 integrated circuit assembly including an embodiment of a substrate having a multi-layer glass core.

FIG. 3 is a block diagram illustrating embodiments of a method of forming a substrate having a multi-layer glass core.

FIGS. 4A-4C are schematic diagrams illustrating embodiments of the method of
25 FIG. 3.

FIG. 5 is a block diagram illustrating an embodiment of a method of forming a multi-layer glass core.

FIGS. 6A-6C are schematic diagrams illustrating embodiments of the method of FIG. 5.

30 FIG. 7 is a block diagram illustrating another embodiment of a method of forming a multi-layer glass core.

FIGS. 8A-8J are schematic diagrams illustrating embodiments of the method of FIG. 7.

FIG. 9 is a block diagram illustrating a further embodiment of a method of forming a multi-layer glass core.

FIGS. 10A-10H are schematic diagrams illustrating embodiments of the method of FIG. 9.

5 FIG. 11 is a block diagram illustrating yet another embodiment of a method of forming a multi-layer glass core.

FIGS. 12A-12E are schematic diagrams illustrating embodiments of the method of FIG. 11.

10 FIG. 13 is a block diagram illustrating embodiments of a method of disposing conductive material in thru-holes of a multi-layer glass core.

FIGS. 14A-14C are schematic diagrams illustrating embodiments of the method of FIG. 13.

FIG. 15 is a schematic diagram illustrating an embodiment of a method of making a multi-layer glass plate.

15 FIGS. 16A-16E are schematic diagrams illustrating another embodiment of a method of making a multi-layer glass plate.

DETAILED DESCRIPTION OF THE INVENTION

Disclosed are embodiments of a substrate having a multi-layer glass core. One or more build-up layers may be disposed on each side of the multi-layer glass core, and
20 electrical conductors extend through the core. The multi-layer glass core may comprise a number of discrete glass layers bonded together. The glass layers may be bonded together by adhesive layers, and the adhesive layers may comprise an organic material.

Embodiments of methods of forming a substrate including a multi-layer glass core and having conductors extending through the core's thickness, as well as embodiments of
25 methods of forming a multi-layer glass core, are described below. Also disclosed are embodiments of an assembly including an integrated circuit die disposed on a substrate with a multi-layer glass core and coupled with the substrate by a set of interconnects.

As noted above, the disclosed embodiments encompass a substrate having a core comprised of multiple layers of glass. According to one embodiment, the term "glass"
30 refers to an amorphous solid. Examples of glass materials that may be used with the described embodiments include pure silica (e.g., approximately 100% SiO₂), soda-lime glass, boro-silicate glass, and alumo-silicate glass. However, the disclosed embodiments are not limited to silica-based glass compositions, and glasses having alternative base

materials (e.g., fluoride glasses, phosphate glasses, chalcogen glasses, etc.) may also be employed with the disclosed embodiments. Further, any combination of other materials and additives may be combined with silica (or other base material) to form a glass having desired physical properties. Examples of these additives include not only the

5 aforementioned calcium carbonate (e.g., lime) and sodium carbonate (e.g., soda), but also magnesium, calcium, manganese, aluminum, lead, boron, iron, chromium, potassium, sulfur, and antimony, as well as carbonates and/or oxides of these and other elements. The aforementioned glasses and additives are but a few examples of the many types of materials and material combinations that may find application with the disclosed
10 embodiments. In addition, a glass layer or structure may include surface treatments and/or coatings to improve strength and/or durability, and a glass layer or structure may also be annealed to lower internal stresses.

Generally, as used herein, the term “glass” does not refer to organic polymer materials, which may be amorphous in solid form. However, it should be understood that
15 a glass according to some embodiments may include carbon as one of the material’s constituents. For example, soda-lime glass, as well as numerous variations of this glass type, comprise carbon.

A glass, once formed into a solid body, is capable of being softened and perhaps remelted into a liquid form. The “glass transition temperature” of a glass material is a
20 temperature below which the physical properties of the glass are similar to those of a solid and above which the glass material behaves like a liquid. If a glass is sufficiently below the glass transition temperature, molecules of the glass may have little relative mobility. As a glass approaches the glass transition temperature, the glass may begin to soften and with increasing temperature the glass will ultimately melt into the liquid state. Thus, a
25 glass body may be softened to an extent sufficient to enable manipulation of the body’s shape, allowing for the formation of holes or other features in the glass body.

According to one embodiment, the “softening temperature” of a glass is temperature at which the glass has softened to an extent sufficient to enable the disclosed embodiments to be performed. For example, in one embodiment, the softening
30 temperature of a glass is the temperature at which the glass is sufficiently soft to allow for formation of holes (or vias) or other features in the glass. The glass transition and softening temperatures are unique properties of a glass, although two or more different glass materials may have similar glass transition and/or softening temperatures. Further, it

should be understood that the glass transition temperature and softening temperature of a particular glass may not necessarily be the same value.

Turning now to FIGS. 1A and 1B, illustrated are embodiments of a substrate 100 having a core 150 comprised of two or more layers of glass. A plan view of the substrate 100 is shown in FIG. 1A, whereas a cross-sectional elevation view of the substrate is shown in FIG. 1B, as taken along line B-B of FIG. 1A. Also, various alternative embodiments of the substrate 100 having a multi-layer glass core are shown in each of FIGS. 1C through 1G, and each of FIGS. 1C through 1G shows a portion of the substrate 100, identified generally by reference numeral 5 in FIG. 1B, in an enlarged view.

With reference to FIGS. 1A and 1B, the substrate 100 includes a core 150 comprised of a number of glass layers 157a, 157b, and 157c. In one embodiment, the core 150 further includes bonding layers 158a and 158b disposed between the glass layers 157a, 157b, 157c (e.g., layer 158a is disposed between glass layers 157a, 157b, and so on). Substrate 100 includes a first side 102 and an opposing second side 104 generally parallel with the first side 102. A periphery 108 of substrate 100 extends between the first and second sides 102, 104. According to some embodiments, the periphery 108 of the substrate 100 is generally rectangular, and in one embodiment all four sides of the periphery 108 are substantially equal such that the periphery forms a square. However, it should be noted that a substrate having a non-rectangular periphery is within the scope of the disclosed embodiments. In one embodiment, the substrate 100 has a thickness of between 0.2 mm and 1.1 mm.

The multi-layer glass core 150 has a first surface 152 and an opposing second surface 154. In one embodiment, the first and second surfaces 152, 154 are generally parallel to each other. A periphery 158 of the glass core 150 extends between the first and second surfaces 152, 154, and in some embodiments the glass core's periphery 158 generally corresponds to the substrate's periphery 108. According to one embodiment, the multi-layer glass core 150 may have a thickness between 50 micrometers and 800 micrometers. The individual glass layers 157a, 157b, 157c may comprise any suitable type of glass. In one embodiment, the glass layers 157a-c comprise the same glass material; however, in other embodiments any one of the glass layers 157a-c may comprise a glass material that is different than the glass material of any of the other glass layers.

A number of conductors 160 extend through the multi-layer glass core 150. Each conductor 160 is disposed in a hole or via 165, and each conductor 160 may extend from

the first surface 152 to the second surface 154. In other embodiments, however, one or more of the conductors extends only partially through the core's thickness. According to one embodiment, a conductor 160 comprises a hole or via 165 formed through the core 150 that has been filled with an electrically conductive material.

5 Conductors 160 may comprise any suitable electrically conductive material, including metals, composite materials, and electrically conductive polymers. Suitable metals include copper, tin, silver, gold, nickel, aluminum, and tungsten, as well as alloys of these and/or other metals. Processes that may be utilized to form a hole or via 165 include, for example, etching, laser drilling, imprinting, and sand blasting. Electrically
10 conductive material may be deposited in the holes or vias 165 to form conductors 160 by any suitable process, such as, for example, plating techniques (electroplating or electroless plating), chemical vapor deposition (CVD), physical vapor deposition (PVD), or screen printing techniques, as well as any combination of these and/or other processes. Various embodiments of the formation of holes 165 and the formation of conductors 160 are
15 described in greater detail below.

 Disposed on the first side 102 of substrate 100 is a first set of electrically conductive terminals 120 (see FIG. 1A). According to one embodiment, the first set of terminals 120 is arranged in a pattern to mate with a corresponding array of terminals disposed on an integrated circuit (IC) die. An IC die is not shown in FIGS. 1A-1B;
20 however, a die region 110 is depicted in FIG. 1A and the terminals 120 lie within this die region (sometimes referred to as a die shadow region). The terminals 120 may each comprise any suitable type of structure capable of forming an electrical connection with a terminal of the IC die. For example, a terminal 120 may comprise a pad, pillar, or stud bump formed from any suitable metal or combination of metals (e.g., aluminum, copper,
25 nickel, etc.), and a solder bump may be disposed on each terminal 120 (and/or on the terminals of the IC die). In one embodiment, an IC die may be disposed on the substrate 100 in a flip-chip manner, and the terminals on the die coupled with the terminals 120 on the substrate 100 by a solder reflow process. According to another embodiment, an IC die may be coupled to the substrate 100 by a layer of adhesive, and terminals on the die
30 electrically coupled to corresponding terminals on the substrate by a wirebond process (in this embodiment, the terminals 120 would lie outside the die region 110).

 Disposed on the second side 104 of substrate 100 is a second set of electrically conductive terminals 125 (only a portion being shown in FIG. 1A for clarity and ease of

illustration). According to one embodiment, the second set of terminals 125 is arranged in a pattern to mate with a corresponding array of terminals disposed on a next level component, such as a mainboard, a motherboard, or other circuit board (not shown in the figures). The terminals 125 may each comprise any suitable type of structure capable of forming an electrical connection with a terminal of the next-level component. By way of example, a terminal 125 may comprise a pad, land, solder bump or other metal bump, or a pin. The next-level component may include a socket (and retention mechanism) to receive the substrate 100 and terminals 125, such as a Land Grid Array (LGA) socket or a Pin Grid Array (PGA) socket. Alternatively, the terminals 125 may be coupled with terminals on the next level component by a solder reflow process.

Disposed on the first surface 152 of core 150 is a first build-up structure 130, and disposed on the core's second surface 154 is a second build-up structure 140. The first build-up structure comprises one or more alternating layers of a dielectric material and a metal, and the terminals 120 are disposed on the first build-up structure 130 (the first substrate side 102 generally corresponding to an outer surface of the first build-up structure 130). At least one of the conductors 160 in multi-layer glass core 150 is electrically coupled with at least one metal layer of the first build-up structure 130, and in one embodiment a metal layer of the first build-up structure nearest the core 150 is coupled with at least one conductor 160. Similarly, the second build-up structure 140 comprises one or more alternating layers of a dielectric material and a metal, and the terminals 125 are disposed on the second build-up structure 140 (the second substrate side 104 generally corresponding to an outer surface of the second build-up structure 140). At least one of the conductors 160 in core 150 is electrically coupled with at least one metal layer of the second build-up structure 140, and in one embodiment a metal layer of the second build-up structure nearest the core 150 is coupled with at least one conductor 160. The first and second build-up structures 130, 140 route power, as well as input/output (I/O) signals, between the first and second sets of terminals 120, 125 (and, hence, facilitate the delivery of power and signaling between an IC die mounted on substrate 100 and a next-level component). Build-up structures 130, 140 are described in greater detail below.

Referring to FIG. 1C, an embodiment of the multi-layer glass core substrate 100 is illustrated in greater detail. As previously described, the substrate includes a core 150 comprised of glass layers 157a, 157b, and 157c, with the core having a first surface 152 and an opposing second surface 154. Bonding layers 158a, 158b are disposed between the

glass layers 157a-c, as noted above. Although three glass layers are shown in FIGS. 1A through 1G, the core 150 may comprise any suitable number of glass layers (e.g., two layers, four or more layers, etc.), depending upon the desired mechanical and electrical characteristics of the substrate 100. The glass layers 157a-c may have any suitable thickness, and in one embodiment each glass layer has a thickness of between approximately 50 and 200 micrometers. Also, in one embodiment the glass layers 157a-c may all have the same thickness (as depicted in the figures), or alternatively any one of the glass layers 157a-c may have a thickness different than one or more of the other glass layers. Bonding layers 158a-b may also have any suitable thickness, and in one embodiment each bonding layer has a thickness of between approximately 20 and 100 micrometers. According to one embodiment, the bonding layers 158a-b all have the same thickness (as shown in the figures); however, in other embodiments any one of the bonding layers 158a-b may have a thickness different than one or more of the other bonding layers.

The discrete glass layers 157a, 157b, 157c may be bonded together by any suitable technique. In one embodiment, bonding layers 158a, 158b are disposed between the glass layers, and each of these layers is coupled with two adjacent glass layers (e.g., bonding layer 158a is coupled with glass layers 157a and 157b, and so on). According to one embodiment, each bonding layer 158a, 158b includes an adhesive, and in a further embodiment the bonding layers 158a, 158b comprise an organic material. In one embodiment, each bonding layer 158a, 158b comprises a dry film adhesive material, such as a film comprised of an acrylic resin or an epoxy resin. It should, however, be understood that the disclosed embodiments are not limited to adhesive bonding and, further, that the multi-layer glass core 150 may be formed without adhesives. In some embodiments, the glass layers 157a-c may be joined together by diffusion bonding. For example, in one embodiment, the bonding layers 158a-b comprise a material that is capable of forming a diffusion bond with the glass material of layers 157a-c (e.g., bonding layer 158a would form a diffusion bond with each of glass layers 157a and 157b, and so on). Alternatively, the glass layers 157a-157c may be diffusion bonded directly to one another (e.g., glass layer 157a is diffusion bonded with glass layer 157b, and so on), in which case the bonding layers 158a-b may be omitted. In other embodiments, the glass layers 157a-c may be mechanically joined together. By way of example, in one embodiment, the conductive material 160 deposited in thru-holes 165 may function to

secure the glass layers 158a-158c together. In a further embodiment, glass layers 157a-c may be secured together using direct oxide-to-oxide bonding.

According to one embodiment, first build-up structure 130 comprises a number of dielectric material layers 133a, 133b, 133c, 133d, and a number of metal layers 136a, 136b, 136c. Dielectric layers 133a-d may comprise any suitable dielectric material (e.g., polymer materials, etc.) and may be formed by any suitable technique (e.g., by deposition, lamination, etc.). Metal layers 136a-c may comprise any suitable electrically conductive metal (e.g., copper, aluminum, silver, etc.), and may be deposited by any suitable technique (e.g., plating processes, such as electroplating and electroless plating). Further, the metal layers 136a-c may each be patterned to form any suitable number and configuration of traces, power planes, ground planes, and other conductors to facilitate the routing of power and I/O signals.

One of the dielectric layers 133a-d is disposed between any two adjacent metal layers 136a-c (e.g., metal layers 136a and 136b are separated by dielectric layer 133b, and so on), and dielectric layer 133a lies adjacent the core 150 and separates the metal layer 136a from the core. According to one embodiment, the dielectric layer 133a lies directly adjacent the core's first surface 152. Vias 139a, 139b, 139c – which are plated or filled with metal – extend through the dielectric layers 133a, 133b, 133c, respectively, and interconnect adjacent metal layers (e.g., vias 139b interconnect metal layers 136a and 136b, and so on). Further, the metal layer 136a nearest the multi-layer glass core 150 is coupled with one or more of the conductors 160 by vias 139a disposed in dielectric layer 133a. In one embodiment, the first surface 152 of core 150 may include a surface treatment or coating to increase adhesion with the dielectric material of the build-up structure 130. Also, in some embodiments, the outermost dielectric layer 133d may comprise a resist layer and/or a passivation layer. Also, according to one embodiment, terminals 120 are formed by, or formed on, the outermost metal layer 136c.

In one embodiment, second build-up structure 140 comprises a number of dielectric material layers 143a, 143b, 143c, 143d, and a number of metal layers 146a, 146b, 146c. Dielectric layers 143a-d may comprise any suitable dielectric material (e.g., polymer materials, etc.) and may be formed by any suitable technique (e.g., by deposition, lamination, etc.). Metal layers 146a-c may comprise any suitable electrically conductive metal (e.g., copper, aluminum, silver, etc.), and may be deposited by any suitable technique (e.g., plating processes, such as electroplating and electroless plating). Further,

the metal layers 146a-c may each be patterned to form any suitable number and configuration of traces, power planes, ground planes, and other conductors to facilitate the routing of power and I/O signals.

One of the dielectric layers 143a-d is disposed between any two adjacent metal layers 146a-c (e.g., metal layers 146a and 146b are separated by dielectric layer 143b, and so on), and dielectric layer 143a lies adjacent the core 150 and separates the metal layer 146a from the core. According to one embodiment, the dielectric layer 143a lies directly adjacent the core's second surface 154. Vias 149a, 149b, 149c – which are plated or filled with metal – extend through the dielectric layers 143a, 143b, 143c, respectively, and interconnect adjacent metal layers (e.g., vias 149b interconnect metal layers 146a and 146b, and so on). Further, the metal layer 146a nearest the multi-layer glass core 150 is coupled with one or more of the conductors 160 by vias 149a disposed in dielectric layer 143a. In one embodiment, the second surface 154 of core 150 may include a surface treatment or coating to increase adhesion with the dielectric material of the build-up structure 140. Also, in some embodiments, the outermost dielectric layer 143d may comprise a resist layer and/or a passivation layer. In addition, in one embodiment, terminals 125 are formed by, or formed on, the outermost metal layer 146c.

In the embodiment of FIG. 1C (as well as the embodiments shown in each of FIGS. 1D and 1G), the first and second build-up structures have the same number of dielectric and metal layers and, further, have generally equivalent thicknesses. However, the disclosed embodiments are not so limited, and in other embodiments the first and second build-up structures may have differing thicknesses and/or differing numbers of dielectric and metal layers. According to another embodiment, a build-up structure is disposed on only one side of the multi-layer glass core 150. Also, in some embodiments, the first and second build-up structures are constructed from the same dielectric material and metal. In other embodiments, however, the first and second build-up structures may have differing materials.

In the embodiment of FIG. 1C, dielectric layers 133a and 143a are positioned adjacent the multi-layer glass core 150, and the metal layers nearest the core (i.e., metal layers 136a and 146a) are separated from the core by these dielectric layers. In an alternative embodiment, as illustrated in FIG. 1D, a metal layer may lie adjacent the multi-layer glass core 150. The incorporation of a metal layer adjacent one or both sides of the core 150 is sometimes referred to as “core layer routing.”

Referring to FIG. 1D, the embodiment of substrate 100 is generally similar to that shown in FIG. 1C (and like features are identified by the same reference numerals).

However, in the embodiment of FIG. 1D, the first build-up structure 130 includes a metal layer 136x adjacent the multi-layer glass core 150, and according to one embodiment the

5 metal layer 136x is directly adjacent the core's first surface 152. Dielectric layer 133a overlies the metal layer 136x (and exposed portions of the core), this metal layer 136x now being the metal layer nearest the core, and at least one of the conductors 160 is coupled with metal layer 136x. Further, in another embodiment, the first surface 152 of core 150 may include a surface treatment or coating to increase adhesion with the metal
10 layer 136x (and perhaps with portions of dielectric layer 133a).

Similar to first build-up structure 130, the second build-up structure 140 of FIG.

1D includes a metal layer 146x adjacent the multi-layer glass core 150, and in one embodiment the metal layer 146x is directly adjacent the core's second surface 154.

Dielectric layer 143a overlies the metal layer 146x (and exposed portions of the glass

15 core), this metal layer 146x now being the metal layer nearest the core, and at least one of the conductors 160 is coupled with metal layer 146x. In addition, in another embodiment, the second surface 154 of core 150 may include a surface treatment or coating to increase adhesion with the metal layer 146x (and perhaps with portions of dielectric layer 143a). In some embodiments, only one of the core's opposing surfaces 152, 154 has an adjacent
20 metal layer (e.g., either one of metal layers 136x, 146x in the first and second build-up structures 130, 140, respectively, may be omitted).

With reference now to FIG. 1E, a further embodiment of multi-layer glass core substrate 100 is illustrated. The embodiment of substrate 100 shown in FIG. 1E is generally similar to that shown in FIG. 1C (and like features are identified by the same reference

25 numerals). However, in the embodiment of FIG. 1E, the hole or via 165 in which each conductor 160 is disposed has a wall that is tapered through the thickness of the core 150.

In one embodiment, the tapered wall of hole or via 165 has an angle 167 relative to a centerline of the hole of between 0 and 45 degrees. The tapered wall of a hole 165 may be the result of the process used to form the hole through the multi-layer glass core 150. As
30 noted above, processes that may be utilized to form a hole or via 165 include, for example, etching, laser drilling, imprinting, and sand blasting. Depending upon the processing conditions, any one of the aforementioned techniques may form a hole 165 having a tapered wall. It should be understood that, depending upon the formation technique and

process conditions, a via may have a shape other than the straight tapered wall depicted in FIG. 1E. For example, in other embodiments, the walls of a via may be curved (e.g., a via may have a scalloped cross-sectional profile).

Turning next to FIG. 1F, a further embodiment of the multi-layer glass core substrate 100 is illustrated. The embodiment of substrate 100 shown in FIG. 1E is generally similar to that shown in FIG. 1C (and like features are identified by the same reference numerals). However, in the embodiment of FIG. 1F, the hole or via 165 in which each conductor 160 is disposed comprises a number of separate, aligned holes formed in each of the discrete glass layers 157a, 157b, 157c and bonding layers 158a, 158b. For example, a thru-hole 165 may comprise a via 159a in glass layer 157a, a via 159b in bonding layer 158a, a via 159c in glass layer 157b, a via 159d in bonding layer 158b, and a via 159e in glass layer 157c. Generally, these separate holes 159a-e are aligned along a common centerline; however, in some embodiments there may be misalignment between these separate holes.

According to one embodiment, the vias formed in the glass layers (e.g., vias 159a, 159c, 159e and perhaps bonding layers 158a, 158b) may have a wall that is tapered through the thickness of that glass layer (or bonding layer). In one embodiment, the tapered wall of a via has an angle 169 relative to a centerline of the hole of between 0 and 45 degrees. The tapered wall of a via (e.g., a via 159a-e) may be the result of the formation process. As noted above, processes that may be utilized to form a via through a glass layer (and through a bonding layer) include, for example, etching, laser drilling, imprinting, and sand blasting. Depending upon the processing conditions, any one of the aforementioned techniques may form a via having a tapered wall. It should be understood that, depending upon the formation technique and process conditions, a via may have a shape other than the straight tapered wall depicted in FIG. 1F. In other embodiments, the walls of a via may be curved. For example, a via may have a scalloped cross-sectional profile (see, e.g., FIG. 8J).

With reference now to FIG. 1G, a further embodiment of multi-layer glass core substrate 100 is illustrated. The embodiment of substrate 100 shown in FIG. 1G is generally similar to that shown in FIG. 1C (and like features are identified by the same reference numerals). However, in the embodiment of FIG. 1G, any one or more of the bonding layers 158a, 158b may include conductors. For example, bonding layer 158a may include conductors 198a, and bonding layer 158b may include conductors 198b. The

conductors 198a, 198b may comprise traces for routing I/O signals and/or for routing power. Further, the conductors 198a, 198b on any one or more of the bonding layers 158a, 158b may comprise a power plane or a ground plane. Conductors 198a, 198b may comprise any suitable electrically conductive material, such as a metal (e.g., copper,
5 nickel, aluminum, silver, gold, as well as alloys of these and/or other metals), a conductive polymer, or a composite material. Also, although both bonding layers 158a, 158b in FIG. 1G include conductors, in other embodiments not all bonding layers will include conductors.

Illustrated in FIG. 2 is an embodiment of an assembly 200 including a multi-layer
10 glass core substrate 100. With reference to FIG. 2, the assembly 200 includes substrate 100 having a multi-layer glass core 150, as well as a first side 102 and an opposing second side 104. Disposed on the substrate's first side 102 is an integrated circuit (IC) die 210. The IC die 210 is electrically (and mechanically) coupled with the substrate 100 by a number of interconnects 220. Terminals 125 (e.g., lands, pins, solder bumps, etc.) on the
15 substrates second side 104 (see FIG. 1A) may be used to form electrical connections with a next-level component, such as a motherboard, mainboard, or other circuit board. A heat spreader or lid 230 – having a first surface 232 and an opposing second surface 234 that faces a back surface 215 of the die – is disposed over the die 210 and thermally coupled with (and perhaps mechanically coupled with) the die's back surface 215 by a layer of
20 thermal interface material 240. An adhesive or sealant 290 may be used to secure the heat spreader 230 to the first surface 102 of glass core substrate 100. Although not shown in FIG. 2, in a further embodiment a heat sink (or other cooling device) may be thermally coupled with the heat spreader 230, and another layer of a thermal interface material may be disposed between the heat spreader's first surface 232 and the heat sink (or other
25 device).

IC die 210 may comprise any type of semiconductor device. In one embodiment, the IC die 210 comprises a processing system or device. For example, IC die 210 may comprise a microprocessor or a graphics processor. The IC die 210 can perform instructions from any number of processor architectures having any number of instruction
30 formats. In one embodiment, an instruction is an "x86" instruction, as used by Intel Corporation. However, in other embodiments, the processor may perform instructions from other architectures or from other processor designers. In another embodiment, the IC die 210 comprises a memory device. According to a further embodiment, the IC die 210

comprises a system-on-chip (SoC). In yet another embodiment, the IC die 210 may include digital circuitry, analog circuitry, or a combination of both analog and digital circuitry.

Interconnects 220 are formed by coupling terminals 120 on the substrate first surface 102 (see FIG. 1A) with terminals on the IC die 210 by, for example, a solder reflow process. As previously described, the substrate terminals 120 may each comprise a pad, pillar, or stud bump formed from any suitable metal or combination of metals (e.g., copper, nickel, aluminum, etc.), and the die terminals may also comprise a pad, pillar, or stud bump formed from any suitable metal or combination of metals. Solder (e.g., in the form of balls or bumps) may be disposed on the substrate and/or die terminals, and these terminals may then be joined using a solder reflow process. It should be understood that the aforementioned interconnects are but one example of the type of interconnects that can be formed between substrate 100 and IC die 210 and, further, that any other suitable type of interconnect may be utilized. In addition, a layer of underfill material (not shown in FIG. 2) may be disposed around the interconnects 220 and between the IC die 210 and the substrate's first side 102.

Heat spreader 230 may be comprised of any suitable thermally conductive materials and may have any suitable shape or structure. According to one embodiment, the heat spreader 230 comprises a lid having a side wall (or walls) 237 extending towards the substrate's first side 102, with this wall (or walls) being secured to the substrate surface 102 by the adhesive 290. The above-described lid is sometimes referred to as an integrated heat spreader, or IHS. Materials that may be used to construct the heat spreader 230 include metals (e.g., copper and alloys thereof), thermally conductive composites, and thermally conductive polymers.

In the embodiment illustrated in FIG. 2, the assembly 200 includes a single IC die 210. However, in other embodiments, the assembly 200 may comprise a multi-chip package. For example, one or more other integrated circuit die (e.g., a memory device, a voltage regulator, etc.) may be disposed on the substrate 100. In addition, passive devices, such as capacitors and inductors, may be disposed on the glass core substrate 100 or, alternatively, integrated into the build-up structures 130, 140 of the substrate. By way of example, an array capacitor or a thin-film capacitor may be integrated into the build-up structures 130, 140 of the substrate 100. In another embodiment, a wireless component, such as an antenna or an RF shield, may be disposed on glass core substrate 100 or

integrated into the build-up structures 130, 140 of this substrate. These additional devices, whether IC die, passive devices, or other components, may be disposed on either side 102, 104 of the glass core substrate 100.

The assembly 200 may form part of any type of computing device. According to one embodiment, the assembly 200 may form part of a server or desktop computer. In another embodiment, the assembly 200 forms part of a lap-top computer or similar mobile computing device (e.g., a net-top computer). In a further embodiment, the assembly 200 comprises part of a hand-held computing device, such as a cell phone, a smart phone, or a mobile internet device (MID). In yet another embodiment, the assembly 200 forms part of an embedded computing device.

Illustrated in FIG. 3 an embodiment of a method of making a multi-layer glass core substrate. The method of FIG. 3 is further illustrated in FIGS. 4A-4C, and reference should be made to these figures as called out in the text below.

Referring to block 310 in FIG. 3, in one embodiment a multi-layer glass core having one or more thru-holes is provided. This is illustrated in FIG. 4A, where a core 450 is shown. Multi-layer glass core 450 may comprise any of the embodiments of core 150 previously described and shown in FIGS. 1A through 1G. The multi-layer glass core 450 includes discrete glass layers 457a, 457b, 457c secured together by bonding layers 458a, 458b, with the core including a first surface 452 and an opposing second surface 454 that is generally parallel with first surface 452. Holes or vias 465 extend from the first surface 452 to second surface 454. The glass layers 457a-c of core 450 may comprise any suitable type of glass and have any suitable thickness (see discussion above), depending upon the application and/or desired characteristics. According to one embodiment, the core 450 is of a size and configuration to enable formation of a single substrate. In a further embodiment, the core 450 is of a size and configuration to enable the formation of two or more substrates (e.g., the core 450 comprises a panel from which two or more substrates will be cut). Various embodiments of a method of forming a multi-layer glass core, such as core 450, having one or more thru-holes are shown in each of FIGS. 5, 7, 9 and 11, and these embodiments will be described in greater detail below.

Referring to block 320, an electrically conductive material is disposed in the thru-holes to form conductors. This is illustrated in FIG. 4B, where an electrically conductive material has been disposed in the holes 465 to form conductors 460.

The electrically conductive material 460 may be deposited in the vias 465 by any suitable process, such as, for example, plating techniques (electroplating or electroless plating), CVD, PVD, or screen printing techniques, as well as any combination of these and/or other processes. The material forming conductors 460 in core 450 may comprise
5 any suitable electrically conductive material, including metals, composite materials, and electrically conductive polymers. Suitable metals include copper, tin, silver, gold, nickel, aluminum, and tungsten, as well as alloys of these and/or other metals.

One embodiment of a method of forming conductors in the thru-holes of a multi-layer glass core is illustrated in FIG. 13, which will now be discussed. Embodiments of
10 the method of FIG. 13 are further illustrated in the schematic diagrams of FIGS. 14A through 14C, and reference should be made to FIGS. 13 and 14A-14C as called out in the text below.

Turning now to block 1305 in FIG. 13, a seed layer or adhesion layer is disposed over the walls of thru-holes in a multi-layer glass core. This is further illustrated in FIG.
15 14A, which shows a core 1450. Core 1450 comprises glass layers 1458a, 1458b, 1458c, 1458d coupled together by bonding layers 1458a, 1458b, 1458c (e.g., bonding layer 1458a is coupled to both glass layers 1457a and 1457b, and so on). Thru-holes 1465 extend through core 1450 from a first surface 1452 to a second opposing surface 1454 of the core. The holes 1465 may be formed by any suitable method or combination of methods, such
20 as etching, laser drilling, imprinting, and sand blasting. Disposed over walls of the thru-vias 1465 is a seed layer 1466. It should be noted that, in other embodiments, one or more other material layers may be deposited prior to seed layer 1466. For example, prior to deposition of seed layer 1466, a dielectric layer may be deposited over walls of thru-vias 1465 (e.g., to achieve desired capacitance, to achieve desired electrical isolation, etc.).

25 A subsequent layer of metal will be deposited over the seed layer 1466, and the seed layer 1466 may comprise any material capable of adhering to the glass material of layers 1457a-d (and material of bonding layers 1457a-c) and to the subsequent layer of metal to be deposited. Suitable seed layer materials include copper, titanium, chromium, nickel, or vanadium, as well as alloys of these and/or other metals. Further, the seed layer
30 1466 may be deposited using any suitable technique, including electroless plating, electroplating, CVD, or PVD. In one embodiment, a blanket deposition technique is employed, and the seed layer 1466 may extend over the first and second surfaces 1452, 1454 of the core 1450, as shown in FIG. 14A. The seed layer 1466 may have any suitable

thickness, and in one embodiment this layer has a thickness of between 0.1 micrometers and 0.5 micrometers.

As set forth in block 1315, metal is disposed over the seed layer. This is illustrated FIG. 14B, where a metal layer 1467 has been disposed over the seed layer 1466. Metal
5 layer 1467 may comprise any suitable electrically conductive metal, such as copper, aluminum, nickel, silver, or gold, as well as alloys of these and/or other metals. The metal layer 1467 may be deposited using any suitable technique, including electroless plating, electroplating, CVD, or PVD. In one embodiment, a blanket deposition technique is employed, and the metal layer 1467 may extend over the first and second surfaces 1452,
10 1454 of the core 1450, as shown in FIG. 14B. The metal layer 1467 may have any suitable thickness, and in one embodiment this layer has a thickness of between 5 micrometers and 30 micrometers. In another embodiment, the metal 1467 deposited over the seed layer 1466 substantially fills the thru-holes 1465.

Referring next to block 1325, a dielectric material is disposed over the metal layer
15 to fill the thru-holes. This is illustrated in FIG. 14C, where a dielectric material 1468 has been disposed over the metal layer 1467 to fill the interior void of each hole 1465. Dielectric material 1468 may comprise any suitable material, and in one embodiment the dielectric material 1468 comprises an organic material. Further, the dielectric material 1468 may be deposited using any suitable technique, such as screen printing, CVD, or
20 PVD. Again, however, the metal layer 1467 may substantially fill the thru-holes 1465, in which case the dielectric material may be omitted. In a further embodiment, as shown in FIG. 14C, excess seed layer 1466 and excess metal layer 1467 may be removed from the first and second surfaces 1452, 1454 of the core 1450. The excess seed and metal layers may be removed from the surfaces 1452, 1454 by, for example, a grinding process, a
25 chemical-mechanical polishing technique, or an etching process.

Returning now to FIG. 3, and block 330 in particular, one or more build-up layers is disposed on each side of the multi-layer glass core (or perhaps only one side) to create build-up structures, as previously described. This is shown in FIG. 4C, where a first build-up structure 430 has been formed on the first surface 452 of core 450, and a second build-up
30 structure 440 has been formed on the core's second surface 454. Each build-up structure 430, 440 may comprise any suitable number of alternating layers of dielectric material and metal (e.g., one or more), and they may be formed by any suitable techniques. The structure and formation of such build-up structures is described in greater

detail with reference to FIGS. 1B through 1G and the accompanying text above. In one embodiment, at least one of the conductors 460 is electrically coupled with a metal layer of the first build-up structure 430 that is nearest the core 450, and in a further embodiment at least one of the conductors 460 is electrically coupled with a metal layer of the second build-up structure 440 that is nearest the core. The combination of multi-layer glass core
5 450 and build-up structures 430, 440 may comprise a substrate 400 for an integrated circuit device.

With reference now to block 340 in FIG. 3, electrically conductive terminals may be formed on the substrate (terminals are not shown in FIGS. 4A-4C). A first set of
10 terminals may be formed on the first build-up structure 430, and a second set of terminals may be formed on the second build-up structure 440. The structure and formation of such terminals is described in greater detail with reference to FIGS. 1A through 1G and the accompanying text above.

As noted above, in one embodiment, the multi-layer glass core 450, as well as first
15 and second build-up structures 430, 440, includes structures and features corresponding to two or more substrates. In this embodiment, the core 450 (with build-up structures 430, 440) will be singulated into these discrete substrates (either before or after formation of the terminals).

Turning now to FIG. 5, illustrated is an embodiment of a method of forming a
20 multi-layer glass core having one or more thru-holes. Embodiments of the method shown in FIG. 5 are further illustrated in the schematic diagrams of FIGS. 6A through 6C, and reference should be made to these figures as called out in the text below.

Referring to block 510 in FIG. 5, a multi-layer glass plate is provided. This is illustrated in FIG. 6A, where a multi-layer glass plate 605 is shown. Plate 605 comprises a
25 number of glass layers 657a, 657b, 657c, 657d attached together by bonding layers 658a, 658b, 658c (e.g., bonding layer 658a is coupled with glass layers 657a and 657b, and so on). Multi-layer glass plate 605 also includes a periphery 651 that extends between a first surface 652 and a second surfaces 654. According to one embodiment, the multi-layer glass plate 605 may have a thickness between 50 micrometers and 800 micrometers. In
30 one embodiment, the multi-layer glass plate is of a size and configuration to enable formation of a single substrate core. In a further embodiment, the plate 605 is of a size and configuration to enable the formation of two or more substrate cores (e.g., plate 605

comprises a panel from which two or more substrate cores, or two or more substrates, will be cut).

The individual glass layers 657a-d may comprise any suitable type of glass. In one embodiment, the glass layers 657a-d comprise the same glass material; however, in other
5 embodiments any one of the glass layers 657a-d may comprise a glass material that is different than the glass material of any of the other glass layers. Although four glass layers are shown in FIGS. 6A through 6C, the plate 605 may comprise any suitable number of glass layers (e.g., two layers, three layers, five or more layers, etc.), depending upon the desired mechanical and electrical characteristics of the core (or cores) to be
10 formed from plate 605. Glass layers 657a-d may have any suitable thickness, and in one embodiment each glass layer has a thickness of approximately 50 to 200 micrometers. Also, in one embodiment the glass layers 657a-d may all have the same thickness (as depicted in the figures), or alternatively any one of the glass layers 657a-d may have a thickness different than one or more of the other glass layers.

15 The bonding layers 658a-c may also have any suitable thickness, and in one embodiment each bonding layer has a thickness of approximately 20 to 100 micrometers. According to one embodiment, the bonding layers 658a-c all have the same thickness (as shown in the figures); however, in other embodiments any one of the bonding layers 658a-c may have a thickness different than one or more of the other bonding layers.

20 The discrete glass layers 657a, 657b, 657c, 657d may be bonded together by any suitable technique. In one embodiment, as shown in the figures, bonding layers 658a, 658b, 658c are disposed between the glass layers, and each of these layers is coupled with two adjacent glass layers (e.g., bonding layer 658a is coupled with glass layers 657a and 657b, and so on). According to one embodiment, each bonding layer 658a-c includes an
25 adhesive, and in a further embodiment the bonding layers comprise an organic material. In one embodiment, each bonding layer 658a-c comprises a dry film adhesive material, such as a film comprised of an acrylic resin or an epoxy resin.

Various methods of coupling multiple glass layers together using adhesive bonding layers will now be described with respect to FIG. 15 and FIGS. 16A through 16E. First,
30 however, it should be understood that the disclosed embodiments are not limited to adhesive bonding and, further, that the multi-layer glass plate 605 (and, hence, a core formed from this plate) may be created without adhesives. For example, as previously described, in other embodiments, multiple glass layers may be coupled together using

direct oxide-to-oxide bonding, diffusion bonding (either with or without intermediate layers between adjacent glass layers), or these glass layers may be secured together mechanically (e.g., as by material deposited in thru-holes extending through the plate 605), as well as by any combination of these and/or other techniques.

5 Turning to FIG. 15, in one embodiment, a multi-layer glass plate is formed using a roller lamination process. In the embodiment of FIG. 15, a first source of glass sheet 1511a, a first source of adhesive film 1512a, a second source glass sheet 1511b, a second source of adhesive film 1512b, and a third source of glass sheet 1511c are compressed together between rollers 1501 and 1502 in a continuous manner to form a multi-layer glass
10 laminate 1503. Multi-layer glass laminate comprises discrete glass layers 1557a, 1557b, and 1557c coupled together by adhesive layers 1558a and 1558b, as shown. Any suitable number of glass sheets may be joined together by adhesive layers to form the glass laminate 1503. The glass laminate 1503 may then be cut to any suitable lengths to form one or more multi-layer glass plates (e.g., a plate 605 having four glass layers coupled
15 together by three adhesive layers, etc.).

With reference now to FIGS. 16A through 16E, in another embodiment, a multi-layer glass plate is formed by lamination on a removable carrier. As shown in FIG. 16A, a first glass layer 1657a is adhered to a removable carrier 1602 by a releasable adhesive 1604. In one embodiment, the releasable adhesive 1604 comprises an adhesive material
20 that degrades under exposure to ultra violet (UV) light. In another embodiment, the releasable adhesive 1604 comprises an adhesive material that degrades under exposure to a solvent. As shown in FIG. 16B, a first adhesive layer 1658a is disposed over glass layer 1657a. In one embodiment, the adhesive layer 1658a comprises a dry film adhesive, and in another embodiment the adhesive layer 1658a comprises a liquid adhesive that is
25 sprayed or printed on the glass layer 1657a and then cured. Referring to FIG. 16C, a second glass layer 1657b is then disposed on the first adhesive layer 1658a, and the aforementioned processes are repeated. For example, as shown in FIG. 16D, a second adhesive layer 1658b (applied as either a dry film or a liquid) is disposed over glass layer 1657b, and a third glass layer 1657c is disposed over this second adhesive layer. As
30 shown in FIG. 16E, the carrier 1602 is released by degradation of the releasable adhesive 1604 (e.g., by application of UV light, by application of a solvent, etc.), leaving a free-standing multi-layer glass plate 1605.

Returning now to FIG. 5, a mask layer is disposed on the multi-layer glass plate and patterned, as set forth in block 520. This is also illustrated in FIG. 6A, where a mask layer 680 has been disposed over the first surface 652 of plate 605. Further, the mask layer 680 is patterned to form openings 685. Mask layer 680 may comprise any material capable of adhering to the glass material of layer 657a, and that is also amendable to patterning. For example, the mask layer 680 may comprise a photoresist material which can be patterned by photolithography and etching techniques. In addition, the mask layer 680 comprises a material that can withstand subsequent removal of portions of the glass layers and bonding layers (e.g., wet etching processes).

As set forth in block 530, holes are formed through all the glass layers, as well as the bonding layers. This is illustrated in FIG. 6B, where thru-holes 665 have been formed at locations corresponding to openings 685 in mask layer 680. The holes 665 extend through all glass layers 657a-d and all of the bonding layers 658a-c. However, in other embodiments, one or more of the holes 665 may extend through only a portion of the plate's thickness. According to one embodiment, the vias 665 are formed by a wet etching process (or processes) utilizing an etch chemistry (or chemistries) that will remove the glass and bonding layers. For example, an etchant that can remove glass may comprise a solution including hydrofluoric acid (HF), or alternatively an oxide etch or buffered oxide etch may be employed. An etchant that can remove the material of bonding layers 658a-c may comprise a solution including an appropriate solvent. In another embodiment, the vias 665 may be formed by a dry etching process (e.g., an etchant comprising fluorocarbon gas to remove the glass and an etchant comprising oxygen and/or hydrogen to remove the bonding layers). After formation of thru-holes 665, the mask layer 680 may be removed from the multi-layer glass plate, as set forth in block 540 and as shown in FIG. 6C.

In the embodiment of FIG. 5 (as well as the embodiments of FIGS. 7, 9, and 11, respectively), an etching process (or processes) is utilized to form vias in the various glass and bonding layer materials. However, it should be noted that the disclosed embodiments are not limited to hole formation by etching and, further, that other processes may be used to form thru-holes in a multi-layer core and/or to form vias in any individual glass or bonding layer. For example, a via may be formed in a glass layer by an imprinting process while the glass has been elevated to the softening temperature. By way of further example, a via may be formed in a glass or bonding layer by sand blasting.

With reference next to FIG. 7, illustrated is another embodiment of a method of making a multi-layer glass core having one or more thru-holes. Embodiments of the method shown in FIG. 7 are further illustrated in the schematic diagrams of FIGS. 8A through 8J, and reference should be made to these figures as called out in the following
5 below.

Referring to block 710 in FIG. 7, a multi-layer glass plate is provided. This is illustrated in FIG. 8A, which shows a multi-layer glass plate 805 having a first surface 852 and an opposing second surface 854. Plate 805 includes separate glass layers 857a, 857b, 857c, and 857d coupled together by bonding layers 858a, 858b, and 858c. Multi-layer
10 glass plate 805 may be similar to multi-layer glass plate 605 (see FIGS. 6A, 15, and 16, as well as the accompanying text above).

As set forth in block 720, a mask layer is disposed on the multi-layer glass plate and is patterned. This is also illustrated in FIG. 8A, where a mask layer 880 has been disposed over the first surface 852 of plate 805. In addition, the mask layer 880 is
15 patterned to form openings 885. Mask layer 880 may comprise any material capable of adhering to the glass material of layer 857a, and that is also amendable to patterning. By way of example, the mask layer 880 may comprise a photoresist material which can be patterned by photolithography and etching techniques. In addition, the mask layer 880 comprises a material that can withstand subsequent removal of portions of the glass layers
20 and bonding layers (e.g., wet etching processes).

As set forth in block 730, a hole or via is formed in one of the glass layers. This is illustrated in FIG. 8B, where vias 891 have been formed in the glass layer 857a at locations corresponding to openings 885 in mask layer 880. According to one embodiment, the vias 891 are formed by a wet etching process utilizing an etch chemistry
25 that will remove the glass layer 857a. In another embodiment, a dry etching process may be utilized to form a via in glass. Examples of suitable etchants for glass are described above.

As set forth in block 740, a protective layer is disposed on the glass layer in which the hole was previously formed. This is illustrated in FIG. 8C, where a protective layer
30 871 has been disposed over the walls of the vias 891 formed in glass layer 857a. Additional vias will be formed in the bonding layers and other glass layers to form thru-holes in the plate 605, and the function of the protective layer 871 is to prevent or substantially inhibit removal of the material of glass layer 857a during the formation of

these other vias (e.g., during subsequent etching processes on the bonding layers and other glass layers). The protective layer 871 may comprise any material capable of withstanding the aforementioned subsequent via formation processes, such as, for example, an organic material (e.g., benzocyclobutene, polytetrafluoroethylene, polyimide, etc.), a metal (e.g., platinum or gold), a metal oxide, or silicon nitride. Further, the protective layer 871 may be deposited over the walls of hole 891 using any suitable technique, such as atomic layer deposition (ALD) or CVD. In one embodiment, the protective layer 871 is deposited by a process that is selective to glass. In another embodiment, a non-selective blanket deposition process is used to deposit the protective material, and subsequently an anisotropic process is utilized to remove the protective material from the via bottoms.

As set forth in block 750, a hole or via is formed in one of the bonding layers. This is illustrated in FIG. 8D, where vias 892 have been formed in the bonding layer 858a at locations corresponding to openings 885 in mask layer 880. Each of the holes 892 is generally aligned relative to the overlying hole 891 in glass layer 857a (e.g., the centerlines of holes 891 and 892 are approximately coincident). According to one embodiment, the vias 892 are formed by a wet etching process, and in another embodiment the vias 892 may be formed using a dry etching process. Examples of suitable etchants for the bonding layer material are described above.

As shown in FIG. 7, the previously described steps are repeated, as needed, to form holes through the multi-layer glass plate. Thus, referring again to block 730, a hole is formed in the next glass layer. This is illustrated in FIG. 8E, where holes 893 have been formed in glass layer 857b. Holes 893 may be formed as described above, and these holes are generally aligned with the previously formed vias 891 and 892 (e.g., the centerlines of holes 891, 892, 893 are approximately coincident). As set forth in block 740, a protective layer is disposed on the glass layer in which the holes were formed. This is illustrated in FIG. 8F, where a protective layer 873 has been disposed over walls of the previously formed holes 893 in glass layer 857b. Protective layer 873 is similar to the protective layer 871, as described above. Referring to block 750, a hole or via is then formed in the next bonding layer. This is illustrated in FIG. 8G, where holes 894 have been formed in the bonding layer 858b, wherein the holes 894 are generally aligned with previously formed vias 891 through 893.

The hole formation processes described above with respect to block 730, 740, and 750 may be repeated, as needed, to form holes extending through the multi-layer glass plate 805. This is illustrated in FIG. 8H, where holes 895 have been formed in glass layer 857c, holes 896 have been formed in bonding layers 858c, and holes 897 have been
5 formed in glass layer 858d. Note that a protective layer 875 was deposited over walls of the holes 895 in glass layer 857c, the protective layer 875 being similar to the previously describe protective layer 871. All of the holes 891 through 897 have been formed at locations corresponding to openings 885 in mask layer 880, and these holes are generally aligned relative to each other (e.g., the centerlines of holes 891 through 897 are
10 approximately coincident).

When hole formation is complete, the mask layer and protective layers are removed, as set forth in block 760. This is illustrated in FIG. 8I, where mask layer 880 and protective layers 871, 873, and 875 have been removed. A number of holes 865 now extend through the multi-layer glass plate 805 from the plate's first surface 852 to the
15 second opposing surface 854. Each thru-hole 865 comprises a series of holes 891, 892, 893, 894, 895, 896, and 897 formed in the glass layers 857a-d and bonding layers 858a-c. The aspect ratio of a hole or via can be defined as the via's length (or depth) divided by a maximum diameter of the via. One advantage of the process described in FIGS. 7 and 8A-8I is that thru-holes in the plate 805 having a large aspect ratio can be obtained. For
20 example, in one embodiment, the thru-holes 865 in multi-layer glass plate 805 may have an aspect ratio in a range of approximately 2 to 6.

In the embodiments of FIGS. 8A-8I, each of the vias 891, 893, 895, and 897 has a cross-sectional profile that is a generally straight taper through the thickness of their respective glass layer 857a, 857b, 857c, and 857d. However, as noted above, the shape of
25 a via formed in a glass layer (or bonding layer) may vary depending upon the fabrication technique (e.g., wet etching, dry etching, laser drilling, etc.), as well as the process characteristics. In other embodiments, for example, a via formed in one of the glass layers 857a-d (or one of the bonding layers 858a-c) may have a curved shape. By way of example, as shown in FIG. 8J, the vias 891, 893, 895, and 897 may have cross-sectional
30 profiles that are scalloped shaped. Any of the disclosed embodiments may incorporate such a scalloped shaped via. Further, the disclosed embodiments are not limited to such a scallop shape, and it should be understood that a via may have any suitable shape or profile.

Turning next to FIG. 9, illustrated is a further embodiment of a method of making a multi-layer glass core having one or more thru-holes. Embodiments of the method shown in FIG. 9 are further illustrated in the schematic diagrams of FIGS. 10A through 10H, and reference should be made to these figures as called out in the text below.

5 Referring to block 910 in FIG. 9, a mask layer is disposed on a first glass layer and is patterned. This is illustrated in FIG. 10A, where a mask layer 1080a has been disposed on a glass layer 1057a. The mask layer 1080a has been patterned to form openings 1085a. As set forth in block 920, holes are formed in the first glass layer. This is illustrated in FIG. 10B, where holes 1091 have been formed in the glass layer 1057a at locations
10 corresponding to openings 1085a in mask layer 1080a. As set forth in block 930 of FIG. 9, a second glass layer is bonded to the first glass layer to form a two-layer structure. This is illustrated in FIG. 10C, where a second glass layer 1057b has been coupled with glass layer 1057a by bonding layer 1058. Referring to block 940, a mask layer is disposed on the second glass layer and patterned. This is illustrated in FIG. 10D, where mask layer
15 1080b has been disposed on glass layer 1057b and patterned to form openings 1085b. Holes are then formed in the second glass layer and bonding layer, as set forth in block 950. This is illustrated in FIG. 10E, where holes 1093 have been formed in glass layer 1057b and holes 1092 have been formed in bonding layer 1058. The holes 1091, 1092, 1093 are generally aligned (e.g., the centerlines of these holes are approximately
20 coincident). As set forth in block 960, the mask layers are removed. This is illustrated in FIG. 10F, where mask layers 1080a, 1080b have been removed, leaving a two-layer structure 1008 having thru-holes 1065, each thru-hole 1065 comprising a series of aligned holes 1091, 1092, 1093. The holes 1091, 1092, 1093 may be formed by any of the techniques previously described and, further, the glass layers 1057a, 1057b may be jointed
25 together by any of the aforementioned methods.

The two-layer structure 1008 of FIG. 10F may be used as a multi-layer glass core in a substrate (e.g., as core 150, or as core 450). Alternatively, the two-layer structure 1008 may comprise a panel from which multiple substrates may be formed. However, in another embodiment (see block 970), two or more of these two-layer structures may be
30 bonded together to form a multi-layer glass core (or a panel from which multiple substrates can be formed). This is illustrated, by way of example, in FIG. 10G, where a first two-layer structure 1008a is coupled with a second two-layer structure 1008b. Each two-layer structure includes a first glass layer 1057a coupled with a second glass layer

1057b by a bonding layer 1058, as described above. An additional bonding layer 1058x couples the first and second two-layer structures 1008a, 1008b to form a multi-layer glass core 1005 having thru-vias 1065. Each thru-via 1065 include a hole 1094x formed in the bonding layer 1058x. In one embodiment, the holes 1094x in bonding layer 1058x are
5 pre-formed prior to bonding of the two-layer structures 1008a, 1008b, and in another embodiment the holes 1094x are formed after bonding of these two-layer structures (e.g., as by etching or other suitable process).

In an alternative embodiment, as set forth in block 980, a protective layer is disposed on the first glass layer (and the second mask layer 1080b may be omitted). This is illustrated in FIG. 10H, where a protective layer 1071 is deposited over a wall of the
10 vias 1091 formed in first glass layer 1057a. Holes 1092 and 1093 in bonding and glass layers 1058, 1057b, respectively, may then be formed using mask layer 1080a and the openings 1085a of this layer. Protective layer 1071 may be similar to protective layer 871 described above. After formation of holes 892, 893, the protective layer 1071 is removed,
15 as is mask layer 1080a (see block 960). The two-layer structure of FIG. 10H may be used as a multi-layer glass core (e.g., as core 150, or as core 450), or this two-layer structure may be coupled with two or more additional two-layer structures (e.g., see FIG. 10G).

With reference now to FIG. 11, illustrated is yet another embodiment of a method of forming a multi-layer glass core having one or more thru-holes. Embodiments of the
20 method shown in FIG. 11 are further illustrated in the schematic diagrams of FIGS. 12A through 12E, and reference should be made to these figures as called out in the following text.

Referring to block 1110 in FIG. 11, a mask layer is disposed on a first glass layer and patterned. This is illustrated in FIG. 12A, where a mask layer 1280 has been disposed
25 on a glass layer 1257a, and the mask layer 1280 has been patterned to form openings 1285. As set forth in block 1120, holes are formed in the first glass layer. This is also shown in FIG. 12A, where holes 1291 have been formed in the glass layer 1257a at locations corresponding to openings 1285 of mask layer 1280. As set forth in block 1130 of FIG. 11, another glass layer is bonded to the first (or prior) glass layer. This is
30 illustrated in FIG. 12B, where a second glass layer 1257b has been coupled with glass layer 1257a by a first bonding layer 1058a. Referring to block 1240, a protective layer is disposed on the first (or prior) glass layer. This is also illustrated in FIG. 12B, where a protective layer 1271 has been disposed over walls of holes 1291 formed in the first glass

layer 1257a. Protective layer 1271 may be similar to the previously described protective layer 871. Holes are then formed in the bonding layer and next glass layer, as set forth in block 1150. This is illustrated in FIG. 12C, where holes 1292 have been formed in bonding layer 1258a and holes 1293 have been formed in second glass layer 1257b.

5 The process described above with respect to blocks 1130, 1140, and 1150 may then be repeated, as needed, to form a multi-layer glass core having any desired number of glass layers. For example, as shown in FIG. 12D, an additional glass layer 1257c has been bonded to second glass layer 1257b by a second bonding layer 1258b, and holes 1294 have been formed in the bonding layer 1258b and holes 1295 have been formed in the
10 glass layer 1257c. Note that a protective layer 1273 was disposed over walls of holes 1293 in second glass layer 1257b (see block 1140) prior to formation of holes 1295 in glass layer 1257c.

As set forth in block 1160, once the desired number of glass layers has been achieved, the mask layer and protective layers can be removed. This is illustrated in FIG.
15 12E, where mask layer 1280 and protective layers 1271 and 1273 have been removed. A multi-layer glass core 1205 having thru-holes 1265 remains. Each thru-hole comprises a series of holes 1291, 1292, 1293, 1294, and 1295 that are generally aligned (e.g., the centerlines of these holes are approximately coincident). The holes 1291, 1292, 1293, 1294, 1295 may be formed by any of the techniques previously described and, further, the
20 glass layers 1257a-c may be joined together by any of the aforementioned methods. In an alternative embodiment, the multi-layer glass structure 1205 comprises a panel from which multiple substrates may be formed. According to another embodiment, protective layers on the glass may be omitted (see dashed line on the left-hand side of FIG. 11).

At this juncture, it should be noted that the figures are schematic diagrams
25 provided as an aide to understanding the disclosed embodiments, and no unnecessary limitations should be implied from the figures. In some instances, a relatively small number of features may have been illustrated for clarity and ease of illustration. For example, the number of conductors 160, 460 (or holes 665, 865, 1065, 1265, 1465) extending through a multi-layer glass core (or multi-layer glass plate) shown in the figures
30 may be substantially less than a number of conductors (or thru-vias) that may, in practice, be disposed in such a substrate core. Also, the figures may not be drawn to scale, and in some cases lines (e.g., hidden lines) have been omitted for ease of understanding.

Glass materials may have a CTE of approximately 3.2 ppm, although the CTE value is temperature dependent and will also vary depending upon the composition of any particular glass material. Silicon may have a CTE of approximately 2.6 ppm, which again is temperature dependent. Organic polymer-based materials typically used in the construction of package substrates and circuit boards may have a CTE of approximately 12 or more (again, a value that is temperature and composition dependent). Although, as noted above, the CTE of a substance is temperature and composition dependent, the CTE mismatch between a silicon die and the underlying substrate is significantly reduced using a multi-layer glass core substrate as compared to a polymer-based substrate material. In addition, glass may have a modulus, E, of approximately 75 GPA, whereas commonly used organic polymer-based materials may have a modulus of approximately 25 GPa (the value of E also being dependent upon the composition of a substance). Thus, a multi-layer glass core substrate may provide a three-fold increase in modulus, which in some embodiments may provide the potential for a corresponding three-fold decrease in substrate warpage. A further advantage of glass is that it may be manufactured with more consistent flatness than common polymer materials.

The above-described reductions in CTE mismatch and warpage may enable the use of a smaller pitch for die-to-package interconnects, as well as a larger number of these interconnects, providing increase I/O capability. For example, in one embodiment, a pitch of 50 micrometers or less may be achieved for die-to-package interconnects when using a multi-layer glass core substrate. Large substrate warpage may lead to non-contact-open failures in the die-to-package interconnects during the chip attach process, as well as leading to high stresses within the die itself (e.g., within the inter-layer dielectric layers, or ILD layers, of the die), both of which can result in lower reliability. Thus, the disclosed multi-layer glass core substrate may enable the implementation of higher I/O packages while, at the same time, maintaining or improving reliability.

The foregoing detailed description and accompanying drawings are only illustrative and not restrictive. They have been provided primarily for a clear and comprehensive understanding of the disclosed embodiments and no unnecessary limitations are to be understood therefrom. Numerous additions, deletions, and modifications to the embodiments described herein, as well as alternative arrangements, may be devised by those skilled in the art without departing from the spirit of the disclosed embodiments and the scope of the appended claims.

CLAIMS

What is claimed is:

1. A substrate comprising:
a core including of a number of discrete glass layers, the core having a first surface and an
5 opposing second surface;
a number of conductors extending through the core from the first surface to the second
surface;
at least one dielectric layer and at least one metal layer disposed at the first surface of the
core, wherein the at least one metal layer at the first surface is electrically coupled
10 with at least one of the conductors;
at least one dielectric layer and a least one metal layer disposed at the second surface of
the core, wherein the at least one metal layer at the second surface is electrically
coupled with at least one of the conductors.
2. The substrate of claim 1, wherein the number of discrete glass layers are
15 coupled together by bonding layers, wherein one of the bonding layers is disposed
between adjacent glass layers.
3. The substrate of claim 2, wherein each of the bonding layers includes an
adhesive
4. The substrate of claim 2, wherein at least one of the bonding layers
20 includes an electrical conductor.
5. The substrate of claim 1, wherein each of the conductors comprises a hole
formed in the core and an electrically conductive material disposed in the hole.
6. The substrate of claim 5, wherein the electrically conductive material
comprises a metal.
- 25 7. The substrate of claim 1, wherein the at least one metal layer disposed at
the first surface of the core is disposed directly adjacent the first surface, and wherein the
at least one metal layer disposed at the second surface of the core is disposed directly
adjacent the second surface.
8. The substrate of claim 1, further comprising:
30 a first set of terminals disposed on at the first side of the core, the first set of terminals to
mate with a corresponding array of terminals on an integrated circuit (IC) die;

a second set of terminals disposed at the second side of the core, the second set of terminals to mate with a corresponding array of terminals on a next-level component.

9. A method comprising:

5 providing a plate including a number of glass layers bonded together, the plate having a first surface and an opposing second surface;

forming a first via in a first glass layer of the number of glass layers;

disposing a protective layer on a wall of the first via;

forming a second via in a second glass layer adjacent the first glass layer, the first via

10 generally aligned with the second via, the first and second vias forming at least part of a hole extending from the first surface to the second surface.

10. The method of claim 9, further comprising removing the protective layer.

11. The method of claim 9, further comprising:

depositing a seed layer over a wall of the hole; and

15 plating a metal over the seed layer to provide a conductor within the hole.

12. The method of claim 11, further comprising

disposing at least one dielectric layer and at least one metal layer at the first surface of the plate and electrically coupling the at least one metal layer at the first surface with the conductor; and

20 disposing at least one dielectric layer and a least one metal layer at the second surface of the glass core and electrically coupling the at least one metal layer at the second surface with the conductor.

13. The method of claim 12, wherein the at least one metal layer disposed at the first surface of the plate is disposed directly adjacent the first surface, and wherein the
25 at least one metal layer disposed at the second surface of the plate is disposed directly adjacent the second surface.

14. The method of claim 9, wherein the first glass layer is coupled with the second glass layer by a bonding layer, the method further comprising forming a via in the bonding layer, the via of the bonding layer forming part of the hole.

30 15. A method comprising:

forming a number of vias in a first layer of glass;

bonding a second layer of glass to the first glass layer to provide a first two-layer structure; and

forming a number of vias in the second glass layer, the vias of the first layer

approximately aligned with the vias of the second layer to provide a number of holes through the two-layer structure;

and, optionally, bonding the first two-layer structure with a second two-layer structure, the

5 number of holes of the first two-layer structure aligned with a number of holes in the second two-layer structure.

16. The method of claim 15, wherein the first two-layer structure provides a substrate core or wherein the first two-layer structure bonded with the second two-layer structure provides a substrate core.

10 17. The method of claim 15, further comprising disposing a bonding layer between the first and second glass layers, the bonding layer coupled with each of the first and second glass layers.

18. The method of claim 17, further comprising forming a number of vias in the bonding layer, the bonding layer vias approximately aligned with the vias in the first
15 glass layer and with the vias in the second glass layer.

19. The method of claim 15, further comprising disposing a bonding layer between the first two-layer structure and the second two-layer structure, the bonding layer coupled with each of the first and second two-layer structures.

20 20. The method of claim 19, further comprising forming a number of vias in the bonding layer, the bonding layer vias approximately aligned with the holes in the first two-layer structure and with the holes in the second two-layer structure.