Semiconductor device Package with Die Receiving Through-Hole and Connecting Through Hole and Method of the Same

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a structure of semiconductor device package, and more particularly to a structure of semiconductor device package with die receiving through-hole and connecting through hole and method of the same, the structure can reduce the package size and improve the yield and reliability.

2. Description of the Prior Art

In recent years, the high-technology electronics manufacturing industries launch more feature-packed and humanized electronic products. Rapid development of semiconductor technology has led to rapid progress of a reduction in size of semiconductor packages, the adoption of multi-pin, the adoption of fine pitch, the minimization of electronic components and the like. The purposes and the advantages of wafer level package includes decreasing the production cost, decreasing the effect caused by the parasitic capacitance and parasitic inductance by using the shorter conductive line path, acquiring better SNR (i.e. signal to noise ratio).

Because conventional package technologies have to divide a dice on a wafer into respective dies and then package the die respectively, therefore, these techniques are time consuming for manufacturing process. Since the chip package technique is highly influenced by the development of integrated circuits, therefore, as the size of

electronics has become demanding, so does the package technique. For the reasons mentioned above, the trend of package technique is toward ball grid array (BGA), flip chip ball grid array (FC-BGA), chip scale package (CSP), Wafer level package (WLP) today. "Wafer level package" is to be understood as meaning that the entire packaging and all the interconnections on the wafer as well as other processing steps are carried out before the singulation (dicing) into chips (dies). Generally, after completion of all assembling processes or packaging processes, individual semiconductor packages are separated from a wafer having a plurality of semiconductor dies. The wafer level package has extremely small dimensions combined with extremely good electrical properties.

In the manufacturing method, wafer level chip scale package (WLCSP) is an advanced packaging technology, by which the die are manufactured and tested on the wafer, and then singulated by dicing for assembly in a surface-mount line. Because the wafer level package technique utilizes the whole wafer as one object, not utilizing a single chip or die, therefore, before performing a scribing process, packaging and testing has been accomplished; furthermore, WLP is such an advanced technique so that the process of wire bonding, die mount and under-fill can be omitted. By utilizing WLP technique, the cost and manufacturing time can be reduced, and the resulting structure of WLP can be equal to the die; therefore, this technique can meet the demands of miniaturization of electronic devices. Further, WLCSP has an advantage of being able to print the redistribution circuit directly on the die by using the peripheral area of the die as the bonding points. It is achieved by redistributing an area array on the surface of the die, which can fully utilize the entire area of the die. The bonding points are located on the redistribution circuit by forming flip chip bumps so the bottom side of the die connects directly to the printed circuit board (PCB) with micro-spaced bonding points.

Although WLCSP can greatly reduce the signal path distance, it is still very difficult to accommodate all the bonding points on the die surface as the integration of die and internal components gets higher. The pin count on the die increases as integration gets higher so the redistribution of pins in an area array is difficult to achieve. Even if the redistribution of pins is successful, the distance between pins will be too small to meet the pitch of a printed circuit board (PCB). That is to say, such process and structure of prior art will suffer yield and reliability issues owing to the huge size of package. The further disadvantage of former method are higher costs and time-consuming for manufacture.

WLP technique is an advanced packaging technology, by which the die are manufactured and tested on the wafer, and then the wafer is singulated by dicing for assembly in a surface-mount line. Because the wafer level package technique utilizes the whole wafer as one object, not utilizing a single chip or die, therefore, before performing a scribing process, packaging and testing has been accomplished; furthermore, WLP is such an advanced technique so that the process of wire bonding, die mount and under-fill can be omitted. By utilizing WLP technique, the cost and manufacturing time can be reduced, and the resulting structure of WLP can be equal to the die; therefore, this technique can meet the demands of miniaturization of electronic devices.

Though the advantages of WLP technique mentioned above, some issues still exist influencing the acceptance of WLP technique. For instance, the coefficient of thermal expansion (CTE) difference (mismatching) between the materials of a structure of WLP and the mother board (PCB) becomes another critical factor to mechanical instability of the structure. A package scheme disclosed by US Patent No.

6,271,469 suffers the CTE mismatching issue. It is because the prior art uses silicon die encapsulated by molding compound. As known, the CTE of silicon material is 2.3, but the CTE of molding compound is around 20 - 80. The arrangement causes chip location be shifted during process due to the curing temperature of compound and dielectric layers materials are higher and the inter-connecting pads will be shifted that will causes yield and performance problem. It is difficult to return the original location during temperature cycling (it caused by the epoxy resin property if the curing Temp near/over the Tg). It means that the prior structure package can not be processed by large size, and it causes higher manufacturing cost.

Further, some technical involves the usage of die that directly formed on the upper surface of the substrate. As known, the pads of the semiconductor die will be redistributed through redistribution processes involving a redistribution layer (RDL) into a plurality of metal pads in an area array type. The build up layer will increase the size of the package. Therefore, the thickness of the package is increased. This may conflict with the demand of reducing the size of a chip.

Moreover, the prior art suffers complicated process to form the "Panel" type package. It needs the mold tool for encapsulation and the injection of mold material. It is unlikely to control the surface of die and compound at same level due to warp after heat curing the compound, the CMP process may be needed to polish the uneven surface. The cost is therefore increased.

In view of the aforementioned, the present invention provides a new structure with die receiving through-hole and connecting through hole and method for a **panel scale package (PSP)** to overcome the above drawback.

SUMMARY OF THE INVENTION

The present invention will descript some preferred embodiments. However, it is appreciated that the present invention can extensively perform in other embodiments except for these detailed descriptions. The scope of the present invention is not limited to these embodiments and should be accorded the following claims.

One objective of the present invention is to provide a structure of semiconductor device package and method of the same, which can provide a new structure of super thin package.

Another objective of the present invention is to provide a structure of semiconductor device package and method of the same, which can allow a better reliability due to the substrate and the PCB have the same coefficient of thermal expansion (CTE).

Still another objective of the present invention is to provide a structure of semiconductor device package and method of the same, which can provide a simple process for forming a semiconductor device package.

Yet another objective of the present invention is to provide a structure of semiconductor device package and method of the same, which can lower cost and higher yield rate.

Another objective of the present invention is to provide a structure of

semiconductor device package and method of the same, which can provide a good solution for low pin count device.

The present invention provides a structure of semiconductor device package comprising a substrate with a die receiving through hole, connecting through holes structure and first contact pads on an upper surface and second contact pads on a lower surface of the substrate; a die having bonding pads disposed within the die receiving through hole; a first adhesion material formed under the die; a second adhesion material filled in the gap between the die and sidewalls of the die receiving though hole of the substrate; a bonding wire formed to couple to the bonding pads and the first contact pads; and a dielectric layer formed on the bonding wire, the die and the substrate.

The present invention provides a method for forming a semiconductor device package comprising providing a substrate with a die receiving through hole, connecting through holes structure and first contact pads on an upper surface and second contact pads on a lower surface of the substrate; redistributing desired dice having bonding pads on a die redistribution tool with desired pitch by a pick and place fine alignment system; bonding the substrate to the die redistribution tool; filling a first adhesion material on the back side of the dice; filling a second adhesion material into the space between the dice edge and said dice receiving through hole of the substrate; separating the "panel " (panel form means substrate with die and adhesion together) from the die redistribution tool; forming a bonding wire to connect the bonding pads and the first contact pads; printing or molding or dispensing a dielectric layer on the active surface of the die and upper surface of the substrate; and mounting the package structure (in panel form) on a tape to saw into individual die for singulation.

The present invention provides a method for forming a semiconductor device package comprising providing a substrate with a die receiving through hole, connecting through hole structure and first contact pads on an upper surface and second contact pads on a lower surface of the substrate; bonding the substrate to a die redistribution tool; redistributing desired dice having bonding pads on the die redistribution tool with desired pitch into the die receiving through hole of the substrate by a pick and place fine alignment system; forming a bonding wire to connect the bonding pads and the first contact pads; forming a dielectric layer on the active surface of the die and upper surface of the substrate and the gap between the die and sidewall of the die receiving through hole; separating the "panel" (panel form means substrate with the die and the adhesion material – in here is dielectric layer) from the die redistribution tool; and mounting the package structure (in panel form) on a tape to saw into individual die for singulation.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, taken in conjunction with the accompanying drawings, wherein:

Fig. 1 illustrates is a cross-section diagram of a structure of semiconductor device package according to one embodiment of the present invention;

Fig. 2a illustrates is a cross-section diagram of a structure of semiconductor device package according to another embodiment of the present invention;

Fig. 2b illustrates is a cross-section diagram of a structure of semiconductor device package according to another embodiment of the present invention;

Fig. 3 illustrates is a cross-section diagram of a structure of semiconductor device package according to one embodiment of the present invention;

Fig. 4 illustrates a bottom view diagram of a structure of semiconductor device package according to the present invention;

Fig. 5a illustrates a top view diagram of a structure of semiconductor device package according to one embodiment of the present invention;

Fig. 5b illustrates a top view diagram of a structure of semiconductor device package according to another embodiment of the present invention;

Fig. 6a-6b illustrate cross-section diagrams of a method of forming a semiconductor device package according to one embodiment of the present invention; and

Fig. 7a-7f illustrate cross-section diagrams of a method of forming a semiconductor device package according to another embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description, numerous specific details are provided in order to give a through understanding of embodiments of the invention. Referring now to the following description wherein the description is for the purpose of illustrating the preferred embodiments of the present invention only, and not for the purpose of limiting the same. One skilled in the relevant art will recognize, however, that the invention may be practiced without one or more of the specific details, or with other methods, components, materials, etc.

Referring to Fig. 1, it is a cross-section diagram of a structure of semiconductor

device package 100 according to one embodiment of the present invention. The package 100 comprises a substrate 102, a die 104, a die receiving through hole 105, a first adhesion material 106, a second adhesion material 107, bonding pads 108, a metal or conductive layer 110, bonding wire 112, first contact pads 113, connecting through holes structure 114, second contact pads 115, a dielectric layer 118 and a plurality of conductive bumps 120.

In Fig. 1, the substrate 102 has a die receiving through hole 105 formed therein to receive a die 104. The die receiving through hole 105 is formed from the upper surface of the substrate 102 through the substrate 102 to the lower surface. The die receiving through hole 105 is pre-formed within the substrate 102. The second adhesion material 107 is also refilled within the space between the edge of die 104 and the sidewalls of the die receiving through holes 105. The first adhesion material 106 is coated under the lower surface of the die 104, thereby sealing the die 104. It maybe uses the same material for both the first adhesion material 106 and the second adhesion material 107.

The substrate 102 further comprises the connecting through holes structure 114 formed therein. The first contact pads 113 and the second contact pads 115 (for organic substrate) are respectively formed on the upper surface and lower surface of the connecting through holes structure 114 and partial part of the upper surface and lower surface of the substrate 102. The conductive material is re-filled into the connecting through holes structure 114 for electrical connection, it is preformed process once making the substrate.

Optional, a metal or conductive layer 110 is coated on the sidewall of the die

receiving through hole 105, that is to say, the metal layer 110 is formed between the die 104 surrounding by the second adhesion material 107 and the substrate 102. It can improve the adhesion strength between die edge and sidewall of the die receiving through hole 105 of the substrate 102 by using some particular adhesion materials, especially for the rubber type adhesion materials.

The die 104 is disposed within the die receiving through holes 105 on the substrate 102. As know, bonding pads 108 are formed within the upper surface of the die 104. A bonding wire 112 is formed to couple to the bonding pads 108 and the first contact pads 113. A dielectric layer 118 is formed to cover the bonding wire 112 and the upper surface of the die 104 and the substrate 102. Then, a plurality of conductive bumps 120 are formed and coupled to the second contact pads 115 by printing the solder paste on the surface, followed by performing re-flow process to reflow the solder paste. Accordingly, the bonding pads 108 formed within the die 104 can be electrically connected with the conductive bumps 120 by the connecting through holes structure 114.

The dielectric layer 118 is employed to prevent the package from external force that may causes damage to the package. The metal layer 110 and the second adhesion material 107 act as buffer areas that absorb the thermal mechanical stress between the die 104 and substrate 102 during temperature cycling due to the second adhesion material 107 has elastic property. The aforementioned structure constructs LGA type package.

In one embodiment, the material of the substrate 102 includes epoxy type FR5, FR4 or BT (Bismaleimide triazine epoxy). The material of the substrate 102 also can

be metal, alloy, glass, silicon, ceramic or print circuit board (PCB). The alloy further includes alloy 42 (42%Ni-58%Fe) or Kovar (29%Ni-17%Co-54%Fe). Further, the alloy metal is preferably composed by alloy 42 that is a nickel iron alloy whose coefficient of expansion makes it suitable for joining to silicon chips in miniature electronic circuits and consists of nickel 42% and ferrous (iron) 58%. The alloy metal also can be composed by Kovar which consists of nickel 29%, cobalt 17% and ferrous (iron) 54%.

Preferably, the material of the substrate 102 is organic substrate likes epoxy type FR5, BT, PCB with defined through holes or Cu metal with pre etching circuit. Preferably, the coefficient of thermal expansion (CTE) is the same as the one of the mother board (PCB), and then the present invention can provide a better reliability structure due to the CTE of the substrate 102 is matching with the CTE of the PCB (or mother board) accordingly. Preferably, the organic substrate with high Glass transition temperature (Tg) are epoxy type FR5 or BT (Bismaleimide triazine) type substrate. The Cu metal (CTE around 16) can be used also. The glass, ceramic, silicon can be used as the substrate. The second adhesion material 107 is formed of silicone rubber elastic materials.

In one embodiment, the material of the first adhesion material 106 and the second adhesion material 107 include ultraviolet (UV) curing type and/or thermal curing type material, epoxy or rubber type material. The first adhesion material 106 also can be included the metal material. Further, the material of the dielectric layer 118 includes liquid compound, resin, silicone rubber and also can be benzocyclobutene (BCB), Siloxane polymer (SINR) or polyimide (PI).

Referring to Fig. 2a, it is a cross-section diagram of a structure of semiconductor device package 200 according to another embodiment of the present invention. The substrate 202 comprises the connecting through holes structure 214 formed on four sides of the substrate 202, that is to say, the connecting through holes structure 214 is respectively formed on both lateral sides of the substrate 202 (maybe four end sides). The first contact pads 213 and the second contact pads 215 are respectively formed on the upper surface and lower surface of the connecting through holes structure 214 and partial part of the upper surface and lower surface of the substrate 202. The conductive material is re-filled into the connecting through holes structure 214 for electrical connection. Then, a plurality of conductive bumps 220 are coupled to the second contact pads 215. Accordingly, the bonding pads 208 formed within the die 204 can be electrically connected with the conductive bumps 220 by the connecting through holes structure 214.

Optionally, a metal or conductive layer 210 is coated on the sidewall of the die receiving through hole 205, namely, the metal layer 210 is formed between the die 204 surrounding by the second adhesion material 207 and the substrate 202.

Further, the various elements in the package 200 are similar to the elements in the package 100, as shown in Fig. 1 and 2, and therefore, the detailed description is omitted.

In Fig. 2b, illustrates is a cross-section diagram of a structure of semiconductor device package 200 according to the present invention. The first contact pads 213 are formed over the connecting through holes structure 214. The connecting through holes structure 214 is located in the scribe line 230. In other words, each package has

half through holes structure 214 after sawed. It can improve the solder join quality during SMT process and also can reduce the foot print. Similarly, the structure of half through holes structure 214 can be formed on the sidewall of the die receiving through hole 205 (does not show the drawing), it can replace the conductive layer 210.

Referring to Fig. 3, it is a cross-section diagram of a structure of semiconductor device package 100 according to the present invention. An alternative embodiment can be seen in Fig. 3, a package structure 100 can be formed without the conductive bumps 120 on the second terminal pads 115. The other parts are similar to Fig. 1, therefore, the detailed description is omitted.

Preferably, the thickness a between the substrate 102 and the second contact pads 115 is approximately 118-218 μm. The thickness b of the dielectric layer 118 is approximately 50-100 μm. Accordingly, the present invention can offer a super thin structure having a thickness less than 200 μm, and the package size is approximately around the die size plus 0.5 mm to 1 mm per side to form a chip scale package (CSP) by using the conventional process of print circuit board.

Referring to Fig. 4, it illustrates a bottom view diagram of a structure of semiconductor device package 100 according to the present invention. The back side of the package 100 includes the substrate 102 (the solder mask layer is not showed on the drawing) and the second adhesion layer 107 formed therein and surrounded by a plurality of second contact pads 115. The package 100 comprises the first adhesion material 106 that includes a metal sputtering and/or electro-plating on back side of the die 104 and the second adhesion material 107 to enhance the thermal conductivity, as shown in the dotted area. It can be solder join with printed circuit board (PCB) by

solder paste, it can exhaust the heat (generate by die) through the copper metal of print circuit board.

Referring to Fig. 5a, it illustrates a top view diagram of a structure of semiconductor device package 100 according to the present invention. The top side of package 100 includes the substrate 102, a die 104 having a plurality of bonding pads 108 and formed on the first adhesion material 106. A plurality of first contact pads 113 are formed surrounding around the edge areas of the substrate 102. Further, the package 100 further comprises a plurality of bonding wire 112 to couple the bonding pads 108 and the first contact pads 113. It is noted that the bonding wire 112 are invisible after the formation of the dielectric layer 118.

Otherwise, the package 100 also can be applied to higher pin counts. In Fig. 5b, it illustrates a top view diagram of a structure of semiconductor device package 100 according to the present invention. The other parts are similar to Fig. 5a, therefore, the detailed description is omitted. Accordingly, the peripheral type format of the present invention can provide a good solution for low pin count device.

It is noted that the structure 100 in Fig. 4, 5a and 5b also can be the package 200 according to the aspect of the present invention.

According to the aspect of the present invention, the present invention further provides a method for forming a semiconductor device package 100 with the die receiving through hole 105 and the connecting through holes structure 114. Refer to Fig. 6a-6b, they illustrate a cross-section diagrams of a method of forming a semiconductor device package 100. The steps are as follows and the following steps also can be referred to Fig. 7a-7f due to they are similar.

First, the substrate 102 with the die receiving through holes 105, connecting through holes structure 114 and the first contact pads 113 on an upper surface and the second contact pads 115 on a lower surface of the substrate 102 is provided, wherein the die receiving through holes 105 and the connecting through holes structure 114 and the first contact pads 113 and the second contact pads 115 are preformed within the substrate 102, as shown in Fig. 6a. The desired dice 104 having bonding pads 108 are redistributed on a die redistribution tool 300 with desired pitch by a pick and place fine alignment system, as shown in Fig. 6b. The substrate 102 is bonding to the die redistribution tool 300, that is to say, the active surface of the die 104 is sticking on the die redistribution tool 300 printed by patterned glues (not shown). After the second adhesion material 107 filled into the space between the die 104 and the first adhesion material 106 on back side of the die 104, the first and second adhesion material 106 and 107 are cured, in this application, it maybe the same materials for the first adhesion material 106 and the second adhesion material 107. Then, the package structure is separated from the die redistribution tool 300.

After cleaning the top surface of the bonding pads 108 and the first contact pads 113 (the pattern glues may residue on the surface of bonding pads 108 and first contact pads 113), the bonding wire 112 is formed to connect the bonding pads 108 to the first contact pads 113. The dielectric layer 118 is coated (or print or dispensing) and cured on the active surface of the die 104 and upper surface of the substrate 102 in order to protect the bonding wire 112, the die 104 and the substrate 102. Next, the terminal contact pads are formed on the second contact pads 115 by printing the solder paste (or ball). Then, the plurality of conductive bumps 120 are formed by an IR reflow method and coupled to the second contact pads 115. Subsequently, the package structure is mounting on a tape 302 to saw into individual die for singulation.

Optionally, a metal or conductive layer 110 is formed on the sidewall of die receiving through hole 105 of the substrate 102, and the metal is pre-formed during the manufacture of the substrate. A metal film (or layer) can be sputtered or plated on the back side of the die 104 as the first adhesion material 106 for better thermal management inquiry.

According to another aspect of the present invention, the present invention also provides another method for forming a semiconductor device package 200 with the die receiving through holes 205 and the connecting through holes structure 214. Refer to Fig. 7a-7f, they illustrate cross-section diagrams of a method of forming a semiconductor device package 200 according to the present invention

The steps of forming the package 200 comprises providing a substrate 202 with die receiving through holes 205, connecting through holes structure 215 and the first contact pads 213 on an upper surface and a second contact pads 215 on a lower surface of the substrate 202. The substrate 202 is bonding to a die redistribution tool 300, as shown in Fig. 7a. In other words, the active surface (for solder join) of the substrate 202 is sticking on the die redistribution tool 300 printed by patterned glues (not shown). The desired die 204 has bonding pads 208 and the first adhesion material 206 (optional) is formed on the back side of the die 204, as shown in Fig. 7b. The die 204 is redistributed on the die redistribution tool 300 with desired pitch by a pick and place fine alignment system. Then, the bonding wire 212 is formed to connect the bonding pads 208 to the first contact pads 213, as shown in Fig. 7c.

Next, the dielectric layer 218 is formed on the active surface of the die 204 and upper surface of the substrate 202 to fully cover the bonding wire 212 and fill into

the gap between die edge and sidewall of die receiving through hole 205 as second adhesion material 207, as shown in Fig. 7d, and the dielectric layer 218 is cured. After the package structure separated from the die redistribution tool 300, the back side of the substrate 202 and the first adhesion material 206 are cleaned, as shown in Fig. 7e.

Alternatively, the terminal contact pads are formed on the second contact pads 215 by printing the solder paste (or ball). Optionally, the plurality of conductive bumps 220 are formed and coupled to the second contact pads 215. Subsequently, the package structure 200 is mounted on a tape 302 to saw into individual die for die singulation.

In one embodiment, a conventional sawing blade 232, is used during the singulation process. The blade 232 is aligned to the scribe line 230 to separate the dice into individual die during the singulation process, as shown in Fig. 7f.

Optional, a metal or conductive layer 210 is formed on the sidewall of die receiving through hole 205 of the substrate 202, it is the pre-formed process during making the substrate 202. Another process is making the first adhesion material 206 by using the steps including seed metal sputtering, patterning, electro-plating (Cu), PR striping, metal wet etching process, etc. to achieve the first adhesion materials 206 as metal layer after.

In one embodiment, the step of forming the conductive bumps 120 and 220 are performed by an infrared (IR) reflow method.

It is noted that the material and the arrangement of the structure are illustrated to describe but not to limit the present invention. The material and the arrangement of

the structure can be modified according to the requirements of different conductions.

According to the aspect of the present invention, the present invention provides a structure of semiconductor device with the die receiving through hole and the connecting through holes structure, that provides a structure of super thin package which the thickness is less than 200 μm and the package size is slight large than the die size. Further, the present invention provides a good solution for low pin count device due to the peripheral type format. The present invention provides a simple method for forming a semiconductor device package which can improve the reliability and yield. Moreover, the present invention further provides a new structure that has a die receiving through hole and connecting through holes structure, and therefore can also minimize the size of chip scale package structure and lower costs due to the lower cost material and the simple process. Therefore, the super thin chip scale package structure and method of the same disclosed by the present invention can provide unexpected effect than prior art, and solve the problems of prior art. The method may apply to wafer or panel industry and also can be applied and modified to other related applications.

As will be understood by a person skilled in the art, the foregoing preferred embodiments of the present invention are illustrative of the present invention, rather than limiting the present invention. Having described the invention in connection with a preferred embodiment, modification will suggest itself to those skilled in the art. Thus, the invention is not to be limited by this embodiment. Rather, the invention is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. A structure of semiconductor device package, comprising:

a substrate with a die receiving through hole, connecting through holes structure and first contact pads on an upper surface and second contact pads on a lower surface of said substrate;

a die having bonding pads disposed within said die receiving through hole;

a first adhesion material formed under said die;

a second adhesion material filled in the gap between said die and sidewalls of said die receiving though hole of said substrate;

a bonding wire formed to couple to said bonding pads and said first contact pads; and

a dielectric layer formed on said bonding wire, said die and said substrate.

2. The structure in claim 1, further comprising a plurality of conductive bumps coupled to said second contact pads.

3. The structure in claim 2, wherein said plurality of conductive bumps can be electrically connected with said bonding pads through said through holes structure.

4. The structure in claim 1, further comprising a metal or conductive layer formed on side walls of said die receiving through hole of said substrate.

5. The structure in claim 1, wherein said connecting through holes structure is formed to pass through said substrate.

6. The structure in claim 1, wherein said connecting through holes structure is formed lateral side of said substrate.

7. The structure in claim 1, wherein material of said substrate includes epoxy type FR5, FR4 or BT (Bismaleimide triazine).

8. The structure in claim 1, wherein material of said substrate includes metal, alloy, glass, silicon, ceramic or print circuit board (PCB).

9. The structure in claim 8, wherein said alloy includes alloy 42 (42%Ni-58%Fe) or Kovar (29%Ni-17%Co-54%Fe).

10. The structure in claim 1, wherein material of said first adhesion material and second adhesion material include UV curing type and/or thermal curing type material, epoxy or rubber type material.

11. The structure in claim 1, wherein said connecting through holes structure are filled by a conductive material.

12. The structure in claim 1, wherein material of said dielectric layer include liquid compound, resin and silicone rubber.

13. The structure in claim 1, wherein material of said dielectric layer include benzocyclobutene (BCB), Siloxane polymer (SINR) or polyimide (PI).

14. The structure in claim 1, wherein material of said first adhesion material include a metal sputtering and/or electro-plating on back side of said die.

15. A method for forming a semiconductor device package, comprising:

providing a substrate with a die receiving through hole, connecting through holes structure and first contact pads on an upper surface and second contact pads on a lower surface of said substrate;

redistributing desired dice having bonding pads on a die redistribution tool with desired pitch by a pick and place fine alignment system;

bonding said substrate to said die redistribution tool;

filling a first adhesion material on the back side of said dice;

filling a second adhesion material into the space between said dice edge and said dice receiving through hole of said substrate;

separating said package structure from said die redistribution tool;

forming a bonding wire to connect said bonding pads and said first contact pads;

printing a dielectric layer on the active surface of said die and upper surface of said substrate; and

mounting said package structure on a tape to saw into individual die for singulation.

16. The method in claim 15, further comprising a step of welding a plurality of soldering bumps on said terminal pads.

17. The method in claim 16, wherein said step of forming said soldering bumps is performed by an infrared (IR) reflow method.

18. The method in claim 16, wherein said step of forming said conductive bumps on said second contact pad is performed by solder paste.

19. The method in claim 15, further comprising a step of sticking active surface of said die on said die redistribution tool printed by patterned glues.

20. The method in claim 15, further comprising a step of curing said first and second adhesion material.

21. The method in claim 15, further comprising a step of curing said dielectric layer.

22. The method in claim 15, further comprising a step of forming a metal or conductive layer on the sidewall of said die receiving through hole of said substrate.

23. The method in claim 15, further comprising a step of cleaning top surface of said package before forming said bonding wire.

24. A method for forming a semiconductor device package, comprising:

providing a substrate with a die receiving through hole, connecting through holes structure and first contact pads on an upper surface and second contact pads on a lower surface of said substrate;

bonding said substrate to a die redistribution tool;

redistributing desired dice having bonding pads on said die redistribution tool with desired pitch by a pick and place fine alignment system;

forming a bonding wire to connect said bonding pads and said first contact pads;

forming a dielectric layer on the active surface of said die and upper surface of said substrate and fill into the gap between dice edge and sidewall of said die receiving through hole of said substrate;

separating said package structure from said die redistribution tool; and

mounting said package structure on a tape to saw into individual die for singulation.

25. The method in claim 24, further comprising a step of welding a plurality of conductive bumps on said second contact pad.

26. The method in claim 25, wherein said step of forming said conductive bumps is performed by an infrared (IR) reflow method.

27. The method in claim 25, wherein said step of forming said conductive bumps on said second contact pad is performed by solder paste.

28. The method in claim 24, further comprising a step of sticking backside surface of said die on said die redistribution tool printed by patterned glues.

29. The method in claim 24, further comprising a step of curing said dielectric layer.

30. The method in claim 24, further comprising a step of forming a first adhesion material on the back side of said dice.

31. The method in claim 24, further comprising a step of forming a metal layer on the sidewall of said die receiving through holes of said substrate.