applied to T/R circuit 165_i-j to control the switching states of T/R switches 70, 72, and may also dynamically control phase shifts of phase shifters 62, 82. During a transmit interval, T/R switches 70 and 72 are switched to first switch positions to route a transmit signal incident from combiner / divider network 180 through phase shifter 82 and amplifier 80 to antenna 120_i-j. During a receive interval, T/R switches 70 and 72 are switched to second switch positions to route an RF receive signal from antenna 120_i-j through amplifier 60 and phase shifter 62 to combiner / divider network 180. The same frequency band, or different frequency bands, may be used for transmit and receive operations.

[0027] T/R circuit 165_i-j of FIG. 3B is but one example of a T/R circuit that routes transmit and receive signals between shared antenna elements 120 (shared for handling both transmit and receive signals) and a shared combiner / divider network 180. Other configurations known to those of skill in the art may be substituted. For instance, an alternative T/R circuit may omit the T/R switches 70, 72 and utilize different frequency bands for transmit and receive operations, respectively, with a suitable isolation mechanism for preventing transmit signal power from damaging the receive amplifier 60. It may also be possible to omit T/R switches 70, 72 by implementing a polarization diversity scheme (e.g., left hand circular on transmit, right hand circular on receive, or vice versa).

[0028] Returning to FIG. 2B, a cross-sectional view illustrating an example arrangement and connection technique between any antenna element 120 and an IC chip 160 of the antenna apparatus 100 is illustrated. IC chip 160 is embedded within embedded structure 154 and may have a signal line contact 162s and a pair of ground contacts 162g at or near a top surface S1 of embedded structure 154 for routing an RF signal. Conductive vias Vs, Vg formed within interconnect layer 155 each have a respective end connected to contacts 162s, 162g and an opposite end having respective contact pads Ps, Pg. In an assembly stage, antenna subassembly 110 may be attached to subassembly 150 by adhering a lower surface of ground plane 119 to a top surface S2 of interconnect layer 155. Such attachment may be realized with an electrical bonding material, e.g., solder, between respective pads on subassemblies 110, 150, and optionally supplemented using an adhesive on other surface regions of subassemblies 110, 150. During this assembly stage, pad Ps may be soldered to the microstrip probe feed 114 through a solder ball (or bump / pillar) 147s melted and then cooled during the adhering process. Likewise, the pair of pads Pg may be soldered to ground plane 119 through a respective pair of solder balls 147g, thereby forming a ground-signal-ground (GSG) connection between feed 114 / ground plane 119 and the signal / ground points of IC chip 160. The solder balls

147s, 147g may have been initially adhered to the antenna feed / ground plane 114 / 119 as illustrated in FIG. 2B, or alternatively to the pads Ps, Pg.

[0029] In the shown embodiment, with the IC chip 160 directly underlying antenna element 120, the vias Vs, Vg form desirable short connections between IC chip 160 and the antenna element 120 contact points. In other embodiments where an IC chip 160 does not directly underlay an antenna element 120, the GSG connection may be made to points of a coplanar waveguide (CPW) transmission line within interconnect layer 155. Such a CPW transmission line may have an inner trace extending to pad Ps and a pair of ground traces (one on each side of the inner trace) respectively extending to the pair of pads Pg.

[0030] FIG. 4 is a cross-sectional view of a portion of antenna apparatus 100 taken along the path IV-IV' of FIG. 1. In this example cross section, embedded component subassembly 150 includes an IC chip 160, a transmission line section 180, a coaxial line ("coax") feed-through 170, and a DC via 190. IC chip 160 may be connected to one or more antenna elements 120 of subassembly 110 in the manner described above for FIG. 2B. An insulating adhesive layer 130 may be formed between the subassemblies 110, 150 following the above-discussed adhesion stage. Adhesive layer 130 is present if an adhesive is applied to supplement electromechanical attachment of subassemblies 110, 150 using the GSG solder connections; otherwise, adhesive layer 130 may be omitted. In the shown example, the one or more RDL layers 155 comprise a lower RDL layer 155a and an upper RDL layer 155b, where upper RDL layer 155b separates conductive traces such as 198, 168, and 188 and the adhesive layer 130 / ground plane 119. In an alternative design, upper RDL layer 155b is omitted, such that only the adhesive layer 130 separates the ground plane 119 and the conductive traces atop the RDL layer 155a.

[0031] IC chip 160, transmission line section 180, and coax feed-through 170 are each an example of a beamforming network component that was embedded within molding material ("encapsulant") 152, and each may have an upper surface substantially coplanar with an upper surface s1 of encapsulant 152. RDL layer connections between these elements may be made through respective vias V1 extending from surface s1 to an upper surface s4 of RDL layer 155a. Any via such as V1, Vg or 190 may have a barrel (e.g. barrel 191 of via 190) extending through the surrounding dielectric material, and a pair of pads, e.g., P1, P3, Pg, Ps on opposite ends. For instance, IC chip 160 may have contact 162f connected to a via V1, which in turn connects to conductive trace 198, another via V1 and DC via 190. DC via 190 may extend to a lower surface s3 of encapsulant 152, where its opposite end has a lower pad P3. Conductive traces 198, 168, 188 patterned along surface s4 may interconnect beamforming components through connection to the via pads. Any via pad

formed atop surface s1 of encapsulant 152 may be formed prior to applying a layer of dielectric to form RDL layer 155a. After the RDL layer 155a dielectric is applied, the opposite pad of the via may be formed, and thereafter a via hole may be drilled through the top pad and extending through to the lower pad. The via hole may then be filled with a conductor, e.g., electroplated, to complete the via formation.

[0032] Coplanar waveguide (CPW) connections may also be made between various components through RDL layers155 to form interconnects to route RF signals. For example, transmission line section 180 may include conductive traces such as inner CPW trace 182 extending along a top surface of a low loss dielectric material 185 such as quartz or fused silica. Dielectric material 185 is desirably a material having a lower loss tangent than that of encapsulant 152. Outer CPW traces, not shown in FIG. 4, discussed later as traces 184a, 184b of FIG. 5, may extend parallel to inner trace 182 on opposite sides thereof. (In the cross-sectional view of FIG. 4, one CPW outer trace may be in front of inner trace 182 while the other outer trace is behind inner trace 182.) One end of inner trace 182 may connect to a signal contact 162t of IC chip 160 through an interconnect formed by RDL trace 168 between a pair of vias V1. Likewise, a pair of outer RDL traces (not shown) may connect the outer CPW traces of transmission line section 180 to a pair of ground contacts of IC chip 160 (not shown in FIG. 4 but exemplified as contacts 162g in FIG. 5) on opposite sides of signal contact 162t.

[0033] Coaxial line 170 is comprised of a dielectric 176 such as glass separating an inner conductor 172 and an outer cylindrical conductor 174. Coaxial line 170 may extend vertically from surface s1 to lower surface s3 of encapsulant 152. Inner conductor 172 may connect to another end of inner CPW trace 182 through an interconnect comprising RDL trace 188 between a pair of vias V1. Outer conductor 174 may connect at two points to outer traces on opposite sides of inner trace 182. For instance, a via V2 may be formed behind inner CPW RDL trace 188 in the cross-sectional view of FIG. 4. This via V2 may electrically connect a point of outer conductor 174 to one of the RDL outer CPW traces located behind inner CPW RDL trace 188. Coax feed-through 170 and DC via 190 may each connect to a surface mount connector (not shown) at surface s3. One or more additional IC chips may be mounted to surface s3 and connected to IC chips 160 through additional vias as desired. One example of such an additional IC chip is a voltage regulator chip providing voltage to IC chip 160. Another example is a microprocessor chip that provides control signals to beamforming circuitry such as phase shifters and/or T/R switches within IC chip 160.