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(54) A COLOR TELEVISION RECEIVER ARRANGEMENT

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

In the usual Standard PAL Decoder the chroma signal (that is, the modulated subcarrier signal) is delayed by 63.943 microseconds and is then added to and subtracted from the direct signal to yield the U and V chroma signals. A disadvantage of this method of comb filtering is that the delay time must be correct within some ± 3 nanoseconds; otherwise, in the synchronous detection process, any delay error produces a phase error in the detected delayed signal only which gives rise to an amplitude difference from line to line, leading to a line crawl or "Hanover bar" effect which is most undesirable. This effect can occur even when there are no other (system) phase errors, and it is a source of concern, since typical ultrasonic delay lines have been known to exhibit a long term (1 year or so) delay time drift of up to ± 50 nanoseconds; i.e., more than ten times the allowable tolerance.

Now the required ± 3 nanosecond tolerance arises because the comb filter signals consist of modulated subcarrier signals which are added and subtracted, and naturally any delay error appears as a phase error. However, basically the delay error is really limited only by image registration requirements of the order of 100 nanoseconds and therefore the stringent ± 3 nanosecond delay tolerance can be avoided by operating the comb filter in the post-demodulator (that is, demodulated subcarrier) domain rather than in the pre-demodulator (modulated subcarrier) domain. Since a pre-demodulator comb filter accepts a mixture of modulated U and V chroma signals and separates them, it may be thought that an equivalent post-demodulator comb

filter could accept a mixture of demodulated U and V signals, such as would be obtained by adding the U and V outputs of a Simple PAL decoder (without V switching), and separate those. However, while this is true, it will be found that, if there is a system phase error ϕ , the resulting comb filtered U output will be $U (\cos \phi - \sin \phi)$, while the V output will be $V (\cos \phi + \sin \phi)$. Thus, U and V are multiplied by different factors so that a system phase error produces a hue shift. This effect is fundamental and is due to the fact that a system phase error shifts both the U and V detection axes in the same direction. Therefore, for post-demodulator comb filtering, a separate filter is required for the U and V channels.

A post-demodulator comb filtering arrangement which would normally employ ultrasonic delay lines according to present-day techniques is shown in Fig. 1. Because presently available ultrasonic delay lines operate at the subcarrier frequency, it is necessary to re-modulate U and V on to some carrier, which, for convenience, can be the subcarrier frequency itself. After the outputs have been amplitude detected, the DC components can be restored by clamping at the horizontal rate. To reduce distortion the amplitude modulation by the U and V signals can be kept low, say 50%.

It can be seen that neither the U nor the V comb filters use the critical physical addition channel. The direct and delayed signals are literally averaged, so that for equal amplitude of the direct and delayed signals Hanover bars are impossible. System phase errors will reduce saturation, but there will be no hue change and no Hanover bars. If either comb filter has an incorrect delay, this will reduce the saturation, but no Hanover bars will result. Thus, suppose one channel has a delay error which is such that its direct and delayed signals are, say, 90° apart, then the output will be reduced by 3 dB because the addition is vectorial rather than algebraic, but no Hanover bars will appear. Even if one considers the highest

possible color-difference frequency of about 100 f_H (1.5 MHz), 100 cycles occur in 64 microseconds, so each cycle has a period of 640 nanoseconds, so that a 90° shift would occur for an error of 160 nanoseconds. Basically, because of the lower frequencies involved in the color-difference signal domain, the delay tolerance is limited only by registration requirements of the order of 100 nanoseconds.

The post-demodulator comb filters have the usual comb filter response of half ("rectified") sinewaves so that, like the pre-demodulator filter, a 3 dB improvement in cross color and chrominance s/N ratio are obtained.

As shown in Figure 1, the post-demodulator filter has the disadvantage that re-modulation of U and V is necessary in order to achieve the one line delay if presently available ultrasonic lines are used. However, we find that substitution of an integrated circuit (IC) shift register for the ultrasonic line provides an elegant and economic solution in which, if desired, no re-modulation is necessary.

According to the present invention, therefore, there is provided in a PAL color television receiver arrangement adapted to separate modulated subcarrier signals from a transmitted PAL color television signal and having a local oscillator operating at the subcarrier frequency, demodulator means responsive to said modulated subcarrier signals and to the output of said oscillator for producing separate U and V demodulated signals, first signal processing means responsive to said U demodulated signals and second signal processing means responsive to said V demodulated signals, each of said signal processing means including a first signal path incorporating time delay means, a second signal path bypassing said time delay means and averaging means coupled to the outputs of said first and second signal paths for producing a signal which is the average of the signals following said two signal paths, wherein the time delay means arranged in said first signal path of each of said signal processing means includes a plurality of cascaded stages, each stage adapted to hold signal information and transfer such information to the next succeeding stage, and control means synchronized by said local oscillator for transferring information from one stage to the next.

In the remaining drawings, Figures 2-7 show such shift registers for use as PAL delay lines and Figures 8 and 9 show receiver arrangements capitalizing on the advantages of the use of such delay lines.

Figure 2 shows a simplified model for such a shift register type delay line. Each stage of the delay line consists of two half-stages, and each half-stage is composed of a sampling switch, a holding capacitor and an amplifier. The voltage amplifiers are assumed to have

infinite input impedance and unity gain (either negative or positive). The switches are electrically controlled and operate so that all odd-numbered switches (i.e., $S_1, S_3, S_5, \dots$) are closed when all even-numbered switches (i.e., $S_2, S_4, S_6, \dots$) are opened, and vice versa.

Information is introduced into the first half-stage by means of switch S_1 . When S_1 opens, the information is sampled and held by capacitor C_1 . The stored information appears at the output of amplifier A_1 and is introduced into the second half-stage by means of switch S_2 , which is closed when S_1 is open.

When switch S_2 opens, the information is stored on capacitor C_2 and appears at the output of amplifier A_2 . The original input information is thus delayed over a period determined by the sequential closing and opening of switches S_1 and S_2 . Larger delays are produced by use of more than one stage, as shown. The information proceeds from stage to stage in a manner analogous to a "bucket brigade" capacitors.

The total delay depends on the number of stages used and the frequency at which the switches operate; i.e., $T_D = n/f_s$, where T_D is the total delay, n is the total number of stages, and f_s is the sampling frequency. It is important to realize that the delayed signal is a sampled signal. It is necessary, therefore, that a sufficient number of samples be obtained to reconstruct the original but delayed signal. The sampling theorem states that a band-limited signal of maximum frequency f_m can be reconstructed if the sampling rate f_s is at least twice the maximum frequency of the signal; i.e., $f_s > 2f_m$.

With the one-line delay provided subsequent to demodulation, the highest frequency to be delayed may be about 1.0 MHz. A sub-multiple, one-half for example, of the color subcarrier may be used for the clock frequency.

Because the delay time of the Figure 2 delay arrangement is not affected by physical characteristics of the devices, maintenance of correct delay time as a function of temperature, aging, etc., is not a problem. The only requirement for a stable and accurate delay time is a stable and accurate clock frequency which can be provided by the sub-multiple of the color subcarrier frequency.

Even if the transmitted color subcarrier frequency is for any reason not accurately maintained, the horizontal line frequency will change with the color subcarrier frequency since in color TV systems of the NTSC or PAL type, the horizontal line frequency is determined by counting down from the color subcarrier frequency. Thus the one line delay required is always accurately maintained even if the transmitted color subcarrier frequency shifts far outside of the prescribed limits.

An advantageous circuit form for IC realization of each Figure 2 stage is shown in Figure 3. This is an all P channel MOS field effect transistor circuit. P_1 and P_2 act in place of the switches, S_1 and S_2 , of Figure 2, and are controlled at their respective gates. P_3 and P_4 form an MOS/MOS-load amplifier, serving as the amplifier A_1 of Figure 2. P_5 and P_6 form a similar amplifier to provide the function of the amplifier A_2 of Figure 2. The input capacitances of the gates P_3 and P_5 respectively function as the capacitors C_1 and C_2 of Figure 2. The gain of -1 for the amplifiers can be achieved by making the geometrical size of P_3 equal to that of P_4 , and that of P_5 equal to that of P_6 . The design gives an output DC voltage equal to the input DC voltage at each amplifier stage.

The transfer signal is shown in a first form in Figure 3, where the "A" signal is the inverted "B" signal, so that P_1 and P_2 are in opposite state, i.e., on or off. An alternative form is a pulse form where the A pulses fall in between the B pulses. The latter case degenerates to the former when the pulses are widened to their limits set by not permitting overlap. In addition, one could even use sine waves to operate as the transfer signal.

Figure 4 shows a modified form of the Figure 3 circuit, with P_1 now changed to N_1 , an N channel MOS transistor. This allows the successive switch gates to be connected together, and only one transfer signal is required.

Figure 5 shows a modification of the Figure 4 circuit where N_3 and N_4 form an MOS/MOS-load amplifier of N channel MOS type, responding to switch N_1 . In this circuit arrangement, each stage incorporates three N units and three P-units, giving an equal amount of each type.

In the circuits of Figures 3 to 5 each switch is constituted by a single MOS unit. In these circuits, undesirably, the transfer signal can be capacity coupled into the path of the delayed signal (as by the capacitance from gate of P_1 to gate of P_3 , for example, which is equivalent to the gate-to-drain capacitance of the P_1 MOS unit). This transfer signal can be electronically filtered from the delayed signal, but will add to the requirements of relative attenuation of pass band to stop band of the output filter (LPF, Figure 2).

Figure 6 illustrates a modification of the Figure 3 circuit, which alleviates the transfer signal coupling problem. Here, each switch includes a P channel MOS unit and an N channel MOS unit (with source-drain paths directly in shunt with each other). By equalizing the gate-drain capacitances for each pair (i.e., by designing for $C_{D1}=C_{D2}$ and $C_{D3}=C_{D4}$), the transfer signal will be balanced. Thus there would be little or no

coupling of the transfer signal into the delayed signal.

An alternative method of alleviating the transfer signal coupling problem is illustrated in Figure 7, which represents a modification of the all P-channel device circuit of Figure 3. Added to the Figure 3 circuit configuration in Figure 7 is a capacitor C_{B1} , which couples the transfer signal waveform B to the drain electrode of the first switch transistor P_1 . Also added is a capacitor C_{B2} , which couples the transfer signal waveform A to the drain electrode of the second switch transistor P_2 . By proportioning the capacitive value of the added capacitors to equal the gate-to-drain capacitors of the switching transistors (i.e., by making $C_{B1}=C_{GD1}$ and $C_{B2}=C_{GD2}$), the undesired transfer signal coupling may be balanced out.

Figure 8 illustrates the manner in which the received arrangement of Figure 1 is simplified when IC shift register delay lines of the type discussed in connection with Figures 2 through 7 are substituted for delay lines of the ultrasonic type. The delayed and undelayed U and V signals are again averaged. It will be noted that the amplitude modulator, amplitude detector and clamp functions may be eliminated, while a frequency divider function is added. Of course the delay line of Figures 2—7 could be used for either or both delay lines in Figure 1 also.

A further receiver simplification, rendered feasible by use of the IC shift register approach to the delay function, is illustrated in Figure 9. Structures for performing the frequency divider and direct/delayed signal combining functions associated with each delay line may readily be incorporated on the same monolithic circuit chip with the delay line. Also, the respective demodulator functions performed in the simple PAL decoder of Figures 1 and 8 may also be performed by structures incorporated in the respective delay line chips.

It may be noted that for 141.75 stages, the delay provided by structures of the type discussed in connection with Figures 2 through 7 is equal to that of Standard PAL 63.943 microseconds. By adding an extra 57 nanoseconds delay to each delay line output, a delay of exactly 64 microseconds can be obtained, which would ensure exact coincidence of the comb filter rejection points with all of the luminance signal sidebands. With a full 64 microsecond delay, the increase in transient rise time associated with the Standard PAL use of a 63.943 microsecond delay may be avoided. While effective realization of 3/4 of the stage may be difficult to achieve, provision of a half stage is readily achieved, as per the discussion of Figure 2. Accordingly, provision of 141.5 stages (providing a delay of 63,830 microseconds) may readily be effected for each shift register, with

a subsequent delay of 170 nanoseconds completing the full 64 microsecond delay. In either case, the added delay should be taken into account when computing the delay required in the receiver's luminance channel.

WHAT WE CLAIM IS:—

1. In a PAL color television receiver arrangement adapted to separate modulated subcarrier signals from a transmitted PAL color television signal and having a local oscillator operating at the subcarrier frequency, demodulator means responsive to said modulated subcarrier signals and to the output of said oscillator for producing separate U and V demodulated signals, first signal processing means responsive to said U demodulated signals and second signal processing means responsive to said V demodulated signals, each of said signal processing means including a first signal path incorporating time delay means, a second signal path bypassing said time delay means and averaging means coupled to the outputs of said first and second signal paths for producing a signal which is the average of the signals following said two signal paths, wherein the time delay means arranged in said first signal path of each of said signal processing means includes a plurality of cascaded stages, each stage adapted to hold signal information and transfer such information to the next succeeding stage, and control means synchronized by said local oscillator for transferring information from one stage to the next.

2. Apparatus as claimed in Claim 1 wherein each stage of said plurality of stages includes at least a sampling switch, a holding capacitor, and an amplifier and operation of said sampling switch produces said transfer of information, said control means controlling the operation of said sampling switches at a sub-multiple of said subcarrier frequency.

3. Apparatus as claimed in Claim 1 or 2 wherein each of said stages in said time delay means has an input terminal and an output terminal, and further includes a first MOS transistor amplifier having an input electrode at which storage capacitance is exhibited, a common electrode and an output electrode, a first MOS switching transistor having gate, source and drain electrodes, the source-drain path of said first MOS switching transistor being disposed serially between said delay stage input terminal and said input electrode of said first MOS transistor amplifier, a second MOS transistor amplifier having an input electrode at which storage capacitance is exhibited, a common electrode and an output electrode, a second MOS switching transistor having gate, source and drain electrodes, the source-drain path of said second MOS switching transistor being disposed serially between the output electrode

of said first MOS transistor amplifier and the input electrode of said second MOS transistor amplifier, means coupling said output electrode of said second transistor amplifier to said delay stage output terminal, said control means are coupled to the gate electrodes of said first and second MOS switching transistors for alternately rendering said first and second MOS switching transistors conducting.

4. Apparatus in accordance with Claim 3 wherein said first and second switching transistors are of opposite channel conductivity type, and said control means including means for applying coinciding phases of a switching waveform to the respective gate electrodes of said first and second switching transistors.

5. Apparatus in accordance with Claim 3 wherein said first and second switching transistors are of the same channel conductivity type, and said control means includes means for applying mutually opposing phases of a switching waveform to the respective gate electrodes of said first and second switching transistors.

6. Apparatus in accordance with Claim 5 wherein third and fourth switching transistors are provided, each having gate, source and drain electrodes but differing in channel conductivity type from said first and second switching transistors, wherein said third switching transistor has its source-drain path shunted across the source-drain path of said first switching transistor and its gate electrode connected to the gate electrode of said second switching transistor, and wherein said fourth switching transistor has its source-drain path shunted across the source-drain path of said second switching transistor and its gate electrode connected to the gate electrode of said first switching transistor.

7. Apparatus in accordance with Claim 5 wherein a first capacitor is coupled between the gate electrode of said second switching transistor and the input electrode of said first transistor amplifier, and a second capacitor is coupled between the gate electrode of said first switching transistor and the input electrode of said second transistor amplifier.

8. Apparatus in accordance with Claim 7 wherein said first and second capacitors substantially correspond in capacitance value to the respective gate-to-drain capacitances exhibited by said first and second switching transistors.

9. Apparatus in accordance with Claims 3, 4 or 5 wherein each of said transistor amplifiers includes, as a load impedance disposed on said common substrate, an MOS transistor having a source electrode connected to the respective amplifier output electrode, and gate and drain electrodes directly connected to each other.

10. Apparatus as claimed in any one of the



a subsequent delay of 170 nanoseconds completing the full 64 microsecond delay. In either case, the added delay should be taken into account when computing the delay required in the receiver's luminance channel.

WHAT WE CLAIM IS:—

1. In a PAL color television receiver arrangement adapted to separate modulated subcarrier signals from a transmitted PAL color television signal and having a local oscillator operating at the subcarrier frequency, demodulator means responsive to said modulated subcarrier signals and to the output of said oscillator for producing separate U and V demodulated signals, first signal processing means responsive to said U demodulated signals and second signal processing means responsive to said V demodulated signals, each of said signal processing means including a first signal path incorporating time delay means, a second signal path bypassing said time delay means and averaging means coupled to the outputs of said first and second signal paths for producing a signal which is the average of the signals following said two signal paths, wherein the time delay means arranged in said first signal path of each of said signal processing means includes a plurality of cascaded stages, each stage adapted to hold signal information and transfer such information to the next succeeding stage, and control means synchronized by said local oscillator for transferring information from one stage to the next.

2. Apparatus as claimed in Claim 1 wherein each stage of said plurality of stages includes at least a sampling switch, a holding capacitor, and an amplifier and operation of said sampling switch produces said transfer of information, said control means controlling the operation of said sampling switches at a sub-multiple of said subcarrier frequency.

3. Apparatus as claimed in Claim 1 or 2 wherein each of said stages in said time delay means has an input terminal and an output terminal, and further includes a first MOS transistor amplifier having an input electrode at which storage capacitance is exhibited, a common electrode and an output electrode, a first MOS switching transistor having gate, source and drain electrodes, the source-drain path of said first MOS switching transistor being disposed serially between said delay stage input terminal and said input electrode of said first MOS transistor amplifier, a second MOS transistor amplifier having an input electrode at which storage capacitance is exhibited, a common electrode and an output electrode, a second MOS switching transistor having gate, source and drain electrodes, the source-drain path of said second MOS switching transistor being disposed serially between the output electrode

of said first MOS transistor amplifier and the input electrode of said second MOS transistor amplifier, means coupling said output electrode of said second transistor amplifier to said delay stage output terminal, said control means are coupled to the gate electrodes of said first and second MOS switching transistors for alternately rendering said first and second MOS switching transistors conducting.

4. Apparatus in accordance with Claim 3 wherein said first and second switching transistors are of opposite channel conductivity type, and said control means including means for applying coinciding phases of a switching waveform to the respective gate electrodes of said first and second switching transistors.

5. Apparatus in accordance with Claim 3 wherein said first and second switching transistors are of the same channel conductivity type, and said control means includes means for applying mutually opposing phases of a switching waveform to the respective gate electrodes of said first and second switching transistors.

6. Apparatus in accordance with Claim 5 wherein third and fourth switching transistors are provided, each having gate, source and drain electrodes but differing in channel conductivity type from said first and second switching transistors, wherein said third switching transistor has its source-drain path shunted across the source-drain path of said first switching transistor and its gate electrode connected to the gate electrode of said second switching transistor, and wherein said fourth switching transistor has its source-drain path shunted across the source-drain path of said second switching transistor and its gate electrode connected to the gate electrode of said first switching transistor.

7. Apparatus in accordance with Claim 5 wherein a first capacitor is coupled between the gate electrode of said second switching transistor and the input electrode of said first transistor amplifier, and a second capacitor is coupled between the gate electrode of said first switching transistor and the input electrode of said second transistor amplifier.

8. Apparatus in accordance with Claim 7 wherein said first and second capacitors substantially correspond in capacitance value to the respective gate-to-drain capacitances exhibited by said first and second switching transistors.

9. Apparatus in accordance with Claims 3, 4 or 5 wherein each of said transistor amplifiers includes, as a load impedance disposed on said common substrate, an MOS transistor having a source electrode connected to the respective amplifier output electrode, and gate and drain electrodes directly connected to each other.

10. Apparatus as claimed in any one of the



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preceding claims, wherein said time delay means is arranged as an integrated circuit with all the stages thereof arranged on a common substrate.

- 5 11. Apparatus as claimed in any one of the preceding claims wherein said first and second signal processing means are arranged as integrated circuits with each of the elements thereof arranged on a common substrate.
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12. Apparatus as claimed in any one of the preceding claims wherein said demodulator means and said signal processing means

are arranged in integrated circuit form on a common substrate.

13. Apparatus according to claim 1 with said time delay means substantially as described in conjunction with any of Figs. 2—7 of the accompanying drawings.

14. Apparatus substantially as described in conjunction with Figure 8 or Figure 9.

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