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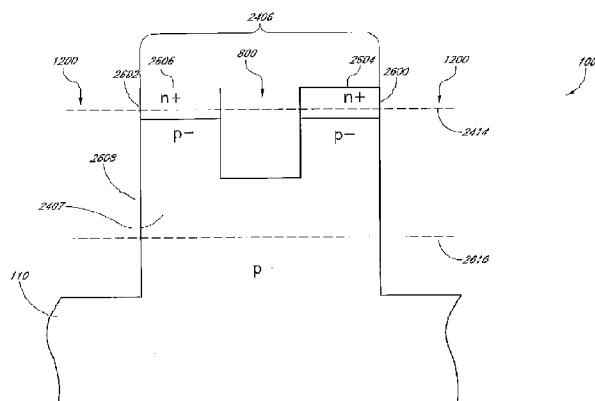
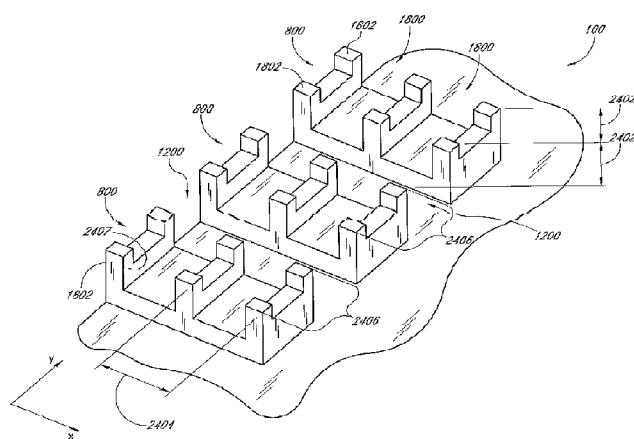
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(54) Title: DRAM CELLS WITH VERTICAL U-SHAPED TRANSISTORS



(57) Abstract: The invention includes a semiconductor structure (100) having U-shaped transistors (2406) formed by etching a semiconductor substrate (110). In an embodiment, the source/drain regions of the transistors are provided at the tops of pairs of pillars defined by crossing trenches in the substrate (110). One pillar is connected to the other pillar in the pair by a ridge (2407) that extends above the surrounding trenches. The ridge and lower portions of the pillars define U-shaped channels on opposite sides of the U-shaped structure, facing a gate structure in the trenches on those opposite sides, forming a two sided surround transistor. Optionally, the space between the pillars of a pair is also filled with gate electrode material to define a three-sided surround gate transistor. One of the source/drain regions of each pair extends to a digit line (2914) and the other extends to a memory storage device, such as a capacitor (2910). The invention also includes methods of forming semiconductor structures.



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