CLAIMS

What is claimed is:

1. A surface-mount structure comprising:

a sub-module, the sub-module comprising:

a dielectric layer;

an adhesive layer directly attached to the dielectric layer;

at least one semiconductor device adhered to the dielectric layer via the adhesive layer, with each of the at least one semiconductor device including a substrate composed of a semiconductor material;

a first level metal interconnect structure electrically coupled to the at least one semiconductor device, the metal interconnect structure extending through vias formed through the dielectric layer so as to be connected to the at least one semiconductor device; and

a second level input/output (I/O) connection electrically coupled to the first level metal interconnect structure and formed on the dielectric layer on a side opposite the at least one semiconductor device, the second level I/O connection configured to connect the sub-module to an external circuit;

a multi-layer substrate structure having a first surface and a second surface, wherein the at least one semiconductor device of the sub-module is attached to the first surface of the multi-layer substrate;

a dielectric material positioned between the dielectric layer and the first surface of the multi-layer substrate structure and at least partially about the at least one semiconductor device of the sub-module; and

a diffusion barrier layer applied over the sub-module, adjacent to the first level metal interconnect structure and the second level I/O connection, and extending down to the multi-layer substrate structure, the diffusion barrier layer configured to reduce the ingress of moisture and gases from a surrounding environment into the surface-mount structure.

2. The surface-mount structure of claim 1 wherein the diffusion barrier layer comprises organic materials, inorganic materials, ceramic materials, and any combination thereof.

3. The surface-mount structure of claim 2 wherein the inorganic material or ceramic comprises oxides, nitrides, carbides, and borides of elements of Groups IIA, IIIA, IVA, VA, VIA, VIIA, IB, IIB, metals of Groups IIIB, IVB, VB, rare earth elements, and any combination thereof.

4. The surface-mount structure of claim 1 wherein the diffusion barrier layer comprises a single layer barrier.

5. The surface-mount structure of claim 1 further comprising a solder mask applied over the first level metal interconnect structure; and

wherein the second level I/O connection comprises one of land grid array (LGA) solder bumps and ball grid array (BGA) solder bumps configured to pass through the solder mask at desired locations so as to be electrically coupled to the first level metal interconnect structure.

6. The surface-mount structure of claim 5 wherein the diffusion barrier layer is applied between the first level metal interconnect structure and the solder mask.

7. The surface-mount structure of claim 5 wherein the diffusion barrier layer is applied over the solder mask and over or around the solder bumps of the second level I/O connection.

8. The surface-mount structure of claim 1 wherein the diffusion barrier layer is applied over the first level metal interconnect structure and is further configured to function as a solder mask.

9. The surface-mount structure of claim 1 wherein the diffusion barrier layer has a thickness of between one atomic layer and 100 microns.

10. The surface-mount structure of claim 1 wherein the multi-layer substrate structure comprises:

a ceramic insulating layer;

a first metallic layer positioned on one side of the insulating layer to form the first surface of the multi-layer substrate structure; and

a second metallic layer positioned on another side of the insulating layer to form the second surface of the multi-layer substrate structure;

wherein the first and second metallic layers comprise first and second direct bond copper (DBC) layers.

11. The surface-mount structure of claim 1 wherein the sub-module comprises a power overlay (POL) sub-module.

12. A method of manufacturing a surface-mount packaging and interconnect structure comprising:

constructing a sub-module including at least one semiconductor device and a packaging structure formed thereabout, wherein constructing the sub-module comprises:

applying an adhesive layer directly to a dielectric layer;

adhering the at least one semiconductor device to a dielectric layer via the adhesive layer;

forming a first-level metallic interconnect structure over the dielectric layer, the first-level metallic interconnect structure extending through vias in the dielectric layer to electrically connect to the at least one semiconductor device; and

forming a second level input/output (I/O) connection on the dielectric layer on a side opposite the at least one semiconductor device, the second level I/O connection configured to connect the sub-module to an external circuit;

forming a substrate structure that includes a center substrate layer and first and second metallic layers on opposing sides of the center substrate layer, such that the first and second metallic layers form a first surface and a second surface, respectively, of the substrate structure;

attaching the sub-module to the first surface of the substrate structure;

providing a dielectric material between the dielectric layer and the first surface of the substrate structure, the dielectric material at least partially encapsulating the at least one semiconductor device of the sub-module; and

applying a diffusion barrier layer applied over the sub-module, adjacent to the second level I/O connection, and extending down to the multi-layer substrate structure, the diffusion barrier layer configured to reduce the ingress of moisture and gases from a surrounding environment into the surface-mount packaging and interconnect structure.

13. The method of claim 12 further comprising applying a solder mask over the first level metal interconnect structure, with the second level I/O connection extending through the solder mask at pre-determined locations.

14. The method of claim 13 wherein applying the diffusion barrier layer comprises applying the diffusion barrier layer between the first level metal interconnect structure and the solder mask.

15. The method of claim 13 wherein applying the diffusion barrier layer comprises applying the diffusion barrier layer over the solder mask and over or around the second level I/O connection.

16. The method of claim 12 wherein applying the diffusion barrier layer comprises applying one or more layers of an organic material, an inorganic material, a ceramic material, or any combination thereof.

17. The method of claim 12 wherein the diffusion barrier layer is applied to have a thickness of between one atomic layer and 100 microns.

18. A power overlay (POL) packaging structure comprising:

a POL sub-module, the POL sub-module comprising:

a dielectric layer;

a plurality of semiconductor devices adhered to the dielectric layer via an adhesive layer, wherein the adhesive layer is directly attached to the dielectric layer;

a first level interconnect structure electrically coupled to the plurality of semiconductor devices, the first level interconnect structure extending through vias formed through the dielectric layer so as to be connected to the plurality of semiconductor devices; and

a second level interconnect structure to electrically couple the POL sub-module to an external circuit structure, the second level interconnect structure comprising a plurality of solder bumps formed over the dielectric layer and first level interconnect structure and configured to make an interconnection to the external circuit structure;

a multi-layer substrate structure having a first surface and a second surface, wherein the plurality of semiconductor devices of the POL sub-module is attached to the first

surface of the multi-layer substrate structure, and wherein the multi-layer substrate structure includes:

a first direct bond copper (DBC) layer forming the first surface of the multi-layer substrate structure;

a second DBC layer forming the second surface of the multi-layer substrate structure; and

a ceramic layer sandwiched between the first and second DBC layers;

an encapsulate positioned between the dielectric layer and the first surface of the multi-layer substrate structure and at least partially about the plurality of semiconductor devices of the sub-module; and

a diffusion barrier layer applied over the POL sub-module, adjacent to the second level interconnect structure, and extending down to the multi-layer substrate structure, the diffusion barrier layer configured to reduce the ingress of moisture and gases from a surrounding environment into the POL packaging structure.

19. The POL packaging structure of claim 18 further comprising a solder mask applied over the first level metal interconnect structure, wherein the diffusion barrier layer is applied in at least one of a position between the first level metal interconnect structure and the solder mask and a position over the solder mask and over the plurality of solder bumps.

20. The POL packaging structure of claim 18 wherein the diffusion barrier layer consists of organic materials, inorganic materials, ceramic materials, and any combination thereof.

21. The surface-mount structure of claim 1 wherein the first level metal interconnect structure extends out from connection pads of each of the at least one semiconductor device, through a plurality of vias formed in the dielectric layer, and across the dielectric layer on the side opposite the at least one semiconductor device.

22. The surface-mount structure of claim 1 wherein the diffusion barrier layer comprises a multi-layer barrier.

23. The surface-mount structure of claim 1 wherein the diffusion barrier layer comprises a graded composition barrier having a composition that varies across a thickness of the diffusion barrier layer between organic and inorganic materials.