SOLVENT ASSISTED BURNISHING OF PRE-UNDERFILLED SOLDER-BUMPED WAFERS FOR FLIPCHIP BONDING

FIELD OF THE INVENTION

The present invention relates generally to methods for preparing and connecting pre-underfilled solder-bumped integrated circuit chip wafers to a circuit substrate. More specifically, the present invention relates to methods for exposing solder bumps after having laminated a highly filled adhesive film underfill to solder bumped integrated circuit chips, so that the solder bumps can make electrical connections between the integrated circuit chips and their packaging circuits.

BACKGROUND OF THE INVENTION

The vast majority of electronic circuit assemblies in the world today utilize integrated circuit (IC) chips which have been housed in protective packages. These packages provide mechanical and sometimes thermal protection for the chips while also providing an intermediate level of interconnection between the chips and printed circuit boards. Years ago, package sizes were large compared to the size of chips. In part this was necessary because attainable feature sizes for printed circuit boards (PCB) were very large compared to those of chips. Over time, the ability to produce fine-featured circuit boards has improved and package sizes have correspondingly decreased relative to IC size. However, because of the needs to cut costs and reduce circuit size and improve performance, there has been a drive to develop circuit assembly methods which minimize the materials and processes which are required to yield a functional device.

One technique used to reduce circuit size and improve performance involves attaching IC devices directly to a substrate using perimeter or area arrays of solder balls mounted on the face of a chip. By inverting or "flipping" the chip such that the balls are placed in contact with pads on the substrate and passing the entire assembly through a solder reflow process, the IC may be metallurgically bonded to the substrate. Although flip-chip assembly technology was first pioneered over 30 years ago, it has been successfully exploited in only a few different segments of the electronics industry. The most notable examples of electronic products which have exploited flip-chip assembly

include wristwatches, automotive sensors/controllers and mainframe computers. These applications are characterized by the need for either extremely compact circuit size (watches, automotive) or by extremely high computing power per unit volume (mainframes). This underscores the simple fact that by eliminating the intermediate IC package, flip-chip assembly provides the smallest possible footprint for silicon on the circuit board.

A primary reason why flip-chip technology has not enjoyed a more widespread use is because the methodology, as it has currently been developed, is extremely process and equipment intensive. As a result, flip-chip technology is expensive to implement and provides many opportunities for problems to arise. In addition, process and performance requirements of the applications have reached the limits of current materials.

Existing flip-chip technology utilizes chips for which solder has been pre-applied to the interconnection pads. The solder is normally either a 95Pb-5Sn or a 63Sn-37Pb alloy, and it is normally reflowed to form a nearly spherical "bump" prior to final board assembly.

A typical assembly process for flip-chip assembly involves the following steps: 1) flux paste is applied to the substrate bond pads; 2) the IC is aligned and placed on the substrate while the tackiness in the flux holds the chip in place; 3) the assembly is passed through the reflow oven and the solder melts and bonds metallurgically with the substrate pads; and 4) the sample is passed through a flux cleaning operation. Flux removal is normally done with solvent rinses. Originally it was required to use chlorinated solvents to remove the flux residues, but more recently improvements to the flux chemistry has permitted the use of more desirable solvents.

The finished flip-chip assembly must then maintain electrical continuity throughout the lifetime of the device as measured by accelerated tests such as thermal cycling and thermal shock. Mismatches of both the coefficient of thermal expansion (CTE) and the elastic modulus (E) between the silicon IC and the PCB generate high stresses in the contact joints when the circuit is passed through thermal excursions. These stresses can lead to solder joint fatigue failure after repeated temperature cycles, and this is a primary failure mechanism for flip-chip joints. This mechanism has limited the selection

of substrate materials mainly to ceramic hybrid substrates such as Al_2O_3, which has high modulus and low CTE, properties similar to silicon. Even with ceramic substrates, flip-chip assembly is limited to applications with small dice.

During the last ten to fifteen years there has been increasing interest in learning how to apply this flip-chip assembly to both larger size die and also to a broader range of printed circuit substrates. Specifically the increased wiring densities available with today's organic based substrates makes them suitable low cost substitutes for ceramic substrates. However, the relatively high CTE of organic materials has slowed the implementation of flip-chip assembly on organic substrates due to the aforementioned failure mechanism. An important breakthrough has been the development of the underfill process. The underfill process uses a high modulus curable adhesive to fill the empty space between the solder balls under the chip so that the stress in the joint is shared by the adhesive and distributed more evenly across the entire interface as opposed to being concentrated at the perimeter balls. The use of an "underfill' adhesive as described above has enabled a flip-chip technology to be applied to a broader range of assemblies.

In current practice, underfill resin is applied as a liquid and is allowed to wick under the reflowed assembly via capillary action. Hence this type of encapsulation is often referred to as "Capillary Underfill". The current procedure for applying and curing underfill resins is separate from and is appended to the overall process sequence described above. After the reflow and flux removal steps, it is necessary to: pre-dry the bonded assembly, preheat the bonded assembly (to aid the wick-under), dispense resin, allow resin to wick under the die, dispense again, and then cure. Currently available underfill resins can require cures of up to 2 hours at 150°C. The extra dispense steps are often needed in order to make sure that there is no entrapped air under the chip and also to provide a good fillet shape around the chip. Developing and maintaining good control over these types of material characteristics and dispensing processes is very difficult, and any imperfections will hurt the reliability of the solder joints. Also, although capillary underfill is still widely used, trends in IC design towards larger IC size and reduced pad pitch will result in increases in both required wicking times and in defect occurrences.

Recently, an alternative approach for applying underfill resin has been pursued in which the uncured liquid resin is actually dispensed prior to the chip placement. The liquid resin in this case is used in place of the aforementioned flux paste, and special adhesive formulations have been developed that are capable of providing fluxing action in the reflow oven before they begin to cure significantly. This type of material is often referred to as a "No-Flow Underfill" because of the elimination of the capillary flow step. Special adhesive formulations that are capable of providing some degree of a fluxing action as they cure in the reflow oven may be used. Because the resin is present on the board before the chip is placed, it is necessary to press the chip down into the resin and displace the resin from the contact sites. This approach is attractive in that it eliminates flux cleaning, dispensing and wicking steps. However, it has been shown that in order for this approach to work, the underfill resin must be unfilled. The inability to utilize fillers in the underfill resin with this approach is a constraint that is expected to limit its utility in dealing with large IC size and fine pitch. See, for example, U.S. Patent No. 5,128,746, Shi et al., High Performance Underfills for Low-Cost Flipchip Applications, Proc. 3d Int'l Symp. On Adv. Packaging Materials, March 1997; Gamota et al., Advanced Flipchip Materials: Reflowable Underfill Systems, Proc. Pac. Rim ASME Int'l Intersociety Electronic and Photonic Packaging Conf., ASME, June 1997; Johnson et al., Reflow Curable Polymer Fluxes for Flipchip Assembly, Proc. Surface Mount Int'l 1997.

The choice of chemistry for the underfill adhesive is constrained by the processing and performance requirements stated above. For best fatigue performance, it is best to choose materials that have the highest modulus and lowest CTE over the temperature range of the thermal cycling. For polymers, this means a glass transition temperature (Tg) above anywhere from 125 to 170°C, depending on the application. By filling polymers with inorganic fillers such as SiO_2 the CTE and modulus may be brought closer to that of silicon. However, to achieve CTE of less than 30 ppm per degrees Celsius in a polymer system, a filler loading of 50% by volume or higher is typically required. Such high filler loading raises the viscosity significantly. To achieve the required balance of processability and cured material properties, it is common to use epoxy resins with the lowest possible viscosity. Highly filled and cured to a high Tg, these materials are quite brittle when cured

and have poor adhesion to polyimide and aluminum nitride passivation layers on the IC's. The optimization of an underfill adhesive system is, therefore, a necessary compromise between processing requirements and performance requirements. An improved flip-chip assembly process or construction which reduced or eliminated any of these materials constraints has the potential to significantly improve the reliability of flip-chip assembly through improved chemistry.

In review of the background, a reliable solder flip-chip method of IC interconnect on ceramic substrates is just beginning to be applied to organic substrates. Significant processing and materials challenges are slowing this technology in spite of strong demand from designers. The current flip-chip assembly process has too many steps, is too costly and is not extendable to future IC designs. A simplified flip-chip assembly process which reduces cost and demands from the underfill adhesive system will enable flip-chip assembly to become a more broadly attractive approach for circuit assembly.

SUMMARY OF THE INVENTION

The present invention provides a new way to simplify the flip-chip assembly process and enables the use of a broader range of materials thereby reducing assembly cost and improving interconnect reliability.

One aspect of the present invention relates to a method for connecting an integrated circuit chip to a circuit substrate. The method includes the step of pre-applying adhesive directly to a bumped side of the integrated circuit chip and removing portions of the adhesive to expose the bumps. The portions of adhesive can be removed after the adhesive application process, preferably by a solvent-assisted burnishing of the bumps. The method also includes the step of pressing the bumped side of the integrated circuit chip, which has previously been coated with adhesive, against the circuit substrate such that the bumps provide an electrical connection between the integrated circuit chip and the circuit substrate. The pre-applied adhesive on the chip forms a bond between the integrated circuit chip and the circuit substrate.

The above-described method provides numerous advantages over the prior art. For example, by applying the adhesive to the bumped IC prior to substrate attachment,

encapsulation of the bumps is easier to achieve and can be more easily inspected, irrespective of IC size and pitch. Also, because no wick under processes are used, the viscosity requirements for adhesive application are significantly relaxed as adhesives with viscosities on the order of about 1000 to about 30,000 poise may be used to achieve effective encapsulation. The removal of the viscosity constraint permits higher filler loading if necessary, as well as the use of alternative chemistries and catalysis systems. Such extra formulation latitude has the potential to enable higher reliability assemblies through improved adhesive material properties. Additionally, the above-described method offers the potential for fluxless attach due to the scrubbing action of the bumps as they deform in the bonding process.

Another aspect of the present invention relates to a method for preparing integrated circuit chips for assembly. The method includes the step of providing a wafer including a bumped side having a plurality of conductive bumps. The method also includes the steps of applying adhesive to the bumped side of the wafer, softening the adhesive with a solvent, wiping the softened adhesive from the tips of the bumps, and then dicing the wafer into individual integrated circuit chips. Because the adhesive is deposited at the wafer level, rather than the chip level, no dispensing, wicking, or damming are required. The process is also faster when conducted at the wafer level, rather than at the chip level. Additionally, with the use of faster curatives, post curing may be eliminated.

A further aspect of the present invention relates to an integrated circuit chip. The integrated circuit chip includes a bumped side having a plurality of conductive bumps. The chip also includes a layer of adhesive that covers the bumped side. The bumps have exposed contact regions that are substantially uncovered by the adhesive layer. The novel solvent assisted burnishing of the bumped side of the wafer allows the exposed contact regions of the bumps to retain their original rounded profile.

A variety of additional advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the claims. It is to be understood that both the foregoing general description and the following detailed

description are exemplary and explanatory only and are not restrictive of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention, and together with the description, serve to explain the principles of the invention. A brief description of the drawings is as follows:

Figs. 1A-1C illustrate a method for preparing an IC chip for connection to a circuit substrate;

Figs. 2A-2B illustrate a method for connecting the prepared IC chip of Fig. 1C to a circuit substrate;

Figs. 3A-3B are micrographs of an IC chip processed via the method of Figs. 1A-1C, Fig. 3A shows the chip prior to abrasion and Fig. 3B shows the chip after abrasion;

Figs. 4A-4C illustrate an alternative method for preparing an IC chip for connection to a circuit substrate;

Figs. 5A-5B are micrographs of an IC chip processed via the method of Figs. 4A-4C, Fig. 5A shows the chip prior to abrasion and Fig. 5B shows the chip after abrasion;

Fig. 6A is a cross-sectional micrograph of an IC chip connected to a circuit substrate, the IC chip was not subjected to an abrasion step prior to connection;

Fig. 6B is a cross-sectional micrograph of an IC chip connected to a circuit substrate, the IC chip was subjected to an abrasion step prior to connection;

Figs. 7A and 7B illustrate a method for making a conductive tape; and

Figs. 8A and 8B illustrate a method for making an electrical connection using the conductive tape of Figs. 7A and 7B; and

Figs. 9A-9D illustrate a method for encapsulating bumps on wafer integrated circuits.

Fig. 10 illustrates a thickness profile of the adhesive on an IC chip after dry burnishing with 1200 grit Emory paper.

Fig. 11 is a micrograph of the IC chip of Figure 10, showing contamination of the adhesive and flattening of the solder bumps.

Fig. 12 shows an IC chip after solvent assisted burnishing which provided poor uniformity and left excessive residue on the IC chip.

Fig. 13 shows an IC chip after solvent assisted burnishing which provided fair uniformity and left minimal residue on the IC chip.

Figs. 14A and 14B illustrate the thickness profile of the adhesive on an IC chip after solvent assisted burnishing.

Figs. 15A-15C illustrate a solvent assisted burnishing method for preparing an IC chip for connection to a circuit substrate, where the adhesive thickness is greater than the height of the solder bumps.

Figs. 16A-16C illustrate a solvent assisted burnishing method for preparing an IC chip for connection to a circuit substrate, where the adhesive thickness is less than the height of the solder bumps.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to exemplary embodiments of the present invention which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

The present invention provides an alternate means for applying underfill adhesive resin to an IC chips. In this case, underfill resin is applied to the bumped sides of IC chips, preferably at wafer level, before the chips have been bonded to an interconnect substrate such as a printed circuit board (PCB). The resin may be applied by techniques such as laminating a film material or by liquid coating. In contrast to traditional underfill methods that rely on wicking to cover the hidden surface, the present invention allows resin to be directly coated on the entire exposed surface/face of the IC chips. Consequently, the problems with entrapped air or incomplete filling typically associated with the traditional underfill are eliminated. With the present method, underfill resin coverage and thickness can be controlled to ensure uniformity. Because the wick-under process is eliminated, rheological requirements of the uncured resin are relaxed. This in turn can permit the use of alternative chemistries and higher filler loading to attain better mechanical properties after cure.

After the chips have been coated with the adhesive resin, or during the coating process itself, portions of the adhesive resin are removed to expose the tops of the solder bumps. The adhesive removal may be accomplished by several means, including physical removal by abrasives that vigorously remove material (including some solder), physical removal by displacement of the adhesive, indirect physical removal such as with plasma treatment, or by combining physical and chemical agents for removal in which surfaces with lower (i.e., finer) abrasive quality are combined with solvents to scrub the adhesive clear of the solder balls. For example, a mechanical process can be used to remove the previously applied adhesive from the tops of the bumps. Exemplary mechanical processes include rubbing the adhesive with an abrasive material, scraping the adhesive with a knife edge, or compressing the adhesive to thin and eventually crack or otherwise displace the adhesive material from the tops of the bumps.

The above-described adhesive removal step is important because to achieve good metal-to-metal contact between the solder bumps and the interconnect substrate prior to the reflow step, the top surfaces of the bumps should preferably be at least partially exposed. The adhesive removal and bump exposing step also function to remove oxide films from the bumps that were formed during their initial reflow. In some instances, it may be desirable after the bump exposure operation has been completed, to apply a film or other type of protective cover to the wafer/chips to protect the adhesive and the exposed bumps.

After the tips of the bumps have been exposed, the wafer forming the chips is diced into a plurality of discrete chips. Following wafer dicing (and removal of the protective film, if any), a selected IC chip can be aligned and pre-attached to the interconnect substrate with heat and pressure. Normally a small amount of a no-flow underfill material is dispensed onto the PC board just prior to the chip placement step. This additional material serves to provide a complete filling of the bond line and also acts as a temporary adhered to hold the chip in place until it reaches the reflow oven. During this pre-attachment step, the solder bumps of the chip are deformed slightly in order to further ensure both good metal to metal contact between the IC and the interconnect substrate as well as good wetting of the adhesive to the substrate. The bump deformation

accommodates the stand off of the IC from the substrate and allows the adhesive to be brought down to contact and fully wet the substrate surface thereby completely filling the cavity under the chip. In addition, the collapse of the bumps causes the surface oxides on the solder bumps to crack and open exposing fresh solder which is then smeared across the substrate pads forming a good metallurgical bond.

When the resin-coated IC chip is bonded to the interconnect substrate, the pre-applied adhesives forms and maintains a mechanical bond between the chip and the substrate significantly reducing the strain in the solder joints. Depending on the application, the solder joints may be formed without flux and still form reliable interconnects. In this case, the adhesive serves to affix the IC to the board prior to reflow instead of a flux paste. The solder reflow process can also serve to partially or even fully cure the underfill resin, which can possibly eliminate the need for an additional post cure.

Figs. 1A-1C show an exemplary process, in accordance with the principles of the present invention, for preparing an IC chip for electrical connection to a circuit substrate. Fig. 1A shows an IC chip 20 or wafer having a passivation surface 22 on which a plurality of conductive bumps 24, such as solder bumps, are disposed. The bumps 24 can be made of a variety of known conductive materials. Exemplary materials include meltable solid metals, gold, conductive slurries, conductive polymers, electroless nickel, and electroless gold.

The bumps 24 are preferably deposited on input/output pads of the chip 20 and protrude or project outward from the passivation surface 22 of the chip 20. The bumped side of the chip 20 has been covered with a layer of adhesive material 26 such as adhesive film or adhesive solution. The adhesive can be deposited or applied to the bumped side of the chip by any number of known techniques. For example, the adhesive can be coated as a hot melt, coated from solution, or bonded as a film in a lamination process.

The adhesive material 26 fills the volume around the bumps 24 and protects the bumps 24 during handling prior to assembly. As shown in Fig. 1A, the adhesive material 26 has a thickness which is less than the heights of the bumps 24. As a result, the exposed surface of the adhesive 26 has a plurality of adhesive protuberances 28 that correspond to the bumps 24. The protuberances 28 cover the bumps 24 and project outward from a

substantially flat primary adhesive surface 30 that is located between the bumps 24. If the adhesive is applied as a liquid, the liquid is preferably b-stage cured or dried to form an adhesive film.

To ensure a better electrical connection with a substrate, it is preferred to at least partially remove the adhesive protuberances 28 that cover the bumps 24. As shown in Fig. 1B, an abrasion process is employed to remove the adhesive material located on top of the bumps 24 exposing the conductive bumps 24 for better electrical connection with a packaging substrate. In the abrasion process, an abrasive material 32 such as sandpaper, micro abrasive, abrasive pads available from 3M Company, St. Paul, MN under the trade designation Scotch Bright, a cloth, a scraping blade or a coating knife is brought in contact with the adhesive protuberances 28 that cover the bumps 24 such that the bumps 24 are exposed for electrical conduction. Because the protuberances project above the average adhesive height on the chip 20, such protuberances become pressure focal points that receive the most abrasion or cutting. Fig. 1C shows the chip 20 after the bumps have been exposed via abrasion. Once the bumps have been exposed, a film, tape or other type of protective cover may be applied to the chip 20 to protect the adhesive 26 and the exposed bumps 24.

A variety of techniques can be used to expose the conductive bumps 24. If the adhesive is coated as a liquid, a scraper or knife edge can be used to remove adhesive from the bumps during the coating process. For example, the knife could be used to spread the adhesive and simultaneously remove portions of the adhesive from over the bumps 24. Alternatively, the bumps 24 could be exposed via abrasion after the liquid adhesive has hardened. Furthermore, the adhesive could be applied as a film with portions of the film being removed by an abrasion process.

As shown in Fig. 1C, each bump 24 extends completely across the adhesive layer 26. In this manner, the height of each abraded bump 24 is roughly equal to or higher than the thickness of at least portions of the adhesive layer 26. Additionally, the exposed regions 36 of the bumps 24 are slightly raised with respect to the primary adhesive surface 30.

Figs. 2A and 2B illustrate a method for electrically connecting the prepared chip 20 to a circuit substrate 34 such as a packaging circuit. To connect the chip 20 to the circuit substrate 34, exposed regions 36 of the bumps 24 are aligned with circuit pads 38 of the circuit substrate 34. Next, the chip 20 is pressed against the circuit substrate 34 with sufficient force to generate electrical contact between the bumps 24 and the circuit pads 38, and to cause the adhesive 26 to wet and fill around the bumps 24 and circuit substrate 34.

It is preferred for the bumps 24 to deform during the bonding process. By deforming the bumps 24, standoff between the chip 20 and the substrate 34 is reduced and the adhesive 26 is caused to fully wet and encapsulate the substrate circuit topography expelling entrapped air. The adhesive 26 may be cured during the bonding process or in a separate bake cure at a later time. Once cured, the adhesive 26 provides the mechanical bond between the IC chip 20 and substrate 34, redistributes the stresses at the solder joints and encapsulates the bumps 24 protecting them from the environment.

In an experimental example that illustrates the above-described aspects of the present invention, an IC chip manufactured by Flipchip Technology was utilized. Solder bumps having 4 mil diameters were located on the perimeter of the chip. An adhesive manufactured by DuPont, with a trade name of Pyralux LF, was used to overcoat the bumps. Specifically, a 3 mil thick layer of adhesive was placed on the bumped chip surface by pressing the adhesive to the chip that was heated to 100°C on a hot plate. Fig. 3A is a micrograph of the chip after having been coated with adhesive. The 4 mil tall bumps were higher than the thickness of the adhesive, so there was substantial protrusion of these bumps above the primary adhesive surface on the chip surface. An Imperial Lapping Film micro abrasive manufactured by 3M Corporation was used to remove the adhesive from the tops of the bumps so as to expose the bumps. Fig. 3B is a micrograph the chip after the bumps have been exposed via abrasion. Inspections of the abraded parts found no evidence of abraded conductive material on the processed parts. The abraded adhesive and bump materials were apparently carried away by the abrasive film.

Figs. 4A-4C illustrate another process, in accordance with the principles of the present invention, for preparing an IC chip for connection to a circuit substrate. It will be

appreciated that the process of Figs. 4A-4C has aspects that are similar to the process of Figs. 3A-3C. For example, Fig. 4A shows an IC chip 120 including a plurality of conductive bumps 124 deposited on a passivation surface 122 of the chip 120. The bumped side of the chip 120 is covered with a layer of adhesive material 126 having a thickness equal to or greater than the heights of the bumps 124. The adhesive material 126 covers the bumps 124 and has an exposed primary surface 130 that is substantially parallel to the passivation surface 122.

As shown in Fig. 4B, a cutting or abrasion process is employed to remove the adhesive material on top of the bumps 124 exposing the conductive bumps 124 for better electrical connection with a packaging substrate. In the abrasion process, an abrasive material 132 is used to burnish the entire primary surface 130 of the adhesive 126 such that the bumps 124 are exposed for electrical conduction. Fig. 4C shows the chip 120 after the bumps have been exposed via abrasion. Once the bumps have been exposed, a film, tape or other type of protective cover may be applied to the chip 120 to protect the adhesive 126 and the exposed bumps 124.

As shown in Fig. 4C, each bump 124 extends completely across the thickness of the adhesive layer 126. In this manner, the height of each abraded bump 124 is roughly equal to the thickness of at least portions of the adhesive layer 126. Additionally, the exposed regions 136 of the bumps 124 are substantially flush with respect to the primary adhesive surface 130. It will be appreciated that the chip 120 can be connected to a circuit substrate in substantially the same manner previously described with respect to Figs. 2A and 2B.

Fig. 5A is a micrograph of an exemplary chip having bumps which have been coated with adhesive in the same manner the chip 120 of Fig. 4A. Additionally, Fig. 5B is a micrograph of the chip of Fig. 5A after portions of the adhesive have been abraded to expose the conductive bumps.

With respect to the above-described embodiments, if the adhesive coating has low flow characteristics during bonding, non-polished bumps may not be able to push through the adhesive to make contact with the bonding pads. Fig. 6A shows a cross-sectional image of a non-abraded chip bonded to a FR4 board using Pyralux, a no-flow adhesive

manufactured by DuPont. The cross-sectional photo shows that the bumps are not in contact with the substrate because the adhesive is thick and covering the bumps. Fig. 6B shows a cross-sectional image of a polished/abraded chip bonded to a FR4 board using Pyralux. In contrast to the chip of Fig. 6A, the cross-section photo of Fig. 6B shows that the bumps are in contact with the substrate because the polishing process was used to remove the extra adhesive from the bump tops.

If the adhesive coating flows significantly, the bumps will push through the adhesive somewhat during bonding. However, the adhesive 126 can get trapped under the bump, thereby preventing good metallurgical bond formation. Consequently, even when high flow adhesives are utilized, it is still typically preferred to abrade the adhesives.

Figs. 7A-7B show another aspect of the present invention which relates to a method for making a z-axis conductive tape. The method includes the step of providing an array of conductive particles 210. An exemplary size distribution for the particles is from 20-75 micrometers. The method also includes the step of coating the particles 210 with a layer of adhesive 214 as shown in Fig. 7A. The adhesive 214 can be applied to the particles 210 by a variety of techniques. For example, the adhesive can be coated as a hot melt, coated from solution, pressed as a film upon the particles 210, or bonded as a film in a lamination process. Additionally, the particles can be mixed within an adhesive suspension which is spread to form a layer or film of adhesive having a plurality of coated particles contained therein.

The adhesive 214 has a primary thickness t that is less than the size of the particles 210. As a result, the adhesive 214 has a top surface 216 having a plurality of humps or top protuberances 218 that correspond to the particles 210. The adhesive 214 also includes a bottom surface 217 having a plurality of bottom humps or protuberances 219 that correspond to the particles 210. Of course, in alternative embodiments of the present invention, the adhesive may have a primary thickness equal to or greater than the size of the particles. In such an embodiment, the adhesive would preferably define substantially flat top and bottom surfaces.

After the adhesive 214 has been applied to the particles 210, at least portions of the top protuberances 218 are removed such that top contact regions 220 of the particles 210

are exposed. Similarly, at least portions of the bottom protuberances 219 are removed such that bottom contact regions 224 of the particles 210 are exposed. The particles 210 can be exposed by techniques such as burnishing or polishing the top and bottom surfaces 216 and 217 of the adhesive 214 with an abrasive material.

In certain embodiments of the present invention, the particles 210 can initially be supported on a release liner (not shown) while adhesive is applied to the particles 210. In such an embodiment, after the particles 210 have been covered with the adhesive 214 and the top contact regions 220 have been exposed by techniques such as abrasion, the liner is removed from the back or bottom side 217 of the adhesive 214 allowing the bottom side 217 of the adhesive to be processed.

Fig. 7B shows the adhesive 214 after the top and bottom contact regions 220 and 224 have been exposed. The product depicted in Fig. 7B comprises a strip of conductive tape 226 suitable for providing z-axis electrical connections. The particles 210 of the tape 226 have sizes substantially equal to or greater than the thickness of the adhesive 214. As a result, each particle 210 extends completely across the thickness of the adhesive 214. A protective film or cover can be used to protect the exposed top and bottom contact regions 220 and 224 until the tape 226 is actually used to provide an electrical connection.

Figs. 8A and 8B show a method of providing a z-axis connection between first and second electrical components 228 and 230 using the conductive tape 226. As shown in Fig. 8A, the conductive tape 226 is positioned between conducting pads 232 of the electrical components 228 and 230. Next, as shown in Fig. 8B, the tape 226 is pressed between the electrical components 228 and 230 with sufficient force to generate electrical contact between the particles 210 and the circuit pads 232. While the tape 226 is pressed, the tape 226 is also heated such that the adhesive 214 wets and fills around the particles 210, and forms a bond between the electrical components 228 and 230. The adhesive can be cured during the bonding process or in a separate bake cure at a later time.

Figs. 9A-9D illustrate an exemplary method for manufacturing integrated circuit chips in accordance with the principles of the present invention. Fig. 9A shows a wafer 320 having a passivation surface 322 on which a plurality of conductive bumps 324 are

disposed. An adhesive film 326 with a protective backing 328 is located adjacent to the passivation surface 322.

Fig. 9B shows the adhesive film 326 being pressed against the passivation surface 322 of the wafer 320. As the adhesive film 326 is pressed against the wafer 320, the adhesive 326 covers the bumps 324 and deforms to fill the voids around the bumps 324. Also, the adhesive film 326 bonds with the passivation surface 322 of the wafer 320.

Next, as shown in Fig. 9C, the wafer 320, which has been pre-coated with adhesive, is diced or divided into discrete integrated circuits 330. Finally, as shown in Fig. 9D, the backing layer 328 is removed from the integrated circuits 330 such that the adhesive layer 326 is exposed. With the backing 328 removed, the integrated circuits are ready for connection to a substrate.

In the foregoing detailed description, the step of removing portions of the adhesive from the bumps to create exposed contact areas has been described in terms of a mechanical process using an aggressive abrasive, scraping the adhesive with a knife edge, or compressing the adhesive to thin and eventually crack or otherwise displace the adhesive material from the tops of the bumps. However, as illustrated in Figures 1C, 2A, 2B, 3B, 4C and 5B, the use of these types of methods for removing adhesive from the surface of the solder bumps also results in removal of some of the solder material. The use of abrasive materials to remove encapsulant material from the tips of the solder bumps as described above clearly shows that this type of scrubbing removes some solder along with the encapsulant from the bump tips, resulting in a flattened bump shape in which the flats of the bump are essentially flush with the adhesive surface.

Removal of solder from the bumps is undesirable for several reasons. These reasons include loss of control of solder volume from bump to bump and from chip to chip, which could compromise the IC reliability. Additionally, solder debris may be spread over the surface of the encapsulant, thereby creating a contamination problem. Finally, the loss of the spherical surface of the solder bump can complicate the automated alignment and placement of the IC chip onto the printed circuit board substrate. Therefore, it is desirable to remove the encapsulant from the surface of the solder bumps without removing any solder from the solder bumps or causing the tips of the solder

bumps to be flattened. That is, it is desirable for the solder bumps to retain their original rounded profile.

It has been found that the underfill material may be removed from the solder tips by means of a wiping action rather than an abrading action. That is, a relatively soft material such as a woven or non-woven fabric or an open cell foam may be used. Prior to use, the wiping pad is dampened with a small amount of an appropriate solvent to soften the encapsulant. Alternatively, a harder micro-structured surface can also be used in place of the wiping pad. When using a harder micro-structured surface, an appropriate amount of solvent is applied to the low spots on the micro-structured surface just prior to use. By employing this type of gentle, solvent assisted wiping action it is possible to remove the underfill encapsulant from the bump tips without altering the bump size and shape in any significant way. Examples of solvent assisted burnishing or wiping of the solder bumps are provided below.

Examples of Solvent Assisted Burnishing

For each of the examples described below, epoxy based underfill encapsulants were used. In all cases, the encapsulants were formulated so as to provide a flexible film format. All of the materials were loaded with a spherical, amorphous silica powder at a level of two parts filler to one part adhesive solids by weight. The silica powder had a size range of 2 to 10 microns diameter nominally. In all examples described below, the adhesive solids were comprised primarily of a blend of epoxy with a largely non-reactive thermoplastic component. The ratio of epoxy:thermoplastic was in the range of 7:3 to 8:2. In all cases, acetone was used as a solvent for the adhesives. Other suitable solvents may be used, as is appropriate for the particular adhesive underfill being used.

Example One: (Comparative, Dry Abrading)

A piece of silicon measuring approximately 2 x 2 inches and comprising an array of 9 x 9 bumped chips was used. The solder bumps were approximately 100 microns in diameter and were of a eutectic 63-37 Sn-Pb alloy. Each chip contained 68 bumps in a peripheral array. The chips were pre-encapsulated, using a heat-lamination process, with

an uncured one-part epoxy based adhesive film having an initial thickness slightly greater than 100 microns.

The pre-encapsulated wafer-section was attached bumped side-up to an aluminum puck which was then placed face down into a Struers Metallurgical polishing machine, available from Struers, Inc. of Westlake, Ohio. The 8 in. diameter turntable was provided with a single piece of 1200 grit Emory paper. The wafer-section was placed in contact with the Emory paper with a total force of 5N. The turntable and the wafer section were spun independently at 150 rpm for a period of 35s with no applied lubricant.

After the dry abrading operation, the adhesive surface was found to be quite smooth. Many but not all of the solder bumps were exposed. A thickness profile of the adhesive revealed a crowned shape as illustrated in Figure 10. The photograph in Figure 11 illustrates the undesirable flattening of the bumps as well as evidence of contamination from possibly both solder debris and residual abrasive media trapped in the adhesive layer.

Example 2: (Comparative, Plasma Etching)

A single chip was laminated with an uncured one-part epoxy based adhesive film. The chip contained solder bumps of roughly 100 micron diameter. The adhesive was laminated by pressing by hand at a temperature of 60 degrees C. Bump locations were visible but bumps were not exposed. Plasma etching was attempted with a Model PS0524 unit from Plasma Science, an RF type system operating at 13.5 MHz and delivering a maximum power of 500W with matching network capability. An oxygen plasma was used. The chip was placed in the middle of the plasma field, which was of a sky blue color. A maximum power in the range of 60% of full power was used, and the chip was exposed for a period of about 15 minutes. Afterwards the adhesive surface was examined with SEM. The surface appearance suggested only a small degree of etching of the adhesive matrix but minimal to no etching of the silica filler particles themselves. The bumps, which were closely examined, remained largely covered with silica filler and some adhesive residue after the etching exposure.

Example 3: (Present Invention, Effect of Wiping Material)

Pieces of silicon measuring approximately 0.8 x 0.8 inches, each comprising an array of 4 x 4 chips, were used. Each chip contained 88 eutectic SnPb bumps of approximately 100 micron diameter. The chip arrays were not pre-diced. Each chip array was pre-encapsulated using a heat-lamination process with an uncured one-part epoxy based adhesive film having a thickness of approximately 100 microns.

For each chip array, the clearing of encapsulant from the bump tips was attempted with one from the series of polishing pad materials listed below in Table I. The polishing pad materials are available from Struers, Inc. of Westlake, Ohio, Allied High Tech Products, Inc. of Rancho Domingo, California, and The Texwipe Company LLC of Upper Saddle River, New Jersey.

For each experiment, the polishing pad was slightly dampened with a small amount of acetone immediately prior to use. Care was taken to avoid having any standing liquid on top of the polishing pad. Each pad was sized at 8 inches diameter to match the turntable of the Struers Metalographic polishing machine. The chip array to be treated was placed bumped side up on an aluminum puck weighing 83g, and the puck was placed into the polisher with the bumped surface facing the polishing pad. The weight of the puck was the only z-axis force applied to the test piece. The turntable and the test piece were independently rotated at 150rpm for the time periods indicated.

Samples were evaluated for uniformity of adhesive removal, amount of residue left by the pad and the amount of adhesive removed. The uniformity of adhesive removal and amount of residue left were evaluated qualitatively. Representative photographs of a sample with excessive residue and poor uniformity are shown in Figure 12, and a sample with minimal residue and fair uniformity are shown in Figure 13. All results are shown in Table I. Examples 3H and 3I were identified as the most preferred approaches from this set, as they exhibited the best uniformity while producing the least amount of residue.

Table I
Solvent Assisted Burnishing, Pad Screening Test Results

	Pad Type	Pad Identification	Burnish Time (s)	Final Adh. Thk. (mm)	Amt. Of Residue From Pad	Uniformity of Adh. Surface
A	Felt	Allied "Billiard"	25	75	Excessive	Fair
B	Felt	Allied "Blue Felt"	28	75	Minimal	Fair
C	Composite	Allied "XT"	28	5	Excessive	Poor
D	Paper	Clean Room, Blue, Class 100			Excessive	Poor
E	Foam	Allied "Chem-Pol"	25	75	Moderate	Fair
F	Foam	Struers "POCTA"	28	75	Moderate	Poor
G	Foam	Struers "POCOA"	28	62	Moderate	Poor
H	Fabric	Texwipe "TX309"	28	75	Minimal	Fair
I	Composite	Struers "MD Plan"	25	75	Minimal	Fair

Example 4: (Present Invention, Effect of Adhesive Thickness)

The preferred pad materials from Examples 3H and 3I were used to assess the effect of adhesive thickness on both the required burnishing time and on the resulting thickness uniformity and surface appearance of the wafer-applied encapsulant material. Other than varying the adhesive thickness and resulting required burnishing times, all other details were as described in Example 3. After burnishing was completed, an adhesive thickness measurement was made for each of the sixteen chips on each test sample. Also, qualitative determinations were made of surface smoothness and condition of the bump surfaces. The results are summarized in Table II below. For Example 4H, it was not possible to complete the burnishing process with the MD-Plan alone because there was too much adhesive volume present compared with the volume of adhesive which the plate could accommodate in its low spots. In this example a second burnishing step using the Texwipe fabric was used in order to complete the exposure of the bumps.

Table II

Solvent-Assisted Burnishing, Adhesive Thickness Effects

	Pad ID	Adhesive Thickness, Initial (microns)	Required Burnish Time (s)	Adhesive Thickness, Final (microns)	Std. Deviation of Final Thickness (microns)	Surface Condition After Burnish	Bump Tip Condition After Burnish
A	Texwipe "TX309"	90	3	61	9.9	Smooth	Smooth, Spherical
B	Texwipe "TX309"	100	3	80	6.4	Smooth	Smooth, Spherical
C	Texwipe "TX309"	116	5	80	6.8	Smooth	Smooth, Spherical
D	Texwipe "TX309"	125	8	71	11	Smooth	Smooth, Spherical
E	Struers "MD Plan"	90	10	87.5	2.3	Non-Uniform	Slight Flattening
F	Struers "MD Plan"	100	5	87.5	1.2	Non-Uniform	Slight Flattening
G	Struers" MD Plan"	116	5	87.5	2.8	Smooth	Slight Flattening
H	Struers "MD Plan"	125	>20	76	6.7		Slight Flattening

Example 5: (Present Invention, Burnishing at wafer level)

The Texwipe"TX309" pad material was used to assess the ability to practice solvent-assisted burnishing at the near-wafer level. In this instance, an array of 9 x 9 chips measuring approximately 1.8 x 1.8 inches was used. This was the largest wafer segment that could be placed successfully into the Metalographic polisher which was used. The chip type was the same as was used in Examples 3 and 4. Two different uncured one-part epoxy based adhesive films were tested for Example 5A and Example 5B. Adhesive film thicknesses were approximately 100 microns. Once again acetone was used as the solvent. Once the solvent-assisted burnishing was completed, surface profiles were generated from dial indicator readings to illustrate the degree of uniformity for the resulting adhesive thicknesses. The results are shown in Figures 14A and 14B below. In these examples the average thickness of the underfill layer after burnishing

was approximately 80 microns, while the bump height was approximately 100 microns. The standard deviations of the thickness measurements were found to be 15 and 11 mm respectively for examples 5A and 5B.

As illustrated in Figures 15A-15C and 16A-16C, the integrated circuit chips 420 which are prepared using the solvent assisted burnishing technique as described in the Examples above have solder bumps 424 which have not been altered significantly or deformed in the adhesive underfill removal process. The processed IC chips 420 have a passivation surface 422 on which conductive bumps 424 are disposed. The passivation surface 422 and bumps 424 are covered by adhesive material 426.

In Figures 15A-15C, an IC chip 420 including conductive bumps 424 is covered with a layer of adhesive 426 with a thickness equal to or greater than the height of bumps 424. Adhesive material 426 covers bumps 424 and has an exposed primary surface 430 that is substantially parallel to the passivation surface 422. As shown in Figure 15B, a polishing pad 432 is wetted with a suitable solvent 434 for softening the adhesive 426. The softened adhesive may then be wiped or polished away with polishing pad 432 until the rounded profile of bumps 424 are exposed. After the bumps 424 are exposed, they may be bonded to the printed circuit board substrate in a manner consistent with that described above for abrasive underfill removal techniques, as shown for example, in Figures 2A and 2B.

In Figures 16A-16C, the adhesive material 426 is of a thickness less than the height of the bumps 424. As a result, the exposed surface of the adhesive 426 has a plurality of adhesive protuberances 428 that correspond to the bumps 424. The protuberances 428 cover the bumps 424 and project outwardly from a substantially primary adhesive surface 430 that is located between the bumps 424. A polishing pad 432 is wetted with a suitable solvent 434, such as acetone or other solvent as may soften the adhesive 426. Solvent 434 softens the adhesive 426 such that polishing pad 432 may remove adhesive 426 without disturbing the rounded profile of bumps 424, as shown in Figure 16C. As described above, once the bumps 424 have been exposed, a film, tape or other protective cover may be applied to the chip 420 to protect the adhesive 426 and the exposed bumps 424.

As shown in Figures 15A-15C and 16A-16C, the use of polishing pad 432, together with solvent 434 allows the exposed regions 436 of the bumps 424 to retain their original rounded shape. Retaining the rounded profile of the bumps confers additional benefits on the bonding process, as it allows easier deformation of the bumps 424 during the bonding process. As noted above, by deforming the bumps 424, the stand off between the IC chip 420 and the substrate is reduced and the adhesive is caused to fully wet and encapsulate the substrate circuit topography. During the deformation process, the surface of the solder bump 424 cracks and exposes unoxidized and clean solder for the connection to the substrate, thereby resulting in a better bond between the IC chip and the substrate.

As can be seen, the solvent assisted burnishing technique described herein provides significant advantages over other adhesive encapsulant removal techniques. The solvent assisted burnishing allows the solder bumps to remain unaltered and undeformed prior to connection to a circuit substrate, and thereby ensures greater uniformity of the solder bumps and greater reliability of the interconnects formed by the solder bumps.

It will be appreciated that other techniques could also be used to apply adhesive to the wafer. For example, the adhesive can be coated as a hot melt or coated from solution. Additionally, the above-described method can also include the step of removing portions of the adhesive from the bumps to generate exposed contact areas as previously disclosed in the detailed description.

With regard to the foregoing description, it is to be understood that changes may be made in detail, especially in matters of the construction materials employed and the shape, size, and arrangement of the parts without departing from the scope of the present invention. It is intended that the specification and depicted embodiment be considered exemplary only, with a true scope and spirit of the invention being indicated by the broad meaning of the following claims.

CLAIMS

1. A method for connecting an integrated circuit chip to a circuit substrate, the integrated circuit chip including a bumped side having a plurality of conductive bumps, the method comprising the steps of:
   - applying adhesive directly to the bumped side of integrated circuit chip,
   - removing portions of the adhesive to expose contact regions of the conductive bumps, and
   - placing the bumped side of the integrated circuit chip against the circuit substrate such that the bumps provide for an electrical connection between the integrated circuit chip and the circuit substrate, and the adhesive forms a bond between the integrated circuit chip and the circuit substrate,

   characterized in that
   - the portions of adhesive are removed by softening the adhesive with a solvent and wiping the softened adhesive from the conductive bump.

2. The method of claim 1, wherein after removing the portions of adhesive, the exposed contact regions of the conductive bumps have a rounded profile.

3. The method of claim 1, wherein after removing the portions of adhesive, the conductive bumps have heights greater than a thickness of the adhesive.

4. The method of claim 1, wherein a portion of the adhesive is removed to create an offset between the exposed contact regions of the conductive bumps and a primary exposed surface of the adhesive.

5. The method of claim 1, wherein the adhesive is applied to the integrated circuit chip by a technique selected from the group of coating the adhesive as a hot melt, coating the adhesive from solution, bonding the adhesive as a film in a lamination process, and pressing the adhesive as a film onto the bumped side of the integrated circuit chip.

6. The method of claim 1, wherein prior to removing the portions of adhesive, the conductive bumps have heights that are greater than a thickness of the adhesive.

7. The method of claim 1, wherein prior to removing the portions of adhesive, the conductive bumps have heights that are smaller than a thickness of the adhesive.

8. A method for manufacturing integrated circuit chips comprising the steps of:
   - providing a wafer including a bumped side having a plurality of conductive bumps,
   - applying adhesive to the bumped side of the wafer, such that the conductive bumps are over-coated with adhesive, and
   - dicing the wafer on which the adhesive has been applied into individual integrated circuit chips,

   characterized by the following further steps performed after applying the adhesive and prior to dicing the wafer:
   - softening the adhesive with a solvent, and
   - wiping the softened adhesive from the tips of the over-coated conductive bumps to expose contact regions of the conductive bumps.

9. The method of claim 8, wherein after wiping the softened adhesive from the tips of the over-coated conductive bumps, the exposed contact regions of the conductive bumps have a rounded profile.

10. The method of claim 8, wherein the adhesive is applied to the wafer by a technique selected from the group of coating the adhesive as a hot melt, coating the adhesive from solution, bonding the adhesive as a film in a lamination process, and pressing the adhesive as a film onto the bumped side of the wafer.

11. The method of claim 8, wherein prior to removing the overcoat portions of adhesive, the conductive bumps have heights that are greater than a thickness of the adhesive.

12. The method of claim 8, wherein prior to removing the overcoat portions of adhesive, the conductive bumps have heights that are smaller than a thickness of the adhesive.

13. The method of claim 8, wherein after removing the overcoat portions of adhesive, the conductive bumps have heights greater than a thickness of the adhesive.

14. The method of claim 8, wherein after removing the overcoat portions of the adhesive, an offset exists between the exposed contact regions of the conductive bumps and a primary exposed surface of the adhesive.

15. The method of claim 8, wherein after the overcoat portions of adhesive are removed, and prior to dicing the wafer, a protective cover is placed over the adhesive and exposed contact regions.

16. An integrated circuit chip comprising:

a bumped side having a passivation surface on which a plurality of conductive bumps are disposed, wherein the conductive bumps are selected from the group consisting of: solder, meltable solid metals, gold, electroless nickel, electroless gold, and combinations thereof, and wherein said conductive bumps are metallurgically bonded to said integrated circuit chip; and

a layer of adhesive that covers the bumped side of the integrated circuit chip, the adhesive having a primary surface that is substantially parallel to the passivation surface, and the conductive bumps having exposed contact regions that are not covered by the adhesive, wherein the exposed contact regions of the conductive bumps have a rounded profile.

17. The integrated circuit chip of claim 16, wherein the primary surface of the adhesive is polished.

18. The integrated circuit chip of claim 16, wherein the conductive bumps have heights greater than a thickness of the adhesive.

19. The integrated circuit chip of claim 16, wherein portions of the conductive bumps project outward from the primary surface of the adhesive such that a stand-off exists between the rounded profile of the conductive bumps and the primary surface of the adhesive.