

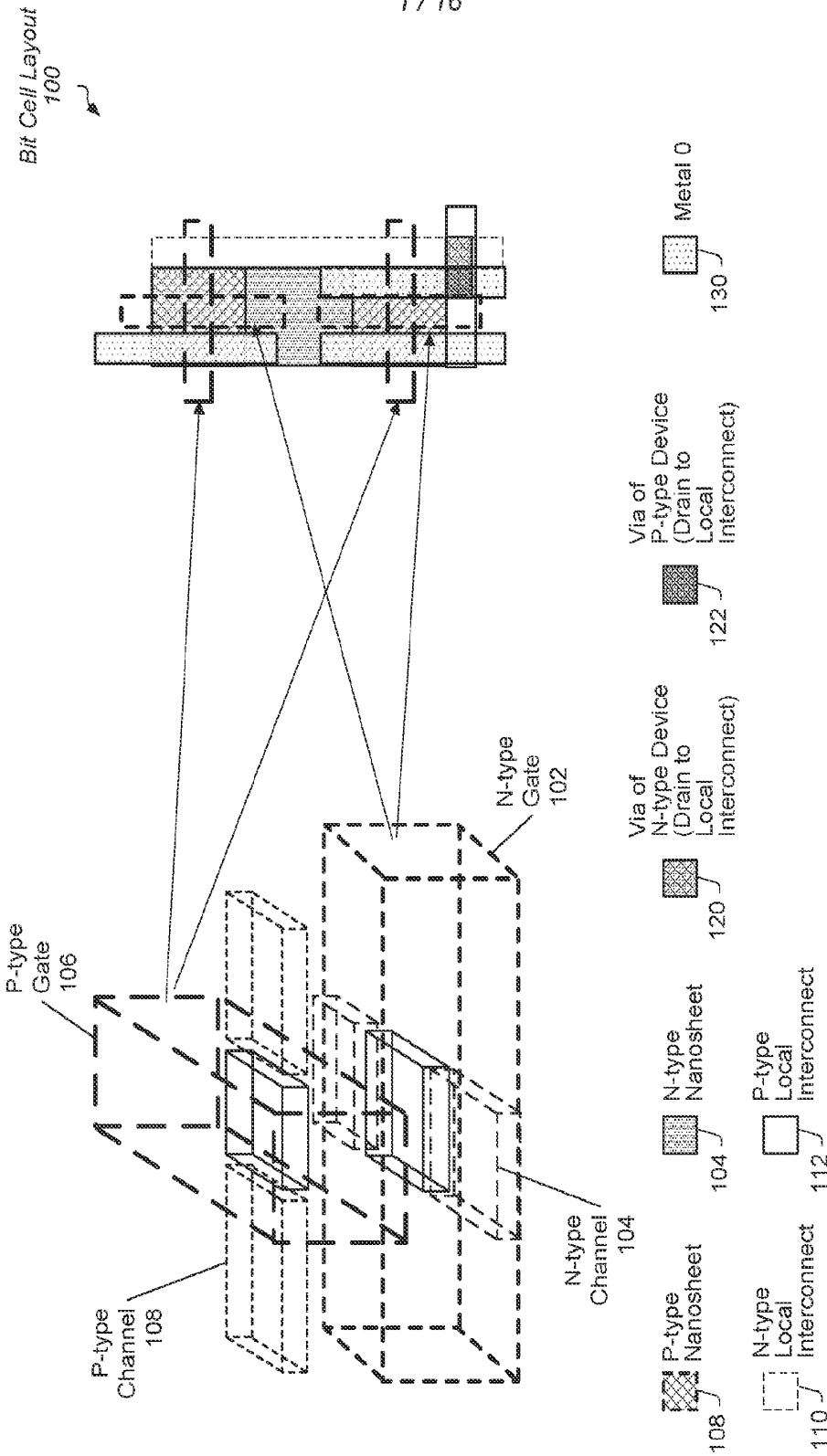


FIG. 1

Bit Cell Layout
200

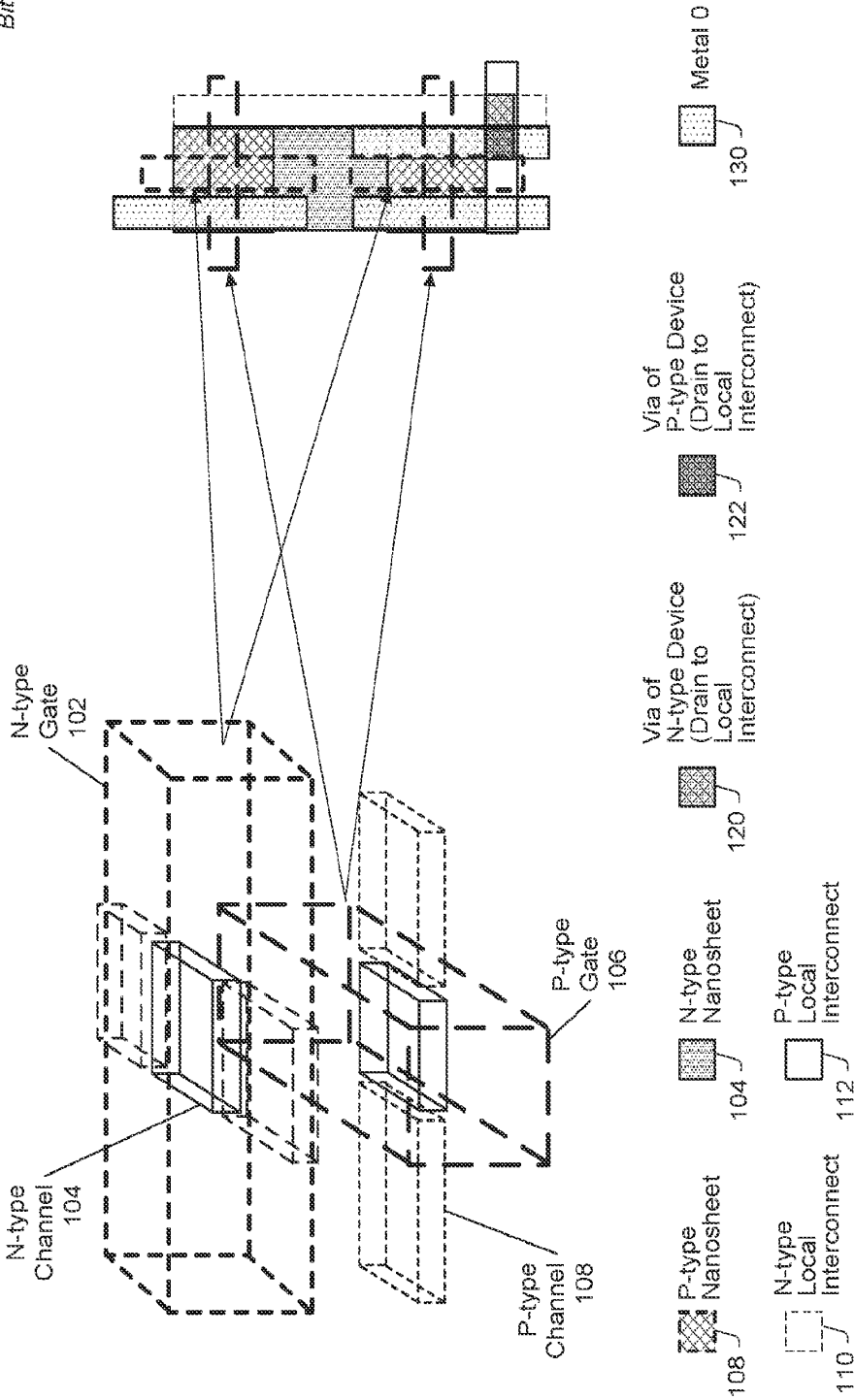
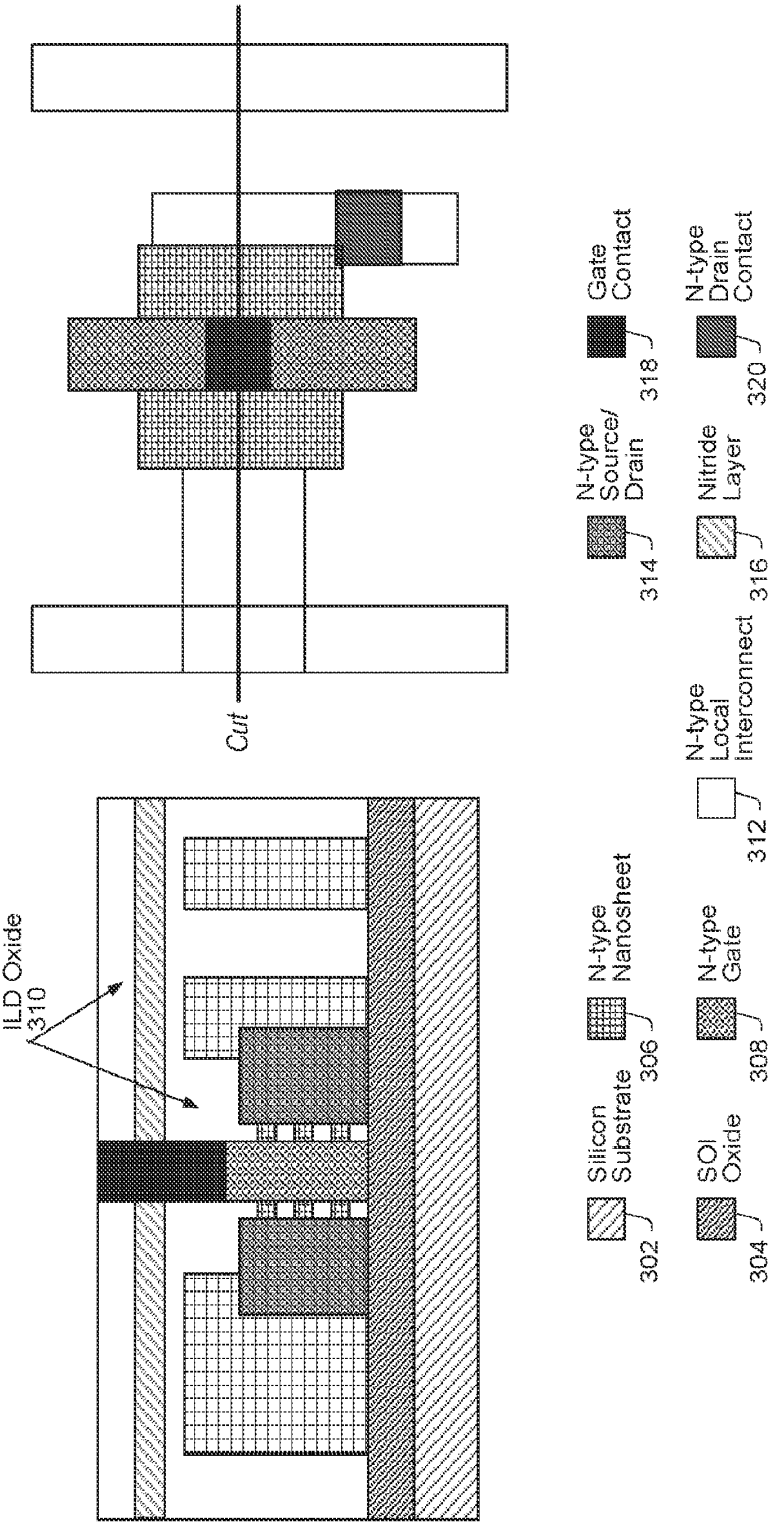


FIG. 2

Standard Cell Layout 300

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Standard Cell Layout 400

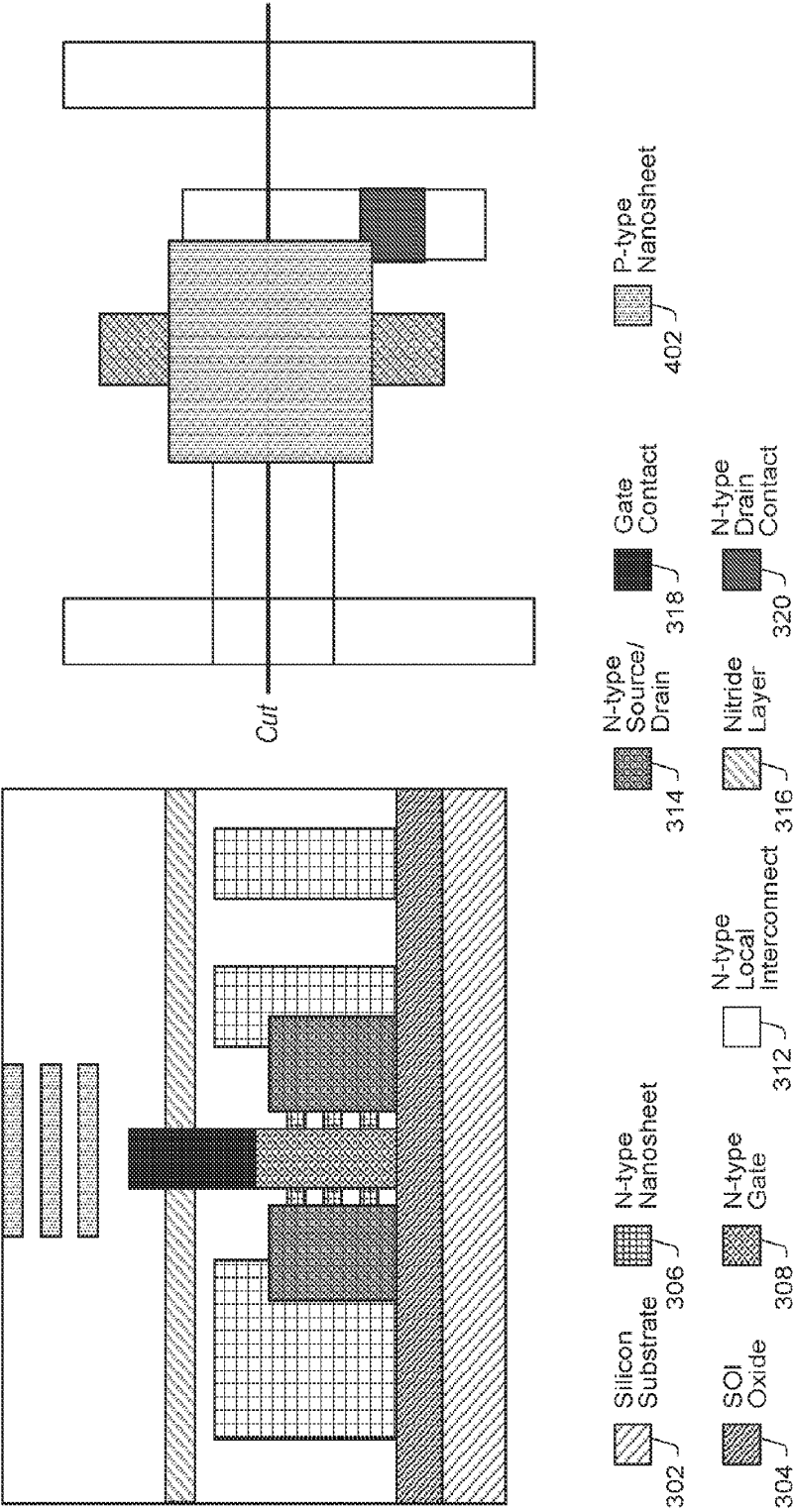


FIG. 4

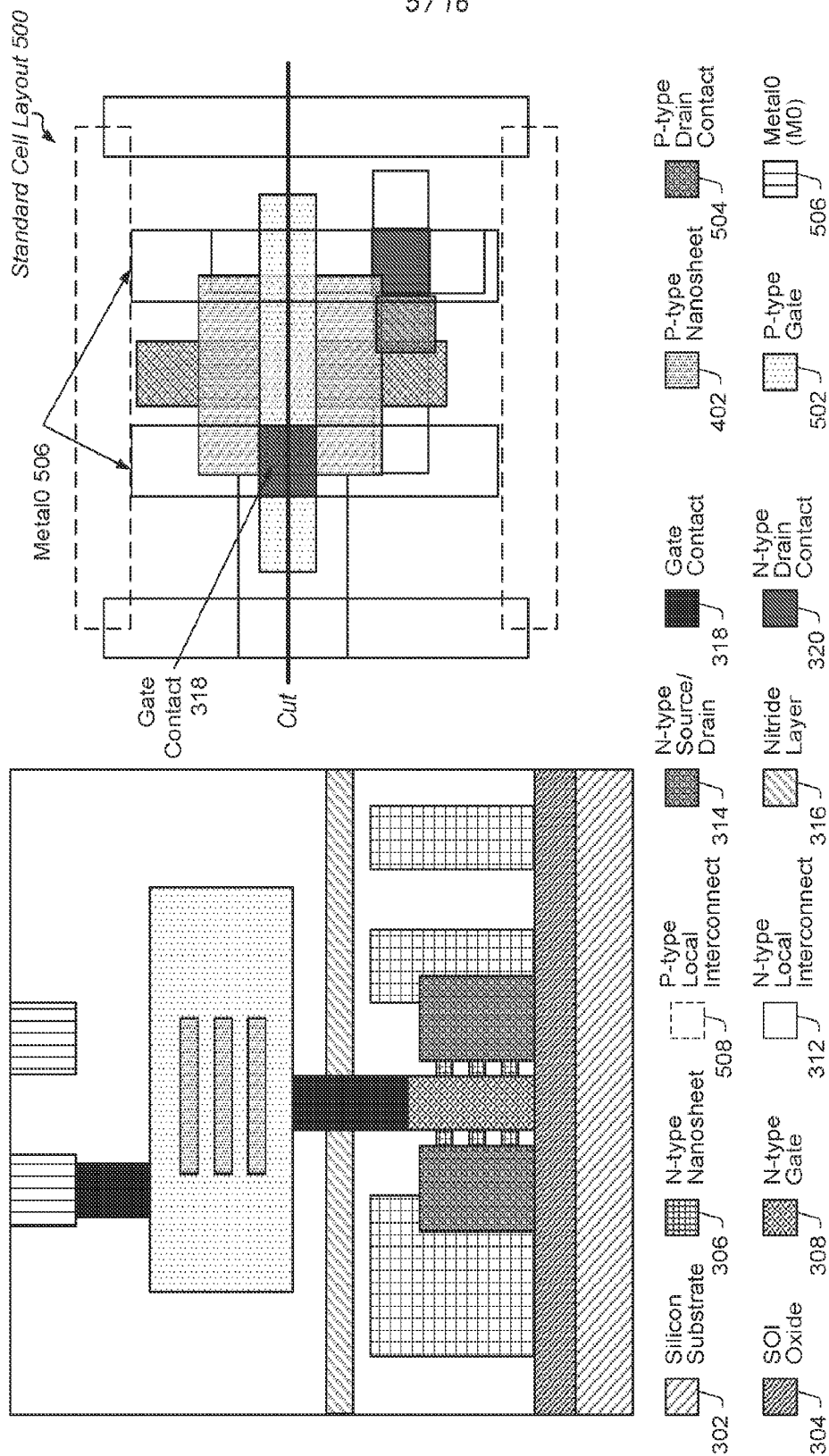


FIG. 5

Boolean NAND Logic Gate 600

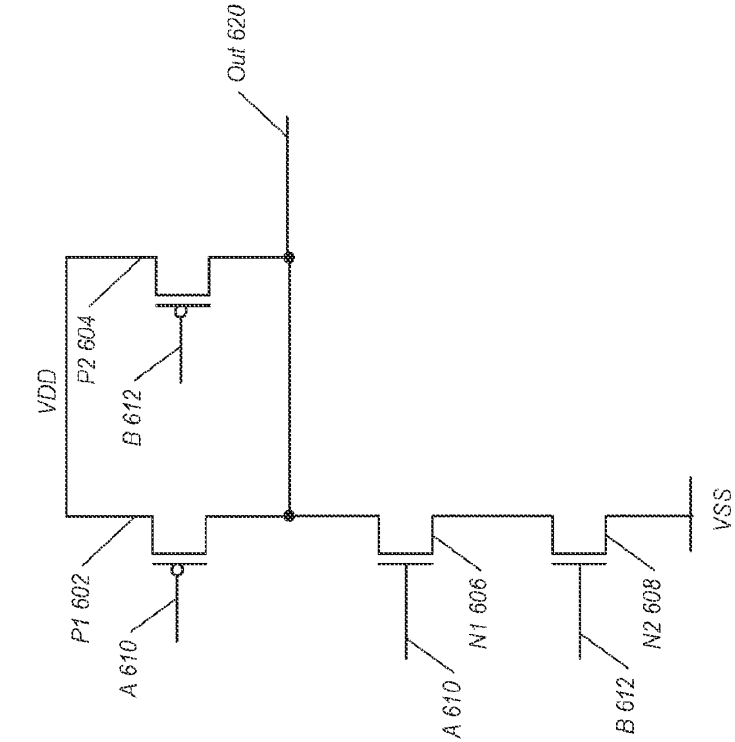


FIG. 6

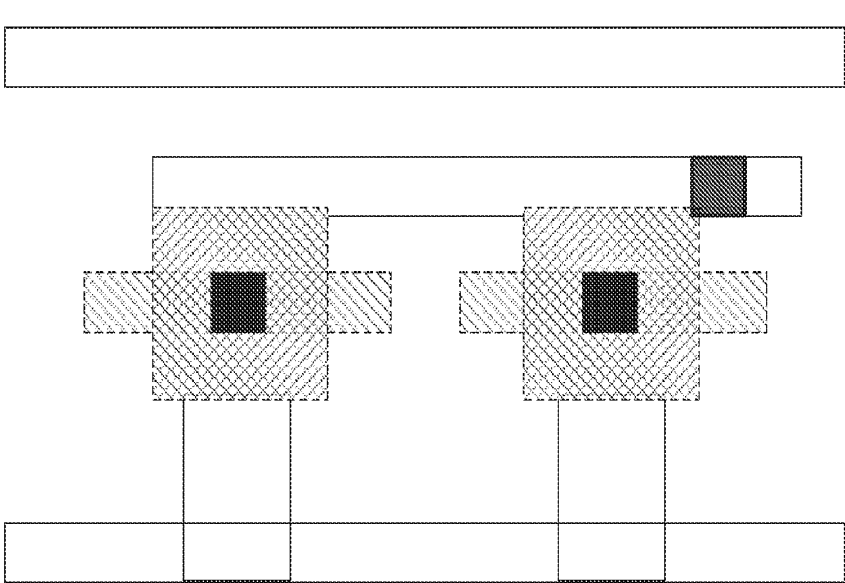
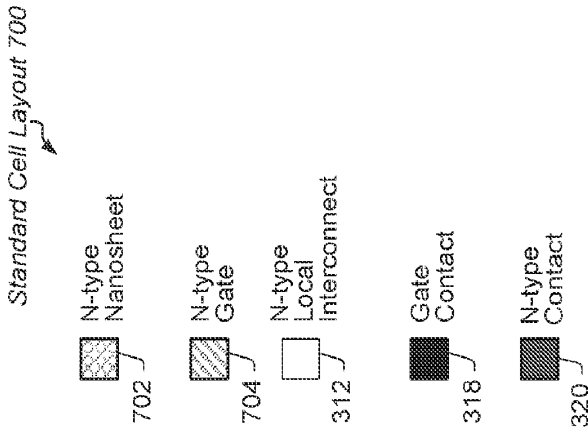


FIG. 7

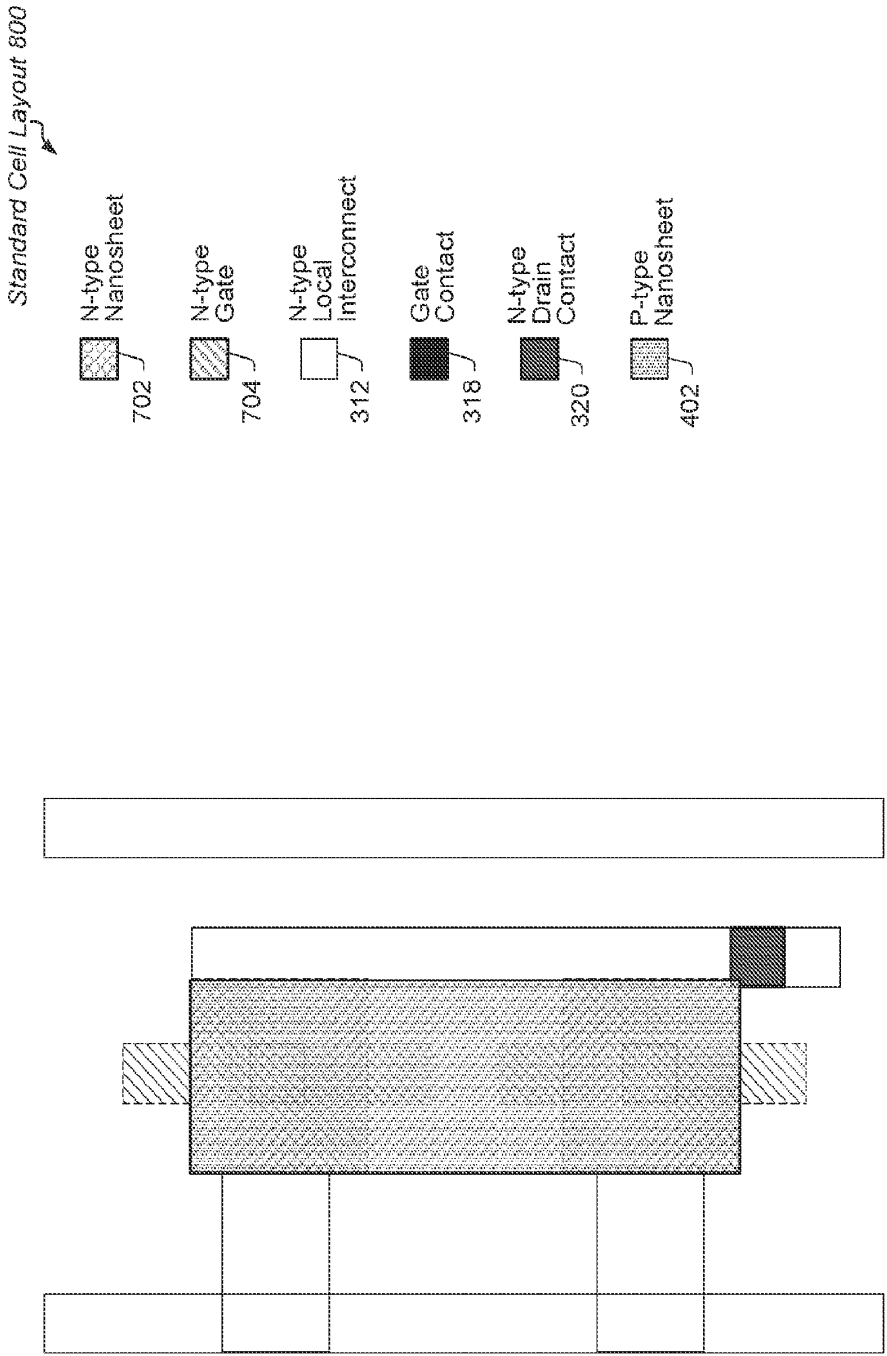


FIG. 8

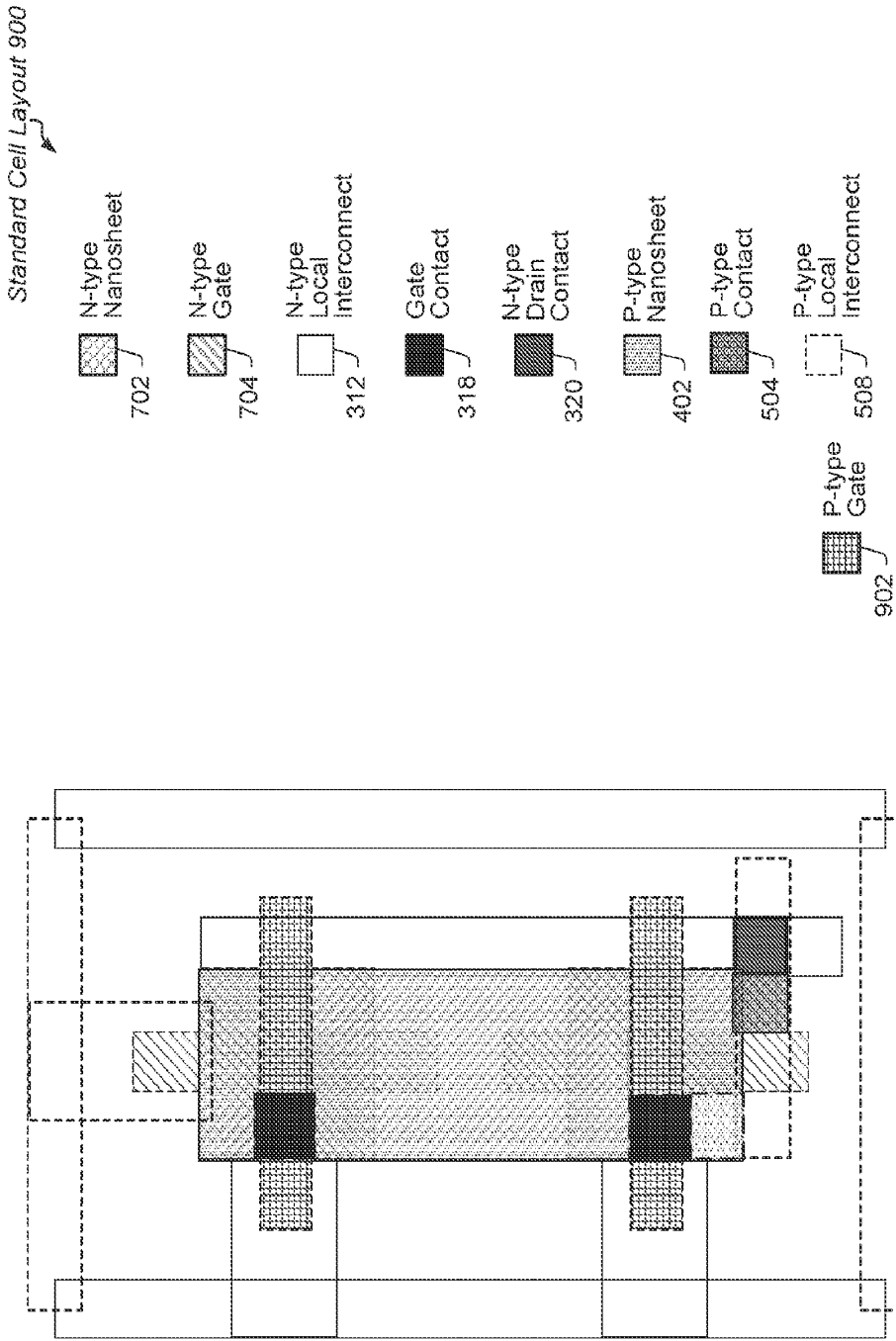


FIG. 9

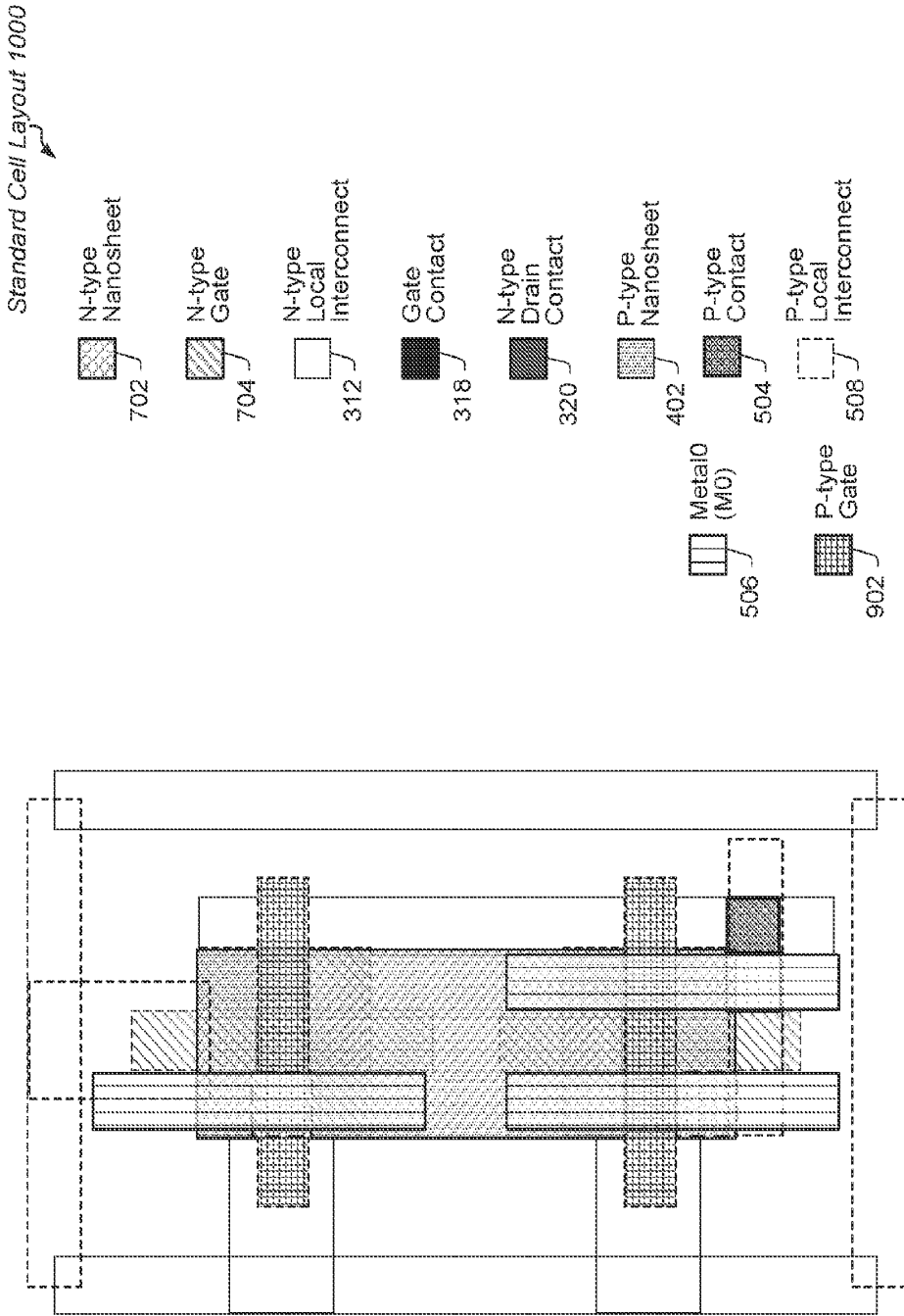


FIG. 10

Multiplexer Gate 1100

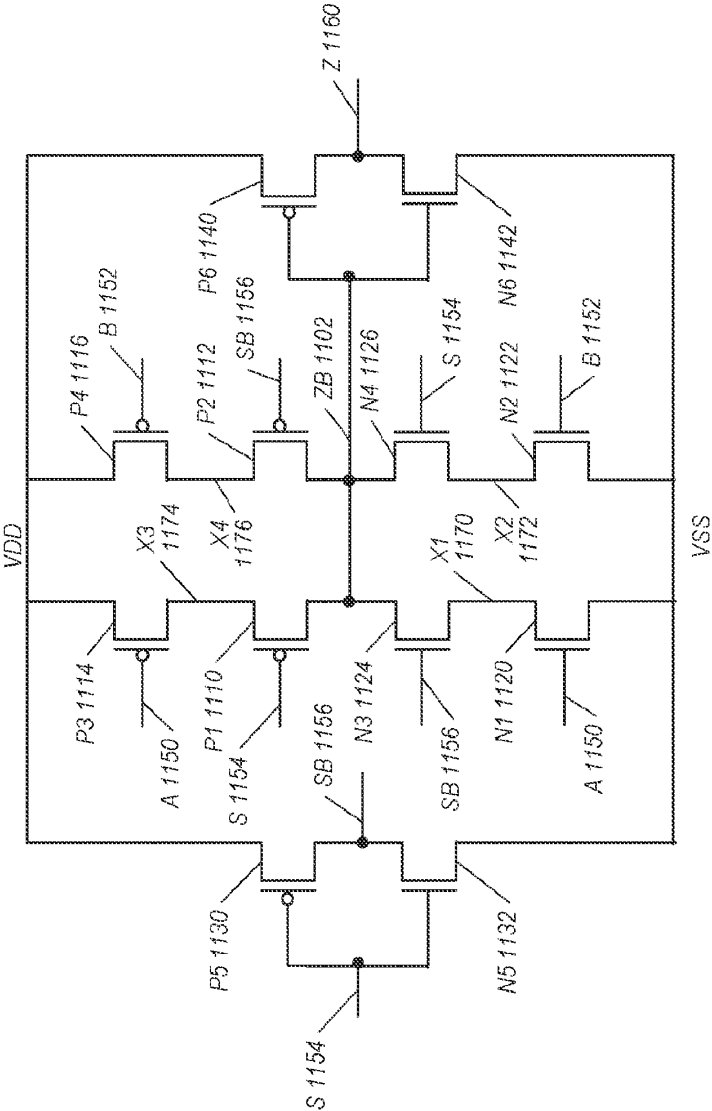


FIG. 11

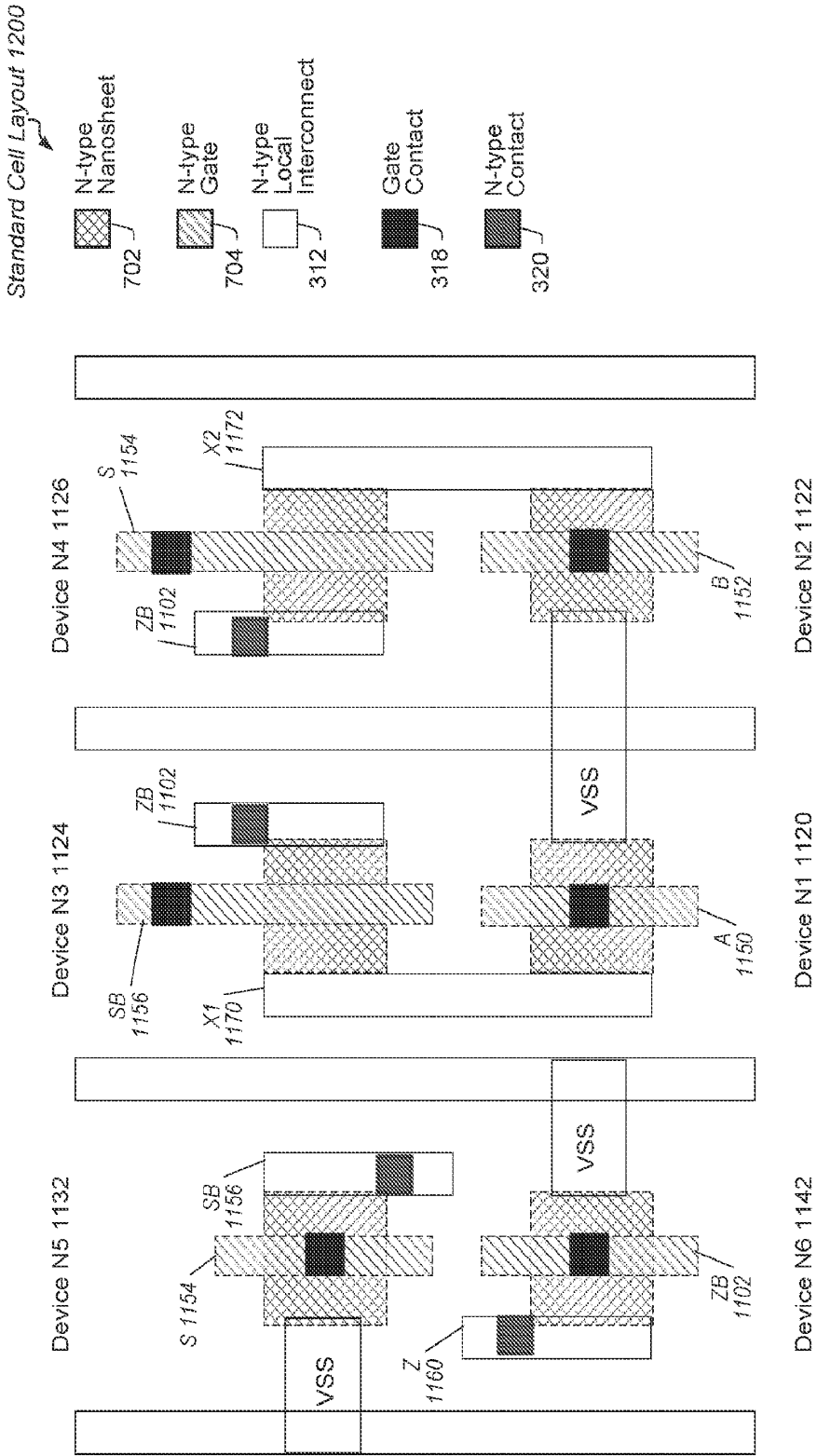


FIG. 12

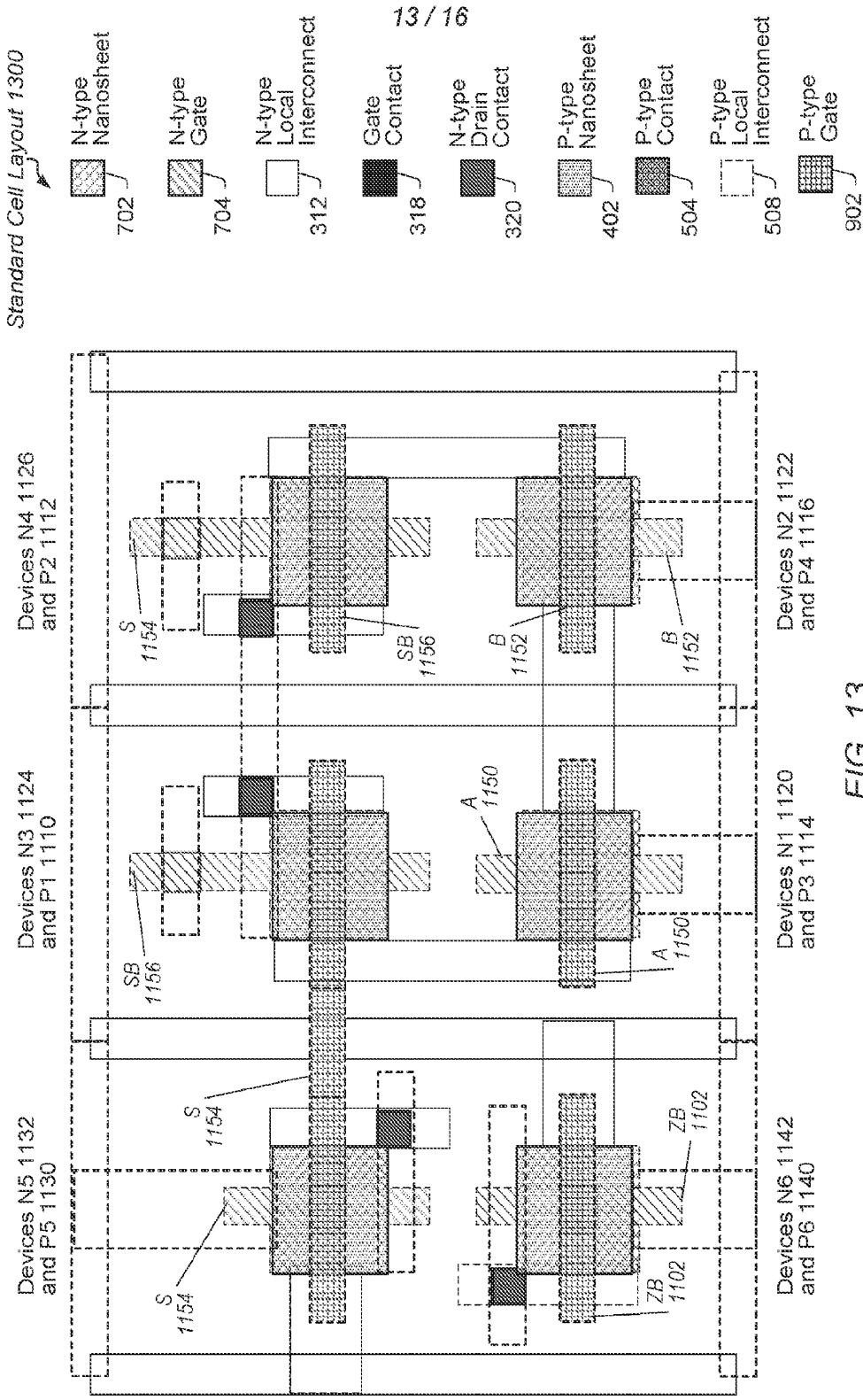


FIG. 13

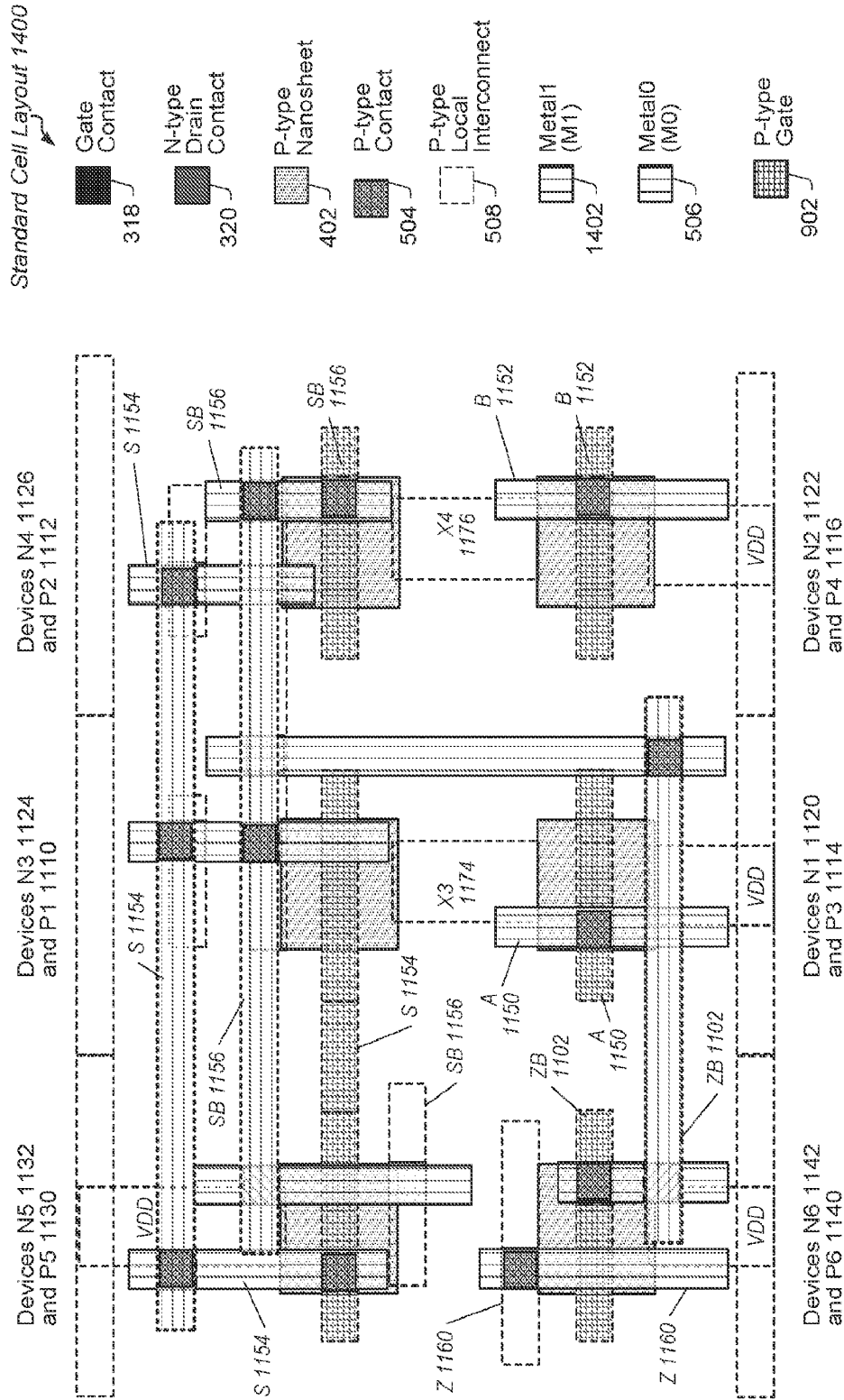


FIG. 14

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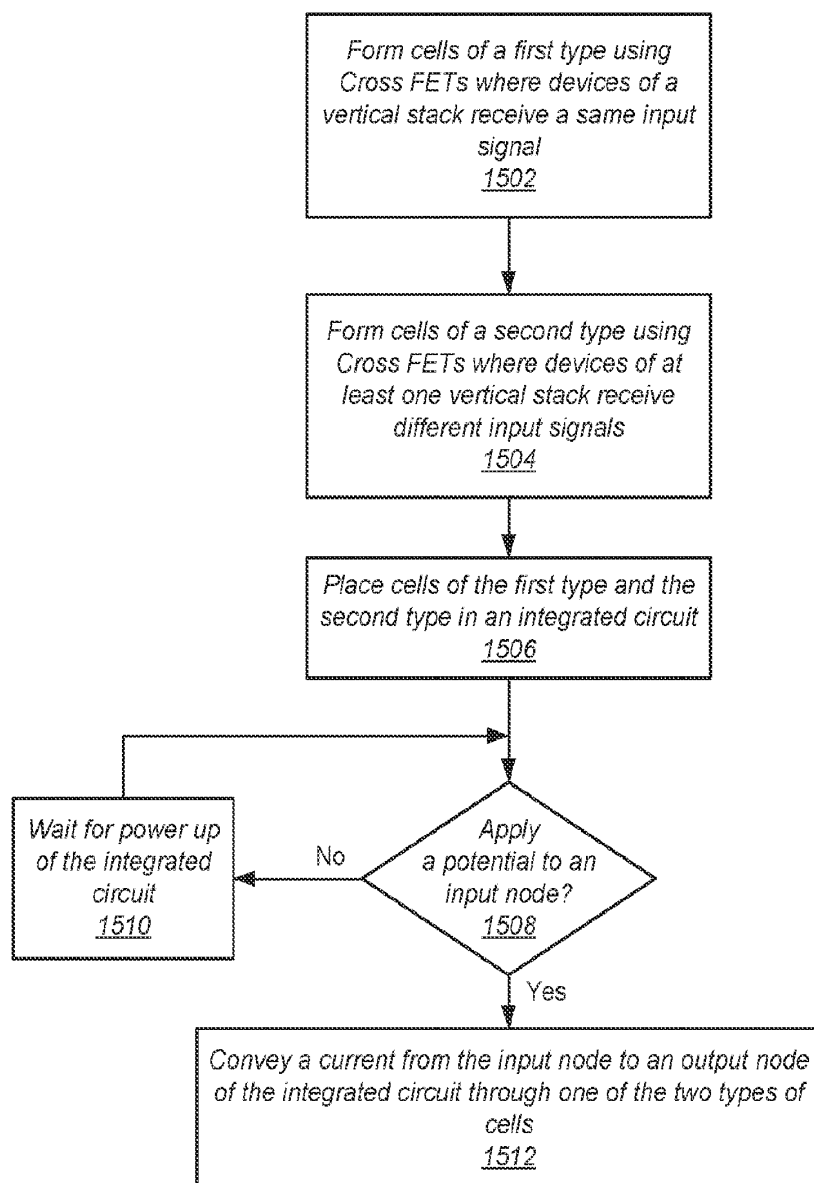
Method
1500

FIG. 15

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Computing System
1600

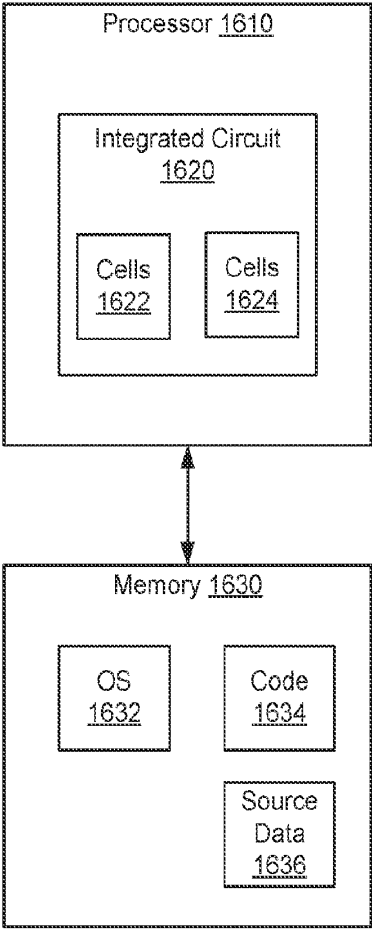


FIG. 16
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