What is claimed is:

1. A method for fabricating an integrated circuit, the method comprising: providing a substrate having a frontside and a backside; depositing a frontside metal layer on the frontside of the substrate; forming a via in the substrate; depositing a backside metal layer onto the backside of the substrate and into the via such that a portion of the backside metal layer is connected to a portion of the frontside metal layer; depositing a diffusion barrier onto the backside metal layer located in the via, the diffusion barrier substantially maintaining a shape of the vial forming first and second areas of active and/or passive components located on the frontside of the substrate and separated by the via, wherein the frontside metal layer includes interconnects to connect the components of the first and second areas of active and/or passive components; forming a solder layer over the diffusion barrier and the via; and forming a ground plane over the solder layer, wherein a path to the ground plane includes the solder layer, the diffusion barrier, the backside metal layer and the frontside metal layer.

2. The method of claim 1, wherein the diffusion barrier comprises a nickel (Ni) layer.

3. The method of claim 1, wherein the diffusion barrier comprises at least one of tantalum nitride, tungsten nitride, titanium nitride, and chromium.

4. The method of claim 1, wherein the diffusion barrier is oxidized to form a solder wetting barrier.

5. The method of claim 1, further comprising depositing a solder layer upon the diffusion barrier filling only a portion of the via.

6. The method of claim 1, further comprising: depositing a thin layer of adhesive material between the frontside metal layer and the backside metal layer.

7. The method of claim 1, wherein the depositing the diffusion barrier comprises patterning the diffusion barrier over the backside metal layer.

8. The method of claim 1, wherein the backside metal layer comprises breaks proximate an end of the via corresponding to the backside of the substrate, and further including depositing the diffusion barrier into the breaks.

9. The method of claim 1, wherein the frontside metal layer comprises gold.

10. The method of claim 1, wherein the backside metal layer comprises gold.

11. An integrated circuit comprising: a substrate having a frontside and a backside; a frontside metal layer deposited on the frontside of the substrate; a backside metal layer deposited onto the backside of the substrate and into a via formed in the substrate, wherein a portion of the backside metal layer is connected to a portion of the frontside metal layer; a diffusion barrier deposited onto the backside metal layer located in the via, wherein the diffusion barrier substantially maintains a shape of the via; first and second areas of active and/or passive components located on the frontside of the substrate and separated by the via, wherein the frontside metal layer includes interconnects to connect the components of the first and second areas of active and/or passive components; a solder layer over the diffusion barrier and the via; and a ground plane over the solder layer, wherein a path to the ground plane includes the solder layer, the diffusion barrier, the backside metal layer and the frontside metal layer.

12. The integrated circuit of claim 11, wherein the diffusion barrier comprises a nickel (Ni) layer.

13. The integrated circuit of claim 11, wherein the diffusion barrier comprises at least one of tantalum nitride, tungsten nitride, titanium nitride, and chromium.

14. The integrated circuit of claim 11, wherein the diffusion barrier is oxidized to form a solder wetting barrier.

15. The integrated circuit of claim 11, wherein the solder layer deposited upon the diffusion barrier fills a portion of the via.

16. The integrated circuit of claim 11, further comprising: a thin layer of adhesive material deposited between the frontside metal layer and the backside metal layer.

17. The integrated circuit of claim 11, wherein the frontside metal layer comprises gold.

18. The integrated circuit of claim 11, wherein the backside metal layer comprises gold.

19. The integrated circuit of claim 11, wherein the backside metal layer includes a stop at the backside of the substrate.