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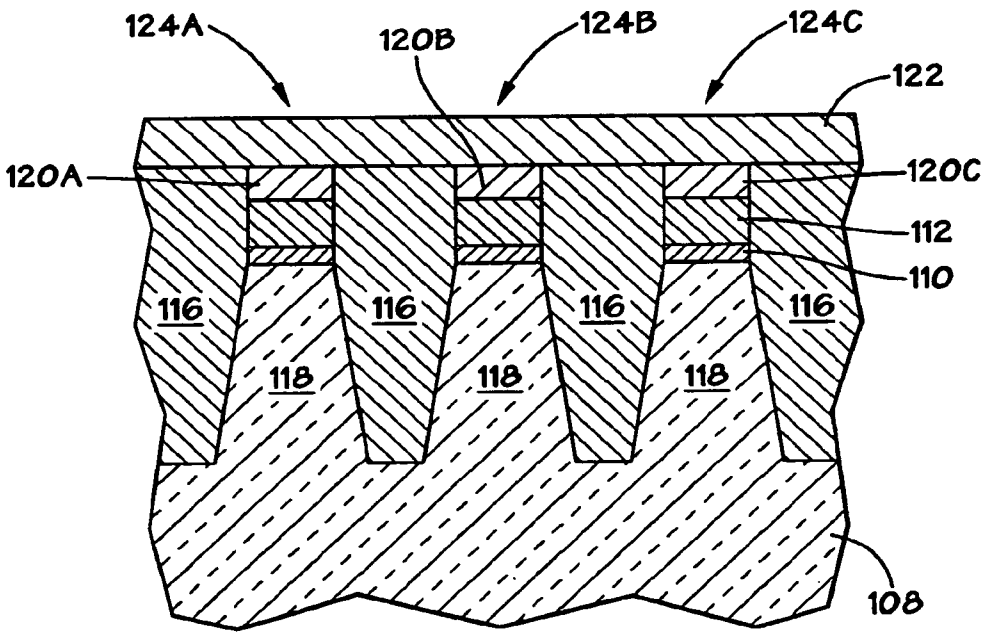
Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) Title: MEMORY DEVICES HAVING REDUCED INTERFERENCE BETWEEN FLOATING GATES AND METHODS OF FABRICATING SUCH DEVICES



(57) Abstract: A floating gate memory array comprising transistors having isolated inter-gate dielectric regions with respect to one another and methods of fabricating the same. Floating gate transistors are formed such that each of the floating gate transistors in the array has a floating gate, a control gate and an inter-gate dielectric layer therebetween. The inter-gate dielectric layer for each transistor is isolated from the inter-gate dielectric of each of the other transistors in the array. Methods of fabricating such structures are also provided.

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