Method for the double-side polishing of a semiconductor wafer

The invention relates to a method for the double-side polishing of a semiconductor wafer.

In particular, the invention is directed to double-side polishing of semiconductor wafers of the next technology generations, primarily of wafers which have a diameter of 450 mm. At the present time, predominantly polished or epitaxially coated silicon wafers having a diameter of 300 mm are used for the most demanding applications in the electronics industry. Silicon wafers having a substrate diameter of 450 mm are in development.

However, the enlargement of the substrate diameter is accompanied by major, in some instances also totally new, hitherto unknown technical problems.

Many processing steps, whether they are of purely mechanical (sawing, grinding, lapping), chemical (etching, cleaning) or chemical-mechanical nature (polishing), and also the thermal processes (epitaxial coating, annealing), require thorough revision, in part also with regard to the machines used therefor and the working materials.

Semiconductor wafers, after being sliced from a single crystal (ingot) composed of semiconductor material, are processed further in a multiplicity of process steps. After the grinding, cleaning and etching steps, in accordance with the prior art, the surface of the semiconductor wafers is smoothed by one or a plurality of polishing steps.

Obtaining a sufficiently good edge geometry and the surface flatness (nanotopology) are particularly critical in the manufacture of semiconductor wafers.

The nanotopology is usually expressed as height fluctuation PV (= "peak to valley"), relative to square measurement windows having an area of 2 mm × 2 mm.

The final nanotopology of a semiconductor wafer is generally produced by means of a polishing process.

In the case of single-side polishing (SSP), semiconductor wafers are held during processing on the rear side on a support plate by means of cement, a vacuum or by means of adhesion and are subjected to polishing on the other side.

In the case of double-side polishing (DSP), semiconductor wafers are inserted loosely into a thin carrier plate and are polished on the front and rear sides simultaneously in a "freely floating" manner between an upper and a lower polishing plate each covered with a polishing pad. This polishing method is effected with the supply of a polishing agent slurry, usually based on a silica sol.

The prior art likewise discloses polishing using fixedly bonded abrasives ("Fixed Abrasive Polishing", FAP), wherein the semiconductor wafer is polished on a polishing pad which, in contrast to other polishing pads, contains an abrasive substance bonded in the polishing pad ("Fixed Abrasive" or FA pad). The German Patent Application DE 10 2007 035 266 A1 describes a method for polishing a substrate composed of silicon material, using FA pads.

After DSP or FAP, the front sides of the semiconductor wafers are generally polished in a haze-free manner. As is usually effected using a softer polishing pad with the aid of an alkaline polishing sol. In the literature, this step is often designated as chemical mechanical polishing (CMP). CMP methods are disclosed, for example, in US 2002-0077039 and in US 2008-0305722.

By comparison with single-side polishing (SSP), simultaneous double-side polishing (DSP) of semiconductor wafers is not only more economic, but higher flatness with regard to the surfaces of the semiconductor wafers is obtained as well.

Double-side polishing is described, for example, in US 3,691,694. A suitable double-side polishing machine is disclosed in DE 100 07 390 A1. In accordance with one embodiment of double-side polishing as described in EP 0 208 315 B1, semiconductor wafers in carrier plates composed of metal or plastic, which have suitably dimensioned cutouts, are moved between two rotating polishing plates covered with a polishing pad in the presence of a polishing agent (polishing sol) on a path predetermined by the machine and process parameters and are thereby polished (in the literature, carrier plates are designated as "templates").

The double-side polishing step is usually carried out using a polishing pad composed of homogeneous, porous polymer foam having a hardness of 60 to 90 (Shore A), as described for example in DE 100 04 578 C1, where it is also disclosed that the polishing pad adhering to the upper polishing plate is pervaded by a network of channels and the polishing pad adhering to the lower polishing plate has a smooth surface without such a texture. This measure is intended firstly to ensure a homogeneous distribution of the polishing agent used during polishing and secondly to prevent the semiconductor wafer from adhering to the upper polishing pad when the upper polishing plate is raised after polishing has finished.

The upper polishing pad comprises a regular chequered arrangement of channels having a segment size of 5 mm x 5 mm to 50 mm x 50 mm and a channel width and depth of 0.5 to 2 mm. This arrangement is used to effect polishing at a polishing

pressure preferably of 0.1 to 0.3 bar. The silicon removal rate is preferably between 0.1 and 1.5 μm/min and particularly preferably between 0.4 and 0.9 μm/min.

However, a procedure in accordance with DE 100 04 578 C1 results in an asymmetrical polishing removal at the outer edge of the semiconductor wafer at the opposite sides (rear side and front side).

A further cause of locally different polishing removals in the case of double-side polishing in accordance with the prior art is the fact that abraded material (semiconductor material, for example silicon or silicon oxide), removed from the surfaces of the semiconductor wafers in the polishing process covers (deposits on) the polishing pad surfaces to in part different extents. In particular, the regions of the polishing pad surface which come into contact with the surfaces of the semiconductor wafers during the polishing process the most often statistically in a defined time period are covered with abraded material. A ring-shaped area with abraded material often forms on the polishing pad surface.

The formation of regions covered with abraded material on the polishing pad surface is additionally fostered by a non-uniform polishing agent distribution in the working gap between polishing pad and carrier plate.

The areas of the polishing pad which are covered with abraded material constitute regions in which the pad is altered in terms of its texture and in terms of its composition near the surface. These regions therefore have different properties with regard to the polishing result in comparison with the regions which are affected to a lesser extent or not at all by covering with abraded material.

As polishing pad covering increases, it becomes more and more difficult to control the polishing machines in such a way that flat wafers having good geometry values (GBIR, wafer shape, edge roll-off) are produced. Furthermore, it is necessary to reckon with an increase in the micro roughness (haze values) of the wafers. The risk of polishing scratches and increased LLS values on the polished wafer surfaces likewise increases in a similar manner.

Regular polishing pad conditioning that becomes necessary as a result reduces the lifetime of the polishing pads (wear) and additionally adversely impairs - on account of the mechanical action on the polishing pad and the associated change in the polishing pad (thickness, pad structure, ...) - the wafer geometry and form.

A further cause of the non-uniform polishing removal is, inter alia, a polishing agent distribution effected non-uniformly on the polishing pad and, as a consequence thereof, a non-uniform wetting of the surfaces to be polished with polishing agent, or application of polishing agent to said surfaces.

In accordance with the prior art, the polishing agent distribution is effected by gravitational force and centrifugal force. The polishing agent is introduced from above into the working gap between polishing pad and carrier plate and flows on account of the gravitational force inter alia through the cutouts for the semiconductor wafers in the carrier plate also onto the lower polishing pad. In this case, the polishing agent distribution is fostered by the rotational movement of the carrier plates and of the polishing plates covered with the polishing pads.

The uniform polishing agent distribution is impeded by the carrier plate, in particular with regard to the polishing pad

regions lying below the carrier plate. In order to improve the polishing agent distribution, US 2006-178089 A discloses a carrier plate having a multiplicity of round openings through which the polishing agent reaches the lower polishing pad.

The teaching of EP 1 676 672 A1 includes improving the supply of polishing agent to the lower polishing plate by at least 15% of the area of the carrier plate being occupied by holes that provide for the polishing agent a passage to the lower polishing plate.

However, these additional "polishing agent cutout" in the circular carrier plates reduce the area moment of inertia thereof and, as a consequence thereof, also the resistance thereof to torsion. That is disadvantageous since the risk of carrier plate warping is thereby increased. The warping of the carrier plate can lead to pad damage, reduced pad lifetime, particle generation, polishing scratches through to wafer fracture and damage to the installation.

On account of the further increasing surface area in semiconductor wafers of future generations, for example having a diameter of 450 mm, the uniform polishing agent distribution (application of polishing agent) can be realized only to a limited extent during the polishing process in accordance with the prior art.

The objective of the present invention emerges from this problem area. The aim of the invention is to ensure the uniform application of polishing agent to the polishing pad surfaces during the simultaneous double-side polishing of semiconductor wafers, without impairing the stability of the carrier plate. The object of the invention is achieved by means of a method for the simultaneous double-side polishing of at least one wafer composed of semiconductor material which is situated in a

suitably dimensioned cutout in a carrier plate and which has a front side and a rear side, and the double-side polishing is effected between an upper polishing plate covered with a first polishing pad and a lower polishing plate covered with a second polishing pad, with a polishing agent being supplied, wherein the surfaces of the first (upper) and of the second (lower) polishing pad are in each case interrupted by at least one channel-shaped depression running spirally from the center to the edge.

The method according to the invention and preferred embodiments will be described and explained in detail, by means of figures 1 to 2.

Figure 1 shows spiral forms used in the method according to the invention: (a) logarithmic spiral, (b) Archimedes' spiral, (c) Fermat's spiral, (d) triple spiral.

Figure 2 shows a preferred embodiment of the carrier plate (1) modified according to the invention with the segmented polishing agent passages (2) interrupted by the three webs (4), and the suitably dimensioned cutouts (3) for the wafers (5) composed of semiconductor material, wherein the cutouts (3) for the wafers (5) composed of semiconductor material are surrounded by the segmented polishing agent passages (2) at a distance A. In this preferred embodiment, the webs (4) are arranged such that the respective centers of the three webs (4) are at an angle of 120° with respect to one another.

The process according to the invention includes not just a partial aspect restricted to a specific technical component or an individual process-technological aspect (e.g. of individual process parameters), but encompasses associated process features. These process features are subdivided into

1) Polishing pads having a specific surface structure,
2) Reconfiguration of the carrier plates for wafer accommodation and
3) Polishing agent supply effected on both sides.

For the process according to the invention for the simultaneous double-side polishing (DSP) of a wafer composed of semiconductor material, as polishing agent in accordance with the prior art use is made of a silica sol, a slurry comprising colloidally distributed particles having a size of 20 to 50 nm, as polishing agent.

The polishing agent distribution during DSP is influenced, inter alia, by the properties of the polishing pad surface (working surface) which comes into contact in a material-removing manner with the front and/or rear side of the semiconductor wafer during the polishing process. Both the absorbency for the polishing agent and the structure (channels, depressions, grooves) influence the polishing agent distribution during DSP, as is described for example in DE 100 04 578 C1.

In accordance with the prior art, circular polishing pads composed of homogeneous, porous polymer foam having a hardness of 60 to 90 (Shore A) are used for the method according to the invention.

In a first embodiment of the method according to the invention for the simultaneous double-side polishing of wafers composed of semiconductor material, the upper and the lower polishing plate are covered with circular polishing pads, the working surface of which is provided with at least one channel (depression, groove) running spirally.

A spiral channel is a depression that runs circularly around a start point and depending on the running direction (orientation), leads away from said point or approaches said point. The distance between two spiral channels (distance W between the turns) can be constant (Archimedes' spiral (figure 1b)) or - as viewed from the start point - can become continuously greater (logarithmic spiral (figure 1a)).

A special form of spiral is the triple spiral, which consists of three Archimedes' spirals arranged circularly around a midpoint and whose lines, after a finite number of turns, form a circular form enclosing the three spirals (figure 1d).

For the method according to the invention for the simultaneous double-side polishing of wafers composed of semiconductor material, use is preferably made of polishing pads having at least one channel running spirally from the inner portion (middle or center of the polishing pad) toward the outer portion (edge of the polishing pad) on the working surface, characterized in that the distance W between the turns of the at least one spiral channel becomes continuously greater from the inner portion toward the outer portion (logarithmic spiral, figure 1a).

For the method according to the invention for the simultaneous double-side polishing of wafers composed of semiconductor material, preference is likewise given to using polishing pads having channels running spirally from the inner portion toward the outer portion on the working surface, characterized in that the distance W between the turns of the channels becomes continuously smaller from the inner portion toward the outer portion (Fermat's spiral, figure 1c).

Particularly preferably, for the method according to the invention for the simultaneous double-side polishing of wafers

composed of semiconductor material, use is made of polishing pads having channels running spirally from the inner portion toward the outer portion on the working surface, characterized in that the distance W between the turns of the channels is constant (Archimedes' spiral, figure 1b).

The distance W between turns between two spiral channels on the polishing pad surface is chosen such that - independently of the diameter of the circular polishing pad - the spiral has at least 3 turns.

Preferably, a spirally arranged channel running from the center of the polishing pad (start point) spirally to the edge region of the polishing pad is situated in the surface of the polishing pad. In this case, the end point of this spiral depression can reach as far as the edge of the polishing pad.

In a likewise preferred embodiment of the method according to the invention, two or more spirally arranged channels running from the center of the polishing pad (start point) to the edge thereof are situated in the surface of the polishing pad.

In this embodiment, particular preference is given to polishing pads whose working surface has in an inner circular region around the midpoint of the circular polishing pad having a radius R three channels running spirally from the center of the polishing pad toward the edge, wherein, in a ring-shaped outer region (edge region) of the polishing pad surface, having a thickness D, the three spiral channels merge into a circular course (triple spiral, figure 1d).

The radius R of the inner circular region of the polishing pad surface is preferably greater than or equal to two thirds of the radius of the circular polishing pad. In this case, the thickness D of the outer ring-shaped region is preferably less

than or equal to one third of the radius of the circular polishing pad and results from the difference in the outer radius of the ring-shaped edge region minus the inner radius of the ring-shaped edge region.

The spiral channels have a preferred depth of 0.5 - 1.5 mm and a preferred width of 1 -5 mm. Particularly preferably, the spiral channels have a depth of 0.7 - 1.0 mm and a width of 1.5 - 3 mm.

Preference is likewise given to an enlargement of the width of the spiral channels from the inner portion toward the outer portion, said enlargement running uniformly over the length of the channels from the start point to the end, wherein the width is preferably 2 mm at the beginning of the spiral channel (in the center of the circular polishing pad) and is preferably 4 mm at the end of the spiral channel (in the edge region or at the edge of the circular polishing pad).

By virtue of the greater width of the spiral channel on the working surface of the polishing pad in comparison with the width of the spiral channel in the pad center, the distribution of the polishing agent is additionally optimized.

According to the invention, the polishing agent distribution in the working gap can also be effected by an enlargement of the depth from the inner portion toward the outer portion, said enlargement running uniformly over the length of the spiral channel from the start point to the end thereof, wherein the depth is preferably 0.5 mm at the beginning of the spiral channel (in the center of the circular polishing pad) and is preferably 1 mm at the end of the spiral channel (in the edge region or at the edge of the circular polishing pad).

The inner form of the spiral channel preferably has a half-round form (U-profile). A rectangular inner form of the spiral channel is likewise preferred.

The edge that arises between the polishing pad surface and the depression formed by the spiral channel is preferably rounded.

Preferably, the channels arranged spirally into the surfaces of the polishing pads are oriented in the same sense. The use of spiral channels oriented in the same sense in the polishing pad surface - and thus the use of fundamentally identical polishing pads - is possible since the polishing plates face one another with their end sides - and thus also the active polishing pad surfaces - and upper and lower polishing plates rotate oppositely (diametrically oppositely).

By virtue of the centrifugal force that arises upon the rotation of the working disks respectively covered with a polishing pad according to the invention, the polishing agent is transported in the spiral channels from the inner portion toward the outer portion and is distributed uniformly in the working gap formed by the distance between the two polishing pad surfaces.

For further optimization of the polishing agent distribution during the DSP, in accordance with the method according to the invention, in addition to the use of the working surfaces of the polishing pads that are provided with spiral channels according to the invention, the carrier plates serving for accommodating and guiding the semiconductor wafers can also be configured.

A carrier plate used during DSP consists, in accordance with the prior art, of a round disk having one or a plurality of suitably dimensioned cutouts (3) into each of which a wafer (5)

composed of semiconductor material is inserted. In addition, carrier plates can have "polishing agent cutouts" through which the polishing agent introduced into the working gap from above passes to the lower polishing plate.

Independently of the respective embodiments of the method according to the invention, in the method according to the invention each wafer composed of semiconductor material is preferably placed into a suitably dimensioned round cutout in the carrier plate such that the front side of the wafer composed of semiconductor material is polished at the upper polishing pad.

In the second embodiment of the method according to the invention for the simultaneously double-side polishing of wafers composed of semiconductor material, modified carrier plates are used instead of the carrier plates in accordance with the prior art.

The carrier plate (1) modified according to the invention has at least one suitably dimensioned cutout (3) for accommodating a wafer (5) composed of semiconductor material, characterized in that the at least one suitably dimensioned cutout (3) is surrounded by at least one further cutout (2), acting as a polishing agent passage, at a distance A.

Preferably, the carrier plate (1) modified according to the invention has at least one suitably dimensioned circular cutout (3) for accommodating a wafer (5) composed of semiconductor material, characterized in that at least one circular cutout (3) is surrounded by three segmented cutouts (2) which have an identical size (relative to the area) and are separated by webs (4), with a distance among one another of in each case at most

110°, in a ring-shaped manner at a distance A from the circular cutout (3) (figure 2).

The preferred thickness of the segmented cutout (2), which results from the difference in the outer edge minus the inner edge, is 1 - 10 mm. Particularly preferably, the thickness of the segmented cutout (2) is 3 - 7 mm. The preferred distance A between the outer edge of the circular cutout (3) and the inner edge of the segmented cutouts (2) is constant and is 5 to 10 mm.

The segmented "polishing agent cutouts" (2) in the carrier plate (1) modified according to the invention do not influence the stability of the carrier plate.

In the carrier plate (1) modified according to the invention, a respective semiconductor wafer (5) can be inserted into a suitably dimensioned cutout (3) in the carrier plate (1) and positioned such that an inherent rotation of the semiconductor wafer (5) within the cutout (3) in the carrier plate (1) is possible during the polishing process.

In a further preferred embodiment of the carrier plate (1) modified according to the invention, the inherent rotation of the at least one semiconductor wafer (5) in the suitably dimensioned cutout (3) in the carrier plate (1) is prevented by the fixing of the semiconductor wafer (5) during the polishing process.

The fixing of the semiconductor wafer (5) in the suitably dimensioned cutout (3) in the carrier plate (1) can be effected, for example, with the aid of one or a plurality of so-called "notch fingers".

A "notch finger" is a protuberance for example in the suitably dimensioned cutout (3) in the carrier plate (1) which projects into a notch in the edge of the semiconductor wafer (5) and thus fixes the semiconductor wafer (5) in the cutout (3) in the carrier plate (1).

In the third embodiment of the method according to the invention for the simultaneous double-side polishing of wafers composed of semiconductor material, the polishing agent supply is effected simultaneously on the front side and on the rear side of the semiconductor wafer both through the upper and through the lower polishing plate.

For this purpose, the polishing agent supply is preferably effected in a pressurized manner through openings integrated in the polishing agent outlets of the two polishing plates such that the outlets terminate flush with the polishing plates.

Particularly preferably, the polishing agent supply is effected in a pressurized manner by means of nozzles integrated in the polishing agent outlets of the two polishing plates such that the nozzle outlets terminate flush with the polishing plates or end within the openings in the polishing plates.

The two circular polishing pads applied to the upper and lower polishing plates before the polishing process likewise have openings besides the spiral depressions, wherein the number and distribution of the openings on the polishing plate corresponds to the number and distribution of the openings in the polishing pad and the polishing pad is applied to the polishing plate in such a way that the polishing agent can pass through the openings from above and below into the working gap.

Preferably, the polishing agent outlets for the application of polishing agent are arranged circularly in the polishing plates

and pads. Particularly preferably, the polishing agent outlets are arranged in an inner circular and an outer ring-shaped region, wherein the radius R of the inner circular region of the polishing plate or polishing pad is preferably greater than or equal to two thirds of the radius of the circular polishing plate or polishing pad.

For further optimization of the polishing agent distribution, the quantity of the polishing agent emerging from the nozzles into the working gap per unit time in an inner circular region of the polishing pad can preferably be higher than the quantity that emerges in the same time from the nozzles situated in the outer ring-shaped region. As a result, an "aquaplaning" effect as a result of an excessively high quantity of polishing agent in the working gap can be counteracted in a targeted manner.

The different quantities of polishing agent per unit time can be set, for example, by means of different nozzle cross sections, nozzle types or by means of nozzles driven individually by pumps.

The nozzles for the polishing agent supply or the openings in the polishing plate or polishing pad are preferably perpendicular to the surface of the polishing plate or polishing pad. Particularly preferably, the nozzles for the polishing agent supply or the openings in the polishing plate or in the polishing pad have an angle, relative to the polishing pad surface, of from 45° to less than or equal to both 90°, wherein the openings are present in the upper and in the lower polishing plate and also in the upper and in the lower polishing pad.

In order to prevent the silica sol particles from crystallizing out (gelation) in the nozzles or lines of the polishing agent

supply, the nozzles are rinsed with water after the conclusion of the polishing process.

In order also to additionally optimize the polishing result with regard to homogenizing the polishing removal - a plane-parallel wafer initial geometry is a precondition here, however - the temperature of the polishing agent supplied ideally corresponds to the surface temperature of the polishing pads. This is achieved by corresponding temperature regulation of the polishing plates and of the polishing agent in accordance with the prior art. Preferably, the temperatures of the polishing agent and of the polishing plate lie in the range of 20°C to 30°C, and especially preferably in a range of 23°C to 27°C.

The method according to the invention for the simultaneous double-side polishing of wafers composed of semiconductor material can also be combined with an apparatus for polishing agent recycling. For this purpose, the used polishing agent, which emerges from the working gap via a lateral outlet, is prefiltered and collected in a container and replenished in a controlled manner with water, fresh polishing agent and KOH, and pumped back via a filter into the supply container for the polishing agent. In this case, temperature regulation ensures that the preferred temperatures of the polishing agent are maintained.

The individual aspects of the method according to the invention interact such that at the end a more homogeneous polishing agent distribution becomes possible directly on site on the polishing pad and, consequently, the material removal on each semiconductor wafer during the DSP is made more uniform.

Patent Claims:

1. A method for the simultaneous double-side polishing of at least one wafer (5) composed of semiconductor material which is situated in a suitably dimensioned cutout (3) in a carrier plate (1) and which has a front side and a rear side, and the double-side polishing is effected between an upper polishing plate covered with a first polishing pad and a lower polishing plate covered with a second polishing pad, with a polishing agent being supplied, wherein the surfaces of the first (upper) and of the second (lower) polishing pad are in each case interrupted by at least one channel-shaped depression running spirally from the center to the edge.

2. The method as claimed in claim 1, wherein the at least one channel-shaped depression running spirally in the polishing pad surface has at least three turns.

3. The method as claimed in either of claims 1 and 2, wherein the distance W between the turns of the at least one channel-shaped depression running spirally in the polishing pad surface is constant from the inner portion toward the outer portion.

4. The method as claimed in either of claims 1 and 2, wherein the distance W between the turns of the at least one channel-shaped depression running spirally in the polishing pad surface becomes continuously greater from the inner portion toward the outer portion.

5. The method as claimed in either of claims 1 and 2, wherein the distance W between the turns of the at least one channel-shaped depression running spirally in the polishing pad surface becomes continuously smaller from the inner portion toward the outer portion.

6. The method as claimed in either of claims 1 and 2, wherein the polishing pad surface has three spiral channel-shaped depressions arranged circularly around the midpoint of the polishing pad in the polishing pad surface, the distance W between whose turns becomes continuously greater from the inner portion toward the outer portion, and each of the three spiral channel-shaped depressions merges into a circular form enclosing the three spirals in the edge region of the polishing pad, without there being a connection between the three circular channels, and the outer edge region is formed by the ring-shaped area in the outer third of the polishing pad surface.

7. The method as claimed in any of claims 1 to 6, wherein the width of the at least one channel-shaped depression running spirally in the polishing pad surface becomes continuously greater from the inner portion toward the outer portion.

8. The method as claimed in any of claims 1 to 7, wherein the depth of the at least one channel-shaped depression running spirally in the polishing pad surface becomes continuously greater from the inner portion toward the outer portion.

9. The method as claimed in any of claims 1 to 8, wherein at least one suitably dimensioned circular cutout (3) in the carrier plate (1) is surrounded by three segmented cutouts (2) which have an identical size (relative to the area) and are separated from one another by the webs (4), with a distance among one another of in each case at most 110°, in a ring-shaped manner at a distance A from the circular cutout (3).

10. The method as claimed in any of claims 1 to 9, wherein an inherent rotation of the semiconductor wafer (5) within the

suitably dimensioned cutout (3) in the carrier plate (1) is possible.

11. The method as claimed in any of claims 1 to 9, wherein an inherent rotation of the semiconductor wafer (5) within the suitably dimensioned cutout (3) in the carrier plate (1) is prevented by the semiconductor wafer being fixed in the cutout (3).

12. The method as claimed in any of claims 1 to 11, wherein the polishing agent supply is effected on the front side and the rear side of the semiconductor wafer (5) in a pressurized manner through openings present both in the upper and in the lower polishing plate and also in the upper and in the lower polishing pad, and wherein nozzles for the polishing agent supply can be integrated in the openings in the polishing plate.

13. The method as claimed in claim 12, wherein the orientation of the openings of the nozzles integrated in the polishing plate for the polishing agent supply or the openings in the polishing plate and/or in the polishing pad, relative to the polishing pad surface, lies in an angular range of from 45° to less than or equal to 90°.

14. The method as claimed in claim 13, wherein the quantity of the polishing agent emerging from the openings into the working gap per unit time in an inner circular region of the polishing pad is higher than the quantity that emerges in the same time from the openings situated in the outer ring-shaped region.

15. The method as claimed in any of claims 1 to 14, wherein the front side of the at least one wafer (5) composed of

semiconductor material is polished at the upper polishing pad.