SUMMARY

According to a first aspect of the present invention, there is provided an analog-to-digital converter (ADC) for a multi-channel signal acquisition system, the ADC comprising: a sample-and-hold (S/H) circuit for each input channel, and operable to receive a respective analog input signal for each input channel; a digital-to-analog converter (DAC) common to all input channels; a comparator for each input channel, said comparator configured to receive an output signal from the S/H circuit of the respective input channel as a first input signal, and an output signal from the DAC as a second input signal, for generating a comparison result at each conversion cycle of the comparator; and a successive approximation register (SAR) common to all input channels and configured to generate, for each input channel, a digital output code based on the comparison results received from the respective comparator.

According to a second aspect of the present invention, there is provided a signal acquisition system comprising: a plurality of input channels; an analog-to-digital converter (ADC) comprising: a sample-and-hold (S/H) circuit for each input channel, and operable to receive a respective analog input signal for each input channel; a digital-to-analog converter (DAC) common to all input channels; a comparator for each input channel, said comparator configured to receive an output signal from the S/H circuit of the respective input channel as a first input signal, and an output signal from the DAC as a second input signal, for generating a comparison result at each conversion cycle of the comparator; and a successive approximation register (SAR) common to all input channels and configured to generate a digital output signal; and a digital multiplexer (MUX) configured to receive the comparison results from the respective comparators as inputs and multiplex said comparison results prior to inputting to the SAR for generating the digital output signal.

According to a third aspect of the present invention, there is provided a method of generating a digital output code from an analog input signal received at an input channel of a plurality of input channels, the method comprising the steps of: receiving said analog input signal at a sample-and-hold (S/H) circuit and a comparator for said input channel; providing a digital-to-analog converter (DAC); comparing, at the comparator, a first input signal received from the S/H circuit of said input channel with a second input signal received from the DAC for generating a

comparison result at each conversion cycle of the comparator; and generating, at a successive approximation register (SAR) common to all input channels, the digital output code based on the comparison results received from the comparator for said input channel.

According to a fourth aspect of the present invention, there is provided a method of converting a plurality of analog input signals to a digital output signal, the method comprising the step of: providing a plurality of input channels, receiving the respective analog input signal at a sample-and-hold (S/H) circuit and a comparator for each input channel; providing a digital-to-analog converter (DAC); comparing, at the comparator, a first input signal received from the S/H circuit of the respective input channel with a second input signal received from the DAC for generating a comparison result at each conversion cycle of the comparator; multiplexing, using a digital multiplexer (MUX), the comparison results received from the respective comparators; and generating, at a successive approximation register (SAR) common to all input channels, a digital output signal based on the multiplexed signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 shows block diagram illustrating a conventional multi-channel signal acquisition system.

Figure 2 shows the timing diagram of the conventional multi-channel signal acquisition system of Figure 1.

Figure 3a shows a schematic circuit diagram of a multi-channel signal acquisition system according to an example embodiment.

SUMMARY

According to a first aspect of the present invention, there is provided an analog-to-digital converter (ADC) for a multi-channel signal acquisition system, the ADC comprising: a sample-and-hold (S/H) circuit for each input channel, and operable to receive a respective analog input signal for each input channel; a digital-to-analog converter (DAC) common to all input channels; a comparator for each input channel, said comparator configured to receive an output signal from the S/H circuit of the respective input channel as a first input signal, and an output signal from the DAC as a second input signal, for generating a comparison result at each conversion cycle of the comparator; and a successive approximation register (SAR) common to all input channels and configured to generate, for each input channel, a digital output code based on the comparison results received from the respective comparator, wherein the S/H circuit and the DAC each comprises a capacitor array, so that the S/H circuit performs coarse conversion and the DAC performs fine conversion.

According to a second aspect of the present invention, there is provided a signal acquisition system comprising: a plurality of input channels; an analog-to-digital converter (ADC) comprising: a sample-and-hold (S/H) circuit for each input channel, and operable to receive a respective analog input signal for each input channel; a digital-to-analog converter (DAC) common to all input channels; a comparator for each input channel, said comparator configured to receive an output signal from the S/H circuit of the respective input channel as a first input signal, and an output signal from the DAC as a second input signal, for generating a comparison result at each conversion cycle of the comparator; and a successive approximation register (SAR) common to all input channels and configured to generate a digital output signal; and a digital multiplexer (MUX) configured to receive the comparison results from the respective comparators as inputs and multiplex said comparison results prior to inputting to the SAR for generating the digital output signal, wherein the S/H circuit and the DAC each comprises a capacitor array, so that the S/H circuit performs coarse conversion and the DAC performs fine conversion.

According to a third aspect of the present invention, there is provided a method of generating a digital output code from an analog input signal received at an input channel of a plurality of input channels, the method comprising the steps of:

receiving said analog input signal at a sample-and-hold (S/H) circuit to perform coarse conversion; performing a fine conversion for each input channel at a digital-to-analog converter (DAC); comparing, at a comparator, a first input signal received from the S/H circuit of said input channel with a second input signal received from the DAC for generating a

comparison result at each conversion cycle of the comparator; and generating, at a successive approximation register (SAR) common to all input channels, the digital output code based on the comparison results received from the comparator for said input channel, wherein the S/H circuit and the DAC each comprises a capacitor array.

According to a fourth aspect of the present invention, there is provided a method of converting a plurality of analog input signals to a digital output signal, the method comprising the steps of: providing a plurality of input channels; receiving the respective analog input signal at a sample-and-hold (S/H) circuit to perform coarse conversion; performing a fine conversion for each input channel at a digital-to-analog converter (DAC); comparing, at a comparator, a first input signal received from the S/H circuit of the respective input channel with a second input signal received from the DAC for generating a comparison result at each conversion cycle of the comparator; multiplexing, using a digital multiplexer (MUX), the comparison results received from the respective comparators; and generating, at a successive approximation register (SAR) common to all input channels, a digital output signal based on the multiplexed signal, wherein the S/H circuit and the DAC each comprises a capacitor array.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 shows block diagram illustrating a conventional multi-channel signal acquisition system.

Figure 2 shows the timing diagram of the conventional multi-channel signal acquisition system of Figure 1.

Figure 3a shows a schematic circuit diagram of a multi-channel signal acquisition system according to an example embodiment.

CLAIMS

1. An analog-to-digital converter (ADC) for a multi-channel signal acquisition system, the ADC comprising:

a sample-and-hold (S/H) circuit for each input channel, and operable to receive a respective analog input signal for each input channel;

a digital-to-analog converter (DAC) common to all input channels;

a comparator for each input channel, said comparator configured to receive an output signal from the S/H circuit of the respective input channel as a first input signal, and an output signal from the DAC as a second input signal, for generating a comparison result at each conversion cycle of the comparator; and

a successive approximation register (SAR) common to all input channels and configured to generate, for each input channel, a digital output code based on the comparison results received from the respective comparator.

2. The ADC as claimed in claim 1, wherein the SAR is further configured to generate control signals based on the comparison result at each conversion cycle of the comparator, for controlling switches in the respective S/H circuit and in the DAC.

3. The ADC as claimed in claim 2, wherein, in a coarse conversion stage, the second input signal is constant and the SAR is configured to control the switches in the S/H circuit such that the comparator successively compares the first input signal against the constant second input signal for generating comparison results corresponding to a first portion of the digital code.

4. The ADC as claimed in claim 3, wherein, in a fine conversion stage, the first input signal is constant and the SAR is configured to control the switches in the DAC such that the comparator successively compares the second input signal against the constant first input signal, for generating comparison results corresponding to a remaining second portion of the digital output code.

5. The ADC as claimed in any one of claims 2 to 4, wherein the switches in the respective S/H circuit and in the DAC comprise logic gates.

6. The ADC as claimed in any one of claims 2 to 5, wherein the respective S/H circuit and the DAC each comprises a capacitor array having a unit capacitor selected from a group consisting of a metal-insulator-metal (MIM) capacitor, a metal-finger capacitor, and a poly-insulator-poly (PIP) capacitor.

7. The ADC as claimed in any one of the preceding claims, wherein the S/H circuits are configured to sample the respective analog input signals at least partially simultaneously.

8. The ADC as claimed in any one of claims 1 to 6, wherein the S/H circuits are configured to sample the respective analog input signals sequentially.

9. The ADC as claimed in claim 8, wherein the S/H circuits of the respective input channels are independent of each other such that a maximum sampling time of each S/H circuit is determined based on the equation:

$$t_{s2} = \left[1 + (m-1)\cdot(n+1)\right]\cdot T_{clk} \approx (m-1)\cdot\frac{1}{2\cdot m\cdot f_{signal}}$$

where t_{s2} is the maximum sampling time, m is the number of input channels, n is the resolution level of the ADC, T_{clk} is the duration of one clock cycle, and f_{signal} is the input signal bandwidth.

10. A signal acquisition system comprising:

a plurality of input channels;

an analog-to-digital converter (ADC) comprising:

a sample-and-hold (S/H) circuit for each input channel, and operable to receive a respective analog input signal for each input channel;

a digital-to-analog converter (DAC) common to all input channels;

a comparator for each input channel, said comparator configured to receive an output signal from the S/H circuit of the respective input channel as a first input signal, and an output signal from the DAC as a second input signal, for generating a comparison result at each conversion cycle of the comparator; and

a successive approximation register (SAR) common to all input channels and configured to generate a digital output signal; and

a digital multiplexer (MUX) configured to receive the comparison results from the respective comparators as inputs and multiplex said comparison results prior to inputting to the SAR for generating the digital output signal.

11. The signal acquisition system as claimed in claim 10, wherein the S/H circuits are configured to sample the respective analog input signals at least partially simultaneously.

12. The signal acquisition system as claimed in claim 10, wherein the S/H circuits are configured to sample the respective analog input signals sequentially.

13. The signal acquisition system as claimed in claim 12, wherein the S/H circuits of the respective input channels are independent of each other such that a maximum sampling time of each S/H circuit is determined based on the equation:

$$t_{s2} = \left[1 + (m-1)\cdot(n+1)\right]\cdot T_{clk} \approx (m-1)\cdot\frac{1}{2\cdot m\cdot f_{signal}}$$

where t_{s2} is the maximum sampling time, m is the number of input channels, n is the resolution level of the ADC, T_{clk} is the duration of one clock cycle, and f_{signal} is the input signal bandwidth.

14. A method of generating a digital output code from an analog input signal received at an input channel of a plurality of input channels, the method comprising the steps of:

receiving said analog input signal at a sample-and-hold (S/H) circuit and a comparator for said input channel;

providing a digital-to-analog converter (DAC);

comparing, at the comparator, a first input signal received from the S/H circuit of said input channel with a second input signal received from the DAC for generating a comparison result at each conversion cycle of the comparator; and

generating, at the a successive approximation register (SAR) common to all input channels, the digital output code based on the comparison results received from the comparator for said input channel.

15. The method as claimed in claim 14, further comprising maintaining the second input signal constant, and coarse controlling, using the SAR, switches in the S/H circuit such that the comparator successively compares the first input signal against the constant second input signal for generating comparison results corresponding to a first portion of the digital code.

16. The method as claimed in claim 15, further comprising maintaining the first input signal constant, and fine controlling, using the SAR, switches in the DAC such that the comparator successively compares the second input signal against the constant first input signal for generating comparison results corresponding to a remaining second portion of the digital output code.

17. A method of converting a plurality of analog input signals to a digital output signal, the method comprising the step of:

providing a plurality of input channels;

receiving the respective analog input signal at a sample-and-hold (S/H) circuit and a comparator for each input channel;

providing a digital-to-analog converter (DAC);

comparing, at the comparator, a first input signal received from the S/H circuit of the respective input channel with a second input signal received from the DAC for generating a comparison result at each conversion cycle of the comparator;

multiplexing, using a digital multiplexer (MUX), the comparison results received from the respective comparators; and

generating, at a successive approximation register (SAR) common to all input channels, a digital output signal based on the multiplexed signal.

18. The method as claimed in claim 17, comprising sampling, using the S/H circuits, the respective analog input signals at least partially simultaneously.

19. The method as claimed in claim 17, comprising sampling, using the S/H circuits, the respective analog input signals sequentially.

20. The method as claimed in claim 19, wherein the step of receiving the respective analog input signal comprises receiving the analog input signals of the respective input channels independent of each other such that a maximum sampling time of each S/H circuit is determined based on the equation:

$$t_{s2} = \left[1 + (m-1)\cdot(n+1)\right]\cdot T_{clk} \approx (m-1)\cdot\frac{1}{2\cdot m\cdot f_{signal}}$$

where t_{s2} is the maximum sampling time, m is the number of input channels, n is the resolution level of the ADC, T_{clk} is the duration of one clock cycle, and f_{signal} is the input signal bandwidth.

CLAIMS

1. An analog-to-digital converter (ADC) for a multi-channel signal acquisition system, the ADC comprising:

a sample-and-hold (S/H) circuit for each input channel, and operable to receive a respective analog input signal for each input channel;

a digital-to-analog converter (DAC) common to all input channels;

a comparator for each input channel, said comparator configured to receive an output signal from the S/H circuit of the respective input channel as a first input signal, and an output signal from the DAC as a second input signal, for generating a comparison result at each conversion cycle of the comparator; and

a successive approximation register (SAR) common to all input channels and configured to generate, for each input channel, a digital output code based on the comparison results received from the respective comparator, wherein the S/H circuit and the DAC each comprises a capacitor array, so that the S/H circuit performs coarse conversion and the DAC performs fine conversion.

2. The ADC as claimed in claim 1, wherein the SAR is further configured to generate control signals based on the comparison result at each conversion cycle of the comparator, for controlling switches in the respective S/H circuit and in the DAC.

3. The ADC as claimed in claim 2, wherein, in a coarse conversion stage, the second input signal is constant and the SAR is configured to control the switches in the S/H circuit such that the comparator successively compares the first input signal against the constant second input signal for generating comparison results corresponding to a first portion of the digital code.

4. The ADC as claimed in claim 3, wherein, in the fine conversion, the first input signal is constant and the SAR is configured to control the switches in the DAC such that the comparator successively compares the second input signal against the constant first input signal, for generating comparison results corresponding to a remaining second portion of the digital output code.

5. The ADC as claimed in any one of claims 2 to 4, wherein the switches in the respective S/H circuit and in the DAC comprise logic gates.

6. The ADC as claimed in any one of claims 2 to 5, wherein the capacitor array of the respective S/H circuit and the DAC each comprises a capacitor array having a unit capacitor selected from a group consisting of a metal-insulator-metal (MIM) capacitor, a metal-finger capacitor, and a poly-insulator-poly (PIP) capacitor.

7. The ADC as claimed in any one of the preceding claims, wherein the S/H circuits are configured to simultaneously sample two or more of the respective analog input signals.

8. The ADC as claimed in any one of claims 1 to 6, wherein the S/H circuits are configured to sample the respective analog input signals sequentially.

9. The ADC as claimed in claim 8, wherein the S/H circuits of the respective input channels are independent of each other such that a maximum sampling time of each S/H circuit is determined based on the equation:

$$t_{s2} = \left[1 + (m-1)\cdot(n+1)\right]\cdot T_{clk} \approx (m-1)\cdot\frac{1}{2\cdot m\cdot f_{signal}}$$

where t_{s2} is the maximum sampling time, m is the number of input channels, n is the resolution level of the ADC, T_{clk} is the duration of one clock cycle, and f_{signal} is the input signal bandwidth.

10. A signal acquisition system comprising:

a plurality of input channels;

an analog-to-digital converter (ADC) comprising:

a sample-and-hold (S/H) circuit for each input channel, and operable to receive a respective analog input signal for each input channel;

a digital-to-analog converter (DAC) common to all input channels;

a comparator for each input channel, said comparator configured to receive an output signal from the S/H circuit of the respective input channel as a first input signal, and an output signal from the DAC as a second input signal, for generating a comparison result at each conversion cycle of the comparator; and

a successive approximation register (SAR) common to all input channels and configured to generate a digital output signal; and

a digital multiplexer (MUX) configured to receive the comparison results from the respective comparators as inputs and multiplex said comparison results prior to inputting to the SAR for generating the digital output signal, wherein the S/H circuit and the DAC each comprises a capacitor array, so that the S/H circuit performs coarse conversion and the DAC performs fine conversion.

11. The signal acquisition system as claimed in claim 10, wherein the S/H circuits are configured to simultaneously sample two or more of the respective analog input signals.

12. The signal acquisition system as claimed in claim 10, wherein the S/H circuits are configured to sample the respective analog input signals sequentially.

13. The signal acquisition system as claimed in claim 12, wherein the S/H circuits of the respective input channels are independent of each other such that a maximum sampling time of each S/H circuit is determined based on the equation:

$$t_{s2} = \left[1 + (m-1)\cdot(n+1)\right]\cdot T_{clk} \approx (m-1)\cdot\frac{1}{2\cdot m\cdot f_{signal}}$$

where t_{s2} is the maximum sampling time, m is the number of input channels, n is the resolution level of the ADC, T_{clk} is the duration of one clock cycle, and f_{signal} is the input signal bandwidth.

14. A method of generating a digital output code from an analog input signal received at an input channel of a plurality of input channels, the method comprising the steps of:

receiving said analog input signal at a sample-and-hold (S/H) circuit to perform coarse conversion;

performing a fine conversion for each input channel at a digital-to-analog converter (DAC);

comparing, at a comparator, a first input signal received from the S/H circuit of said input channel with a second input signal received from the DAC for generating a comparison result at each conversion cycle of the comparator; and

generating, at a successive approximation register (SAR) common to all input channels, the digital output code based on the comparison results received from the comparator for said input channel, wherein the S/H circuit and the DAC each comprises a capacitor array.

15. The method as claimed in claim 14, wherein the coarse conversion comprises maintaining the second input signal constant, and coarse controlling, and configuring the SAR, to control switches in the S/H circuit such that the comparator successively compares the first input signal against the constant second input signal for generating comparison results corresponding to a first portion of the digital code.

16. The method as claimed in claim 15, wherein the fine conversion comprises maintaining the first input signal constant, and fine controlling, ~~using~~ and configuring the SAR, to control switches in the DAC such that the comparator successively compares the second input signal against the constant first input signal for generating comparison results corresponding to a remaining second portion of the digital output code.

17. A method of converting a plurality of analog input signals to a digital output signal, the method comprising the step of:

providing a plurality of input channels;

receiving the respective analog input signal at a sample-and-hold (S/H) circuit to perform coarse conversion;

performing a fine conversion for each input channel at a digital-to-analog converter (DAC);

comparing, at the comparator, a first input signal received from the S/H circuit of the respective input channel with a second input signal received from the DAC for generating a comparison result at each conversion cycle of the comparator;

multiplexing, using a digital multiplexer (MUX), the comparison results received from the respective comparators; and

generating, at a successive approximation register (SAR) common to all input channels, a digital output signal based on the multiplexed signal, wherein the S/H circuit and the DAC each comprises a capacitor array.

18. The method as claimed in claim 17, comprising simultaneously sampling, using the S/H circuits, two or more of the respective analog input signals.

19. The method as claimed in claim 17, comprising sampling, using the S/H circuits, the respective analog input signals sequentially.

20. The method as claimed in claim 19, wherein the step of receiving the respective analog input signal comprises receiving the analog input signals of the respective input channels independent of each other such that a maximum sampling time of each S/H circuit is determined based on the equation:

$$t_{s2} = \left[1 + (m-1)\cdot(n+1)\right]\cdot T_{clk} \approx (m-1)\cdot\frac{1}{2\cdot m\cdot f_{signal}}$$

where t_{s2} is the maximum sampling time, m is the number of input channels, n is the resolution level of the ADC, T_{clk} is the duration of one clock cycle, and f_{signal} is the input signal bandwidth.