transverse redistribution of traces are schematically represented 134, 136, and 138) facilitate the redistribution. The example transverse redistribution of traces of each level may be connected directly to an adjacent level or to another vertically offset location) by vertical interconnects (such as micro-vias, or analogous structures, as known to persons skilled in the art). In some examples, interposer 106 may include one or more layers formed of one or more insulating layers, such as glass-reinforced epoxy (such as FR-4), polytetrafluorethylene (Teflon), cotton-paper reinforced epoxy (CEM-3), phenolic-glass (G3), paper-phenolic (FR-1 or FR-2), polyester-glass (CEM-5), as well as many other example dielectric materials, and combinations of the above. In many examples, interposer 106 may be formed through a buildup process, either on a core or in a coreless configuration; and a micro via formation process, such as laser drilling, followed by metal fill, can be used to form interconnections between conductive layers in the buildup and die bond pads.

[0023] Fig. 1B illustrates generally a simplified cross section of a schematic representation of an alternative embodiment of an example microelectronic device 100' having a patch 102 and an interposer 106. Microelectronic device 100' differs from microelectronic device 100 of FIG. lA primarily in the following respects: the second embedded die 105' is of an example configuration including a vertical through contact 107 (which in some examples may be a characteristic of any or all embedded die within a substrate), such as a TSV through the die; and substrate 102 includes an additional lower surface vertical contact 114’ extending to through contact 107 of embedded die 105'.

[0024] Addressing second embedded die 105', as with the first embedded die 104, second embedded die 105' may be either a bridge die or an active die, and can be of any desired configuration. Though first and second embedded die are depicted in FIG. lA and 1B, as will be apparent to persons skilled in the art, many more embedded die may be supported within patch 102. As noted above in this example, for purposes of illustration, second embedded die 105' includes an example vertical through contact 107. As will be apparent to persons skilled in the art, an embedded die may commonly include multiple vertical through contacts, at least some of which may be arranged in an array at a

desired pitch relative to one another. The presence of a vertical through contact 107 may commonly result in the need for a lower surface vertical contact 114' extending to second embedded die 105' to facilitate connection to interposer 106' as shown.

[0025] It is noted that the thickness of the first embedded die 104 and the thickness of the second embedded die 105' are different. The thickness being a dimensional measure of an embedded die as assembled in the patch 102 in a direction perpendicular to either the top surface 112 or bottom surface 128. In addition to allowing a patch to accommodate embedded dies of differing thickness, the techniques discussed herein also allow for reduced bump top variation (BTV).

[0026] FIGS. 2A-2R illustrate generally simplified schematic representations of sequential representative stages in an example process for forming an example patch incorporating the techniques and structures described herein. As depicted in FIG. 2A, one or more initial patterned metallization layers 202 can be formed on a first carrier structure, indicated generally 210. In some examples, carrier structure 210 can include a support structure defining a planar support surface over which the patch may be formed. In some examples, carrier structure 210 may also include a release layer or other surface layer on the planar surface of the support structure. For purposes of the present example, a seed layer 206 can be deposited on the carrier structure 210.

[0027] The metallization layers 202 can be of any desired form for forming a temporary bottommost portion of vertical contacts (or other conductive structure) of the patch. The metallization layer 202 can be formed through desired processes known to those skilled in the art. For example, for many materials, a semi-additive process (SAP), may be used to form the patterned structures for these lower metallization layers 202.

[0028] The patch may include a dielectric body in which the embedded die is retained. In some examples, a first portion of the dielectric body may define an upper surface of the dielectric body, and a second portion of the dielectric body may extend to encapsulate or embed the embedded dies 104, 105. In some examples both the first portion of the dielectric body and the second portion may have planarized surfaces, as described below. Such planarized

assembly. At FIG. 21, the first carrier structure 210 can be removed from the assembly such as by, but not limited to, laser de-bonding, thermal or mechanical means or combinations thereof At FIG. 2J, at least a portion, if not the entire initial metallization layers 214, can be removed using processes such as etching, for example. At FIG. 2K, the bond material 231 used to initially fix the embedded dies 204, 205 can be removed such as by dry etching, for example. At FIG. 2L, the assembly can be flipped and a conductive routing layer 240 can be fabricated to for example, connect contacts of the embedded dies 204, 205 with vertical contacts 222, or to provide connection pads for contacts of the embedded dies 204, 205 or vertical contacts 222.

[0037] At FIG. 2M an insulative layer 242 can be attached or formed to the exposed surfaces of the first portion 214 of the dielectric body and to the exposed surfaces of the conductive routing layer 240. The insulative layer 242 can further be etched or drilled to allow formation of exposed connections 244, 245 for the surface dies or other devices. In certain examples, the exposed connections 244, 245, for connection to the surface dies or other devices, can be arranged with a minimum pitch commensurate with a pitch of connection pads of the surface dies 108, 110 (FIG. 1) or bridge die 204, 205. In some examples, the first pitch can be on the order of 40um or less. In certain examples, the first pitch can be on the order of 30um or less. In certain examples, the material of the insulative layer 242 can include a solder resist.

[0038] At FIG. 2N, stiffeners 246 can be attached to the material of the insulative layer 242 to stiffen the patch assembly. At FIG 20, the second carrier structure 236 can be removed. In certain examples, a laser can be used to ablate the adhesive layer 238 attaching the second carrier structure 236 to the patch assembly. At FIG. 2P, the protective layer 234 can be removed to expose portions of the vertical contacts 222. FIGs, 2Q and 2R illustrate options for fabricating terminals of the patch for connecting to the interposer. At FIG. 2Q, an second insulative layer 248 can be attached to the underside of the patch assembly and can further be etch or drilled to expose retracted contact areas of the vertical contacts 222. At FIG, 2R, microballs 250 can be attached to the exposed portions of the vertical connectors 222.