[0005] To further scale cell height while maintaining robust power delivery, the semiconductor industry is looking toward buried power rail (BPR). Moving the power rails below the device plane allows the cell height to be reduced to 5T (i.e. 4 wiring tracks for signaling plus one wiring track to absorb line-end extensions and tip-to-tip spacing in tightly packed cells).

[0006] While buried power rail (BPR) plays a vital role in exploiting 3D transistor-on-transistor stacking to open up a new path forward at the end of 2D scaling, a new challenge is presented: how to get power into the BPRs. Connecting a power rail, which now sits below the device plane, with the power-delivery network (PDN), which sits above the device plane, requires a tall power connection. This power connection cannot afford to be too small for risk of creating a current pinch-point or be too large for risk of interfering with dense cell placement.

[0007] Realizing the advantages of CFET and BPR as outlined above, and further realizing the need for a robust, low-resistance means of delivering power into the BPR, a unique middle-of-line power-delivery-network approach is provided in the present disclosure.

[0008] According to a first aspect of the present invention, there is provided a semiconductor device. The semiconductor device includes a first power rail, a first power input structure, a circuit and a first middle-of-line rail. The first power rail is formed in a first rail opening within a first isolation trench on a substrate. The first power input structure is configured to connect with a first terminal of a power source that is external of the semiconductor device to receive electrical power from the power source. The circuit is formed, on the substrate, by layers between the first power rail and the first power input structure, the layers extending in a direction parallel to a surface of the substrate. The first middle-of-line rail is formed by one or more of the layers that form the circuit. The first middle-of-line rail is configured to deliver the electrical power from the first power input structure to the first power rail along the direction,

the first power rail providing the electrical power to the circuit for operation, the first middle-of-line rail including an upper layer for forming an upper local interconnect, a lower layer for forming a lower local interconnect, and a strap layer that continuously merges the upper layer and the lower layer.

[0009] Further, in some embodiments, the semiconductor device includes a second power rail, a second power input structure, and a second middle-of-line rail. The second power rail is formed in a second rail opening within a second isolation trench on the substrate. The second power rail is parallel with the first power rail. The

local interconnect in the second transistor, and a strap layer to merge the first layer and the second layer.

[0016a] According to a second aspect of the present invention, there is provided a method for fabricating a semiconductor device, comprising:

forming, in a first rail opening in a first isolation trench on a substrate, a first power rail;

forming, a first power input structure for coupling with a first terminal of a power source that is external of the semiconductor device to receive electrical power from the power source; and

forming, a circuit and a first middle-of line rail in layers between the first power rail and the first power input structure, the first middle-of-line rail delivering the electrical power from the first power input structure to the first power rail, and the first power rail providing the electrical power to the circuit for operation.

[0017]There is also provided a method for fabricating a semiconductor device. For example, buried power rails are formed in rail openings within isolation trench on a substrate. The buried power rails form a BPR power delivery network in an example. Then, active devices and MOL power delivery network are formed. In some examples, the MOL power delivery network includes MIL rails and M0 rails. In an example, a MIL rail includes a top LI structure, a bottom LI structure and a strap structure that merges the top LI structure and the bottom LI structure. The MIL rails are connected with the BPRs by short power vias, and the MIL rails and the M0 rails are connected by top CD structures. Further, upper metal layers are formed, via structures that connect wires in different metal layers are also formed. An UML power delivery network is formed in the upper metal layers. In an example, power input pads are formed in the top metal layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0019] Fig. 1 shows a diagram of a semiconductor device according to some embodiment of the disclosure.

[0020] Fig. 2 shows a top view of a semiconductor device according to some embodiments of the disclosure.

[0021] Fig. 3 shows a top view and a cross-sectional view of power tap cells, according to some embodiments of the disclosure.

[0022] Fig. 4 shows a top view and a cross-sectional view of power tap cells, according to some embodiments of the disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first power rail formed in a first rail opening within a first isolation trench on a substrate;

a first power input structure configured to connect with a first terminal of a power source that is external of the semiconductor device to receive electrical power from the power source;

a circuit that is formed, on the substrate, of layers between the first power rail and the first power input structure, the layers extending in a direction parallel to a surface of the substrate; and

a first middle-of-line rail that is formed by one or more of the layers that form the circuit, the first middle-of-line rail being configured to deliver the electrical power from the first power input structure to the first power rail along the direction, the first power rail providing the electrical power to the circuit for operation, the first middle-of-line rail including an upper layer for forming an upper local interconnect, a lower layer for forming a lower local interconnect, and a strap layer that continuously merges the upper layer and the lower layer.

2. The semiconductor device of claim 1, further comprising:

a second power rail formed in a second rail opening within a second isolation trench on the substrate, the second power rail being parallel with the first power rail;

a second power input structure configured to connect with a second terminal of the power source, and to receive, with the first power input structure, the electrical power from the power source; and

a second middle-of-line rail that is formed by the one or more of the layers that form the circuit, the second middle-of-line rail being parallel with the first middle-of-line rail, and the first and second middle-of-line rails being configured to deliver the electrical power from the first and second input structures to the first and second power rails, the first and second power rails providing the electrical power to the circuit for operation.

3. The semiconductor device of claim 1, wherein:

the circuit includes a cell row of cell circuits that have a same cell height; and

the first middle-of-line rail includes a section in a power tap cell that is disposed in the cell row, the power tap cell having the same cell height as the cell circuits.

4. The semiconductor device of claim 3, wherein:

the first middle-of-line rail is formed by at least a layer that is used to form connections within a cell circuit.

5. The semiconductor device of claim 3, wherein:

the circuit includes multiple cell rows of cell circuits; and

the first middle-of-line rail is formed of sections respectively in power tap cells disposed in the multiple cell rows.

6. The semiconductor device of claim 5, wherein

the power tap cells are aligned in a column, and the sections in the respective power tap cells are conductively connected to form the first middle-of-line rail.

7. The semiconductor device of claim 5, wherein each section of the sections in the respective power tap cells is connected to the first power rail by at least a power via, and is connected to a metal rail by at least a contact.

8. The semiconductor device of claim 2, wherein:

the first and second middle-of-line rails are perpendicular to the first and second power rails.

9. The semiconductor device of claim 1, wherein:

the circuit includes a first transistor that is disposed above a second transistor in a vertical direction that is perpendicular to a surface of the substrate.

10. The semiconductor device of claim 9, wherein:

the first middle-of-line rail includes a first layer for forming a local interconnect in the first transistor, a second layer for forming a local interconnect in the second transistor, and a strap layer to merge the first layer and the second layer.

11. A method for fabricating a semiconductor device, comprising:

forming, in a first rail opening in a first isolation trench on a substrate, a first power rail;

forming, a first power input structure for coupling with a first terminal of a power source that is external of the semiconductor device to receive electrical power from the power source; and

forming, a circuit and a first middle-of line rail in layers between the first power rail and the first power input structure, the first middle-of-line rail delivering the electrical power from the first power input structure to the first power rail, and the first power rail providing the electrical power to the circuit for operation.

12. The method of claim 11, further comprising:

forming, in a second rail opening within a second isolation trench on the substrate, the second power rail that is parallel with the first power rail;

forming, a second power input structure for coupling with a second terminal of the power source to receive the electrical power form the power source; and

forming, a second middle-of-line rail in the layers that form the circuit, the second middle-of-line rail being parallel with the first middle-of-line rail, and the first and second middle-of-line rails delivering the electrical power from the first and second input structures to the first and second power rails, the first and second power rails providing the electrical power to the circuit for operation.

13. The method of claim 11, wherein forming, the circuit and the first middle-of-line rail in layers between the first power rail and the first power input structure further comprises:

forming a cell row of cell circuits and at least a power tap cell that has a same height as the cell circuits, the power tap cell including a section of the first middle-of-line rail.

14. The method of claim 13, further comprising:

using at least a layer that is used to form connections within a cell circuit to form, the first middle-of-line rail.

15. The method of claim 13, further comprising:

forming multiple cell rows of cell circuits with power tap cells disposed in the multiple cell rows; and

forming the first middle-of-line rail using respective sections in the power tap cells.

16. The method of claim 15, further comprising:

forming the power tap cells that are aligned in a column.

17. The method of claim 15, wherein each section of the sections in the respective power tap cells is connected to the first power rail by at least a power via, and is connected to a metal rail by at least a contact.

18. The method of claim 12, wherein:

the first and second middle-of-line rails are perpendicular to the first and second power rails.

19. The method of claim 11, further comprising:

forming the circuit having a first transistor that is disposed above a second transistor in a vertical direction that is perpendicular to a surface of the substrate.

20. The method of claim 19, further comprising:

forming the first middle-of-line rail in a first layer that is used for forming local interconnects in the first transistor, a second layer that is used for forming local interconnects in the second transistor, and a strap layer that merges the first layer and the second layer.