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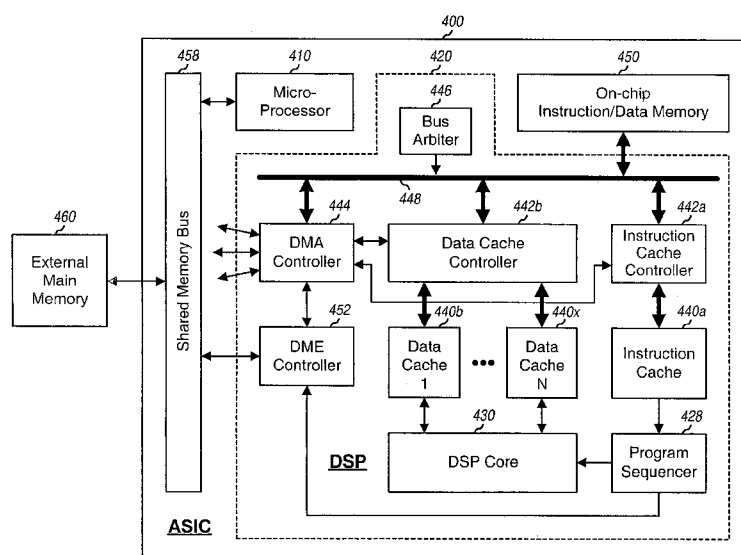
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— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA,

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(54) Title: CACHED MEMORY SYSTEM AND CACHE CONTROLLER FOR EMBEDDED DIGITAL SIGNAL PROCESSOR



(57) Abstract: A cached memory system that can handle high-rate input data and ensure that an embedded DSP can meet real-time constraints is described. The cached memory system includes a cache memory located close to a processor core, an on-chip memory at the next higher memory level, and an external main memory at the topmost memory level. A cache controller handles paging of instructions and data between the cache memory and the on-chip memory for cache misses. A direct memory exchange (DME) controller handles user-controlled paging between the on-chip memory and the external memory. A user/programmer can arrange to have the instructions and data required by the processor core to be present in the on-chip memory well in advance of when they are actually needed by the processor core.

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