SILICIDED RECESSED SILICON

Field of the Invention

[0001] This invention relates generally to silicidation reactions and the products thereof, and more particularly to the full silicidation of silicon in a recess.

Background of the Invention

[0002] Integrated circuit designs are continually being scaled down in efforts to reduce power consumption and increase speed. With each passing generation, devices tend to get smaller and more densely packed, raising a variety of problems for integration. One of the problems for integration is the small volumes provided for conductive elements. In order to achieve acceptable circuit speeds, it is important that such elements are provided with very high conductivity.

[0003] Other problems relate to difficulties in lining or filling high aspect ratio trenches or vias. For example, elongated trenches are used for damascene metallization; isolated holes or vias are used for forming vertical contacts; stacked trenches above the substrate and deep trenches within the substrate are used for memory cell capacitor formation; etc. Depositing within such vias becomes more challenging with higher aspect ratios with each passing generation. Voids can easily form during deposition or subsequent processing, leading to lower device yields.

Summary of the Invention

[0004] In accordance with one aspect of the invention, a method is provided for forming a metal silicide structure in an integrated circuit. The method includes providing a recess within a partially fabricated integrated circuit. Silicon is deposited into the recess. A mixture of metals is deposited over the recess and in contact with the silicon, where the mixture of metals includes at least two metals having opposing diffusivities relative to silicon. The mixture of metals and the silicon are reacted in the recess to form a metal silicide within the recess.

[0005] In accordance with another aspect of the invention, a method is provided for forming a recessed access device for an integrated circuit. The method includes etching a trench in a semiconductor structure. The trench is lined with a

dielectric layer, and the lined trench is at least partially filled with silicon. A metal layer is deposited over the trench and in contact with the silicon. The silicon in the trench is fully reacted in a silicidation reaction with the metal layer.

[0006] In accordance with another aspect of the invention, an integrated circuit is provided, including a metal silicide structure. A metal silicide fills at least a lower portion of a recess without voids. The metal silicide includes a mixture of at least a first metal having a greater diffusivity in silicon than silicon has in the first metal. The metal silicide also includes a second metal having a lesser diffusivity in silicon than silicon has in the second metal.

[0007] In accordance with another aspect of the invention, a memory device is provided. The device includes a recessed access device in a memory array, including a recess within a semiconductor substrate, a thin dielectric layer lining the recess, and a metal silicide filling at least a lower portion of the trench without voids.

Brief Description of the Drawings

[0008] [0015] The invention will be better understood from the detailed description of the preferred embodiments and from the appended drawings, which are meant to illustrate and not to limit the invention.

[0009] Figure 1 is a schematic plan view of a memory device, laid out in accordance with a preferred embodiment of the invention.

[0010] Figure 2 is a schematic, cross-sectional side view of the memory device of Figure 1 taken along lines 2-2, in accordance with a preferred embodiment of the invention.

[0011] Figures 3-7 are a series of cross-sectional views of a portion of a semiconductor device, illustrating formation of DRAM access transistors similar to those of Figures 1 and 2, according to a preferred embodiment of the present invention.

[0012] Figure 8 is a schematic, cross-sectional view of the device of Figure 7 after recessing silicon within the trench, and prior to deposition of metal for silicidation, in accordance with one embodiment of the present invention.

[0013] Figure 9 is a schematic, cross-sectional view of the device of Figure 7 after planarizing silicon within the trench and depositing metal for silicidation, in accordance with another embodiment of the present invention.

[0014] Figures 10A-11B are micrographs illustrating fully silicided, recessed gates for memory access devices after a silicidation anneal is performed on the device of Figure 9.

[0015] Figure 12 is a schematic cross-section showing the partially fabricated semiconductor device of Figures 10A-11B after recessing and burying the fully silicided gates within their trenches.

[0016] Figures 13-21 are a series of cross-sectional views of a portion of a semiconductor device, illustrating simultaneous formation of peripheral transistor gate stacks and recessed access devices (similar to those of Figures 1 and 2) in the array, according to another embodiment of the invention.

Detailed Description of the Preferred Embodiment

[0017] While the preferred embodiments of the present invention are illustrated in combination with a pitch doubling technique, it should be understood that the circuit design of these preferred embodiments may be incorporated into any integrated circuit. In particular, they may be advantageously applied to form any device having an array of electrical devices, including logic or gate arrays and volatile or non-volatile memory devices, such as DRAMs, RAMs, or flash memory. The integrated circuits formed by the methods described herein can be incorporated in any of a number of larger systems, such as motherboards, desktop or laptop computers, digital cameras, personal digital assistants, or any of a number of devices for which memory is useful.

[0018] The design and functioning of one memory device, a DRAM, laid out according to one embodiment of the present invention, is illustrated in the figures, and described in greater detail below.

[0019] Figure 1 shows a view of a portion of a memory device 10. This schematic layout illustrates the various electrical devices and other components that form the memory device 10. Of course, many of these components would be indistinguishable in a purely visual representation, and some of the components shown in Figure 1 are artificially distinguished from other components in order to highlight their functionality. The memory device 10 is built on and in a substrate 11, which forms the lowest level of semiconductor material in which electrical devices are formed. The substrate 11 typically comprises silicon. Of course, other suitable materials (*e.g.*, other group III-V elements) may also be used, as is well-known to those skilled in the art. When describing the other

components, their depth or height may be most easily understood with reference to the top surface of the substrate 11, best seen in Figure 2.

[0020] Four elongate word lines 12a, 12b, 12c, 12d are also shown in Figure 1 extending along the memory device 10. In a preferred embodiment, these word lines 12 were formed using a pitch doubling technique. In particular, these word lines 12 are preferably formed by a method that will be discussed in greater detail with reference to Figures 3-9. Using such a technique, the pitch of the resulting features may be less than the minimum pitch defined by the photolithographic technique. For example, in one embodiment, the pitch of the resulting features may equal one half the minimum pitch defined by the photolithographic technique.

[0021] In general, pitch doubling may be performed by the following sequence of steps, as is well understood by those skilled in the art. First, photolithography may be used to form a pattern of lines in a photoresist layer overlying a layer of an expendable material and a substrate. This photolithographic technique achieves a pitch between adjacent lines of 2F, as disclosed above, which pitch is limited by the optical characteristics of photolithography. In one embodiment, F is within the range of 60 to 100 nm. This range is typical for state-of-the-art photolithographic techniques used to define features. In one photolithography system, F equals approximately 86 nm, while, in another system, F equals approximately 78 nm.

[0022] The width of each line defined by photolithography is typically also defined as F, as would be well understood by those skilled in the art. The pattern may then be transferred by an etching step (preferably anisotropic) to the lower layer of expendable material, thereby forming placeholders, or mandrels in the lower layer. The photoresist lines can then be stripped, and the mandrels can be isotropically etched to increase the distance between neighboring mandrels. Preferably, the distance between the neighboring mandrels is increased from F to 3F/2. Alternatively, the isotropic "shrink" or "trim" etch could have been performed at the level of the resist. A conformal layer of spacer material may then be deposited over the mandrels. This layer of material covers both horizontal and vertical surfaces of the mandrels. Spacers, *i.e.*, material extending from sidewalls of another material, are therefore formed on the sides of the mandrels by preferentially etching the spacer material from the horizontal surfaces in a directional spacer etch. The remaining mandrels are then selectively removed, leaving behind only the spacers, which together may act as a mask for patterning. Thus, where a given pitch,

2F, formerly included a pattern defining one feature and one space, the same width now includes two features and two spaces defined by the spacers. As a result, the smallest feature size achievable with a given photolithographic technique is effectively decreased. This method of pitch doubling, which may be repeated for further reduction in the size of the features, will be discussed in greater detail below with reference to Figures 3-9.

[0023] Of course, as would be well known in the art, the extent of the shrink/trim etch and the thicknesses of the deposited spacers may be varied to achieve a variety of feature and pitch sizes. In the illustrated embodiments, whereas the photolithographic technique may resolve a pitch of 2F, the features, *i.e.* word lines 12 in the instant example, have a pitch of F. The word lines 12 are defined by a width of about F/2, and adjacent word lines 12a, 12b or 12c, 12d are separated by the same width, F/2. Meanwhile, as a byproduct of the pitch-doubling technique, the separation between the spaced-apart word lines 12b, 12c is 3F/2. In a preferred embodiment, an isolation trench is filled with an insulator and lies within this separation between these word lines 12b, 12c; however, in other embodiments, this isolation trench need not be present.

[0024] For every distance of 3F, there are two word lines, yielding what may be referred to as an effective pitch of 3F/2. More generally, the word lines preferably have an effective pitch between 1.25F and 1.9F. Of course, the particular pitch used to define the word lines is only an example. In other embodiments, the word lines may be fabricated by more conventional techniques, and pitch doubling need not be used. In one embodiment, for example, the word lines may each have a width of F and may be separated by F, 2F, 3F or some other width. In still other embodiments, the word lines need not be formed in pairs either. For example, in one embodiment, only one word line need pass through each active area.

[0025] The entire length of the word lines 12 is not visible in Figure 1, but, in a typical implementation, each word line 12 may extend across hundreds, thousands or millions of transistors. At the edges of the word lines 12, as is well-known to those of skill in the art, the word lines 12 are typically electrically coupled to a device, such as a power source, that can place a current across the word line 12. Often, the power sources for the word lines 12 are indirectly coupled to a CPU through a memory controller.

[0026] In one embodiment, the word lines 12 comprise a p-type semiconductor, such as silicon doped with boron. In other embodiments, the word lines 12 may comprise an n-type semiconductor, metal silicide, tungsten or other similarly

behaving material, as is well-known to those of skill in the art. In some embodiments, the word lines 12 may comprise a variety of materials, in a layered, mixed or chemically bonded configuration.

[0027] The horizontal lines seen in Figure 1 are formed by digit lines 14a, 14b. In one exemplary embodiment, the width of each of these digit lines, illustrated as DL in Figure 1, is equal to F. No pitch doubling has been used to form these exemplary digit lines 14. Adjacent digit lines 14a, 14b are separated, in a preferred embodiment, by a distance, illustrated as S in Figure 1, equal to 2F. The pitch of the digit lines is preferably greater than 2.5F, and preferably less than 4F. Without pitch-doubling techniques, the lower limit is, of course, imposed by the photolithographic technique used to form the digit lines. On the other hand, near the upper end of this range, the photolithography is less precise, and therefore less expensive, but the memory itself begins to grow too large. In a more preferred embodiment, the pitch of the digit lines is between 2.75F and 3.25F. This range represents a desirable balance between the ease of manufacturing and the size of the chip. In the illustrated embodiment, the digit lines 14 have a pitch of 3F. Of course, in other embodiments, different widths and spacing are possible.

[0028] As with the word lines 12, the entire length of the digit lines 14 is also not visible in Figure 1, and the digit lines 14 typically extend across many transistors. At the edges of the digit lines 14, as is well-known to those of skill in the art, the digit lines 14 are typically electrically coupled to current sense amplifiers, and thereby to a power or voltage source. Often, the power sources for the digit lines 14 are also indirectly coupled to a CPU through a memory controller. As a result of the more relaxed pitch between the digit lines 14, the sense amplifiers may be spaced farther from one another, relaxing their manufacturing tolerances, and decreasing the likelihood of capacitance coupling of adjacent digit signals.

[0029] In one embodiment, the digit lines 14 comprise a conducting metal, such as tungsten, copper, or silver. In other embodiments, other conductors or semiconductors may be used, as is well-known to those of skill in the art.

[0030] The other features visible in Figure 1 are the active areas 16, illustrated within curvilinear rectangles, which form axes A that are angled relative to the axes B of the digit lines. These rectangles represent a doped region or well within the substrate 11; however, in other embodiments, these rectangles need not represent physical structures or materials within or upon the memory device 10 and substrate 11. The active areas 16

define those portions of the memory device 10 that contain field effect transistors and are typically surrounded by field isolation elements (*e.g.*, shallow trench isolation (STI)). In one preferred embodiment, these active areas each comprise two drains 18 and one source 20. The source and drains may be larger or smaller than illustrated in Figure 1, as is well known to those of skill in the art. They may also be fabricated in any of a number of ways well-known to those of skill in the art.

[0031] In another embodiment, the active areas may comprise one source and one drain, wherein the source is formed near the digit line, and the drain is separated from the source by a word line. In such an embodiment, the memory device may be configured similarly to the memory device 10 in Figure 1, but there need only be one word line passing through each active area. Of course, in another embodiment, an active area may comprise one source and one drain, and the memory device may further comprise two word lines extending near the active area, configured similarly to the paired word lines 12c, 12d shown in Figure 1. In such an embodiment, the two word lines may both extend between the source and drain, and provide redundant control of the transistor.

[0032] As illustrated, a digit line 14 runs proximal to, and preferably above (see Figure 2), each source 20 that lies in the digit line's row. Meanwhile, each source 20 is separated to either side from its adjacent drains 18 by word lines 12. In one embodiment, the source 20 and drains 18 comprise an n-type semiconducting material, such as silicon doped with phosphorous or antimony. In other embodiments, the source 20 and drains 18 may comprise a p-type semiconductor, or they may be fabricated from other materials, as is well-known to those of skill in the art. In fact, the source 20 and drains 18 need not be fabricated from the same compounds.

[0033] The functioning of memory device 10 is briefly discussed with reference to Figure 2, which shows a cross-sectional view of one of the active areas 16. For a further discussion of the basic manner in which DRAMs function, U.S. Patent No. 3,731,287, issued to Seely et al., which is incorporated by reference herein in its entirety, discusses DRAMs in greater detail.

[0034] As shown in Figure 2, the drains 18 and source 20 may comprise protrusions from the relatively flat, upper surface of the substrate 11. In one preferred embodiment, the source 20 and drains 18 are fabricated as one-piece with the substrate 11, and are raised relative to the surface of the substrate 11 by etching a monolithic wafer

or substrate; in another arrangement, the source and drain protrusions are formed by selective epitaxial deposition using techniques well-known to those of skill in the art.

[0035] In one embodiment, at least a portion of digit line 14b is located above the upper surface of source 20. As illustrated in Figure 2, the source 20 is electrically coupled to the digit line 14b by a digit line plug 22, which plug may be formed in multiple stages or in a single stage, as shown. Meanwhile, the source 20 is separated from the two drains 18 by word lines 12a, 12b. The word lines 12a, 12b are preferably embedded in the substrate 11, extending downwards from the surface. Transistors of this design are often referred to as recessed access devices or RADs. The drains 18 are, in turn, electrically coupled to storage capacitors 24, and, in particular, to the lower electrode 26 of the storage capacitors 24, by contact plugs 28. In a preferred embodiment, the storage capacitors 24 comprise a lower electrode 26 separated from a reference electrode 30 by a dielectric material 32. In this configuration, these stacked storage capacitors 24 function in a manner well known to those of skill in the art. As illustrated, the storage capacitors 24 are preferably located above the plane of the substrate 11, although trench capacitors can be used in other arrangements.

[0036] In one embodiment, one side of every storage capacitor 24 forms a reference electrode 30, while the lower electrode 26 is electrically coupled to an associated drain 18. The word lines 12a, 12b function as gates in the field effect transistors they pass through, while the digit line 14b functions as a signal for the sources to which it is electrically coupled. Thus, the word lines 12a, 12b preferably control access to the storage capacitors 24 coupled to each drain 18, by allowing or preventing the signal (representing a logic "0" or a logic "1") carried on the digit line 14b to be written to or read from the storage capacitors 24. Thus, each of the two capacitors 24 connected to an associated drain 18 can contain one bit of data (i.e., a logic "0" or logic "1"). In a memory array, the combination of the digit line and word line that are selected can uniquely identify the storage capacitor 24 to or from which data should be written or read.

[0037] Turning back then to Figure 1, the design and geometry of the memory device 10 may be discussed in further detail. In the lower right hand corner of Figure 1, a number of axes have been illustrated. These axes are generally aligned with the longitudinal axes of circuit elements forming the memory device 10, and are illustrated to more clearly show the angles formed between various electrical devices and components. Axis A represents the longitudinal axis of active area 16. The drains 18 and source 20 of

each active area 16 preferably have a substantially linear relationship that may be used to define a longitudinal axis. As illustrated, all of the active areas 16 are substantially parallel. It will be understood, of course, that the drains 18 and source 20 need not form an absolutely straight line, and indeed a substantial angle may be defined by these three points. In some embodiments, therefore, the axis A may be defined by the two drains 18, or by the source 20 and only one of the drains 18, or in a number of other ways that would be clearly understood by those skilled in the art. In other embodiments, in which the active area comprises a single drain and a single source, the axis A may be defined by a line between the single drain and single source.

[0038] Axis B represents the longitudinal axis of digit line 14b. In the illustrated embodiment, the digit line 14b forms a substantially straight line. Just as the active areas 16 are preferably parallel, the digit lines 14a, 14b also preferably form generally parallel axes. Thus, in a preferred embodiment, axis A of every active area 16 forms a similar angle with every axis B of the digit lines 14, at least in the region of each memory cell.

[0039] In a preferred embodiment, illustrated in Figure 1, an acute angle is formed between axis A and axis B. In the illustrated embodiment, this acute angle, θ, defined between axis A and axis B, is 45°.

[0040] The angling of the active areas 16 relative to the digit lines 14 facilitates the location of the contact plugs 28 extending between drains 18 and associated storage capacitors 24. Since these contact plugs 28 extend from the top surface of the drains 18 in the preferred embodiment (illustrated in Figure 2), the engineering is simplified if the digit lines 14 do not extend over the tops of the drains 18. By angling the active areas 16, the distance between a digit line 14 and drains 18 may be selected to facilitate electronic contact between the drains and contact plugs, even while the digit line 14 substantially overlaps and contacts the source 20 of the same active area 16.

[0041] Of course, the angle, θ, may have any of a number of values chosen to maximize the pitch of the electrical devices. As will be readily apparent to one of skill in the art, different angles will yield different pitches between adjacent active areas. In one embodiment, the angle, θ, is preferably between 10° and 80° degrees. In a more preferred embodiment, the angle, θ, is between 20° and 60°. In a still more preferred embodiment, the angle, 0, is between 40° and 50°.

[0042] Turning to Figures 3-10, one method of fabricating the pitch-doubled word lines 12 of the memory device 10 is illustrated in greater detail. The skilled artisan will readily appreciate that the particular materials of the illustrated embodiment can be replaced individually or in combination with other groups of materials. Figure 3 illustrates a semiconductor substrate 11 over which a thin, temporary layer 40, comprising oxide in a preferred embodiment, has been formed according to conventional semiconductor processing techniques. A hard mask layer 42, such as silicon nitride, is then deposited over the substrate 11 and temporary layer 40. The hard mask layer 42 may be formed by any well-known deposition process, such as sputtering, chemical vapor deposition (CVD) or low-temperature deposition, among others. Although the hard mask layer 42 comprises silicon nitride in the preferred embodiment, it must be understood that it may also be formed of silicon oxide, for example, or other materials suitable for the selective etch steps described below.

[0043] Next, in a step not illustrated in the figures, the hard mask layer 42 is patterned using a photoresist layer formed over the hard mask layer 42. The photoresist layer may be patterned to form a mask using conventional photolithographic techniques, and the hard mask layer 42 may then be anisotropically etched through the patterned photoresist to obtain a plurality of hard mask columns 44 extending in the y-dimension (as defined by Figure 1), with trenches 46 separating those columns. The photoresist layer may then be removed by conventional techniques, such as by using an oxygen-based plasma.

[0044] With reference to Figure 5A, after the trenches 46 have been formed in the hard mask layer 42, a conformal layer of spacer material may be deposited to cover the entire surface of the memory device 10. Preferably, the spacer material can be selectively etched with respect to the substrate 11 and the temporary layer 40, and the substrate 11 and the temporary layer 40 can each be selectively etched with respect to the spacer material. In the illustrated embodiment, the spacer material comprises polysilicon. The spacer material may be deposited using any suitable deposition process, such as, for example, CVD or physical vapor deposition (PVD).

[0045] After laying the spacer material over the vertical and horizontal surfaces of the memory device 10, an anisotropic etch may be used to preferentially remove the spacer material from the horizontal surfaces in a directional spacer etch. Thus, the spacer material is formed into spacers 48, *i.e.*, material extending from the

sidewalls of another material. As shown in Figure 5, spacers 48 are formed within the trench 46 and narrow it.

[0046] With reference to Figure 5B, a second hard mask layer 49 may then be deposited over the entire surface of the memory device 10. This layer of hard mask 49, also silicon nitride in a preferred embodiment, is preferably deposited to a thickness sufficient to fill the trench 46. Of course, the hard mask material 49 may be deposited by any of a number of suitable deposition processes, including CVD or PVD. After deposition of a sufficient amount of hard mask material 49, the excess that may have formed over the spacers 48 and over the other portions of previously deposited hard mask 42 may be removed by any of a number of processes well-known to those of skill in the art. For example, the surface of the device 10 may be planarized to the level of the dotted line of Figure 5B, such that the sidewalls of the remaining spacers 48 are nearly vertical. Any suitable planarization process, such as, for example, chemical mechanical planarization may be used.

[0047] The spacers 48 that are now exposed at the top surface of the memory device 10 may be stripped using any of a number of processes. In the illustrated embodiment, a process may be used that selectively strips polysilicon relative to silicon nitride. For example, in one embodiment, a selective wet etch may be used. The trenches formed where the spacers 48 have been etched are further deepened by a secondary etch that selectively etches the temporary layer 40 as well as the substrate 11. These trenches are also preferably formed using a directional process, such as, for example, ion milling or reactive ion etching.

[0048] Figure 6 illustrates the result of these processes, with openings or recesses in the form of trenches 50 separated by less than the minimum pitch possible using photolithographic techniques alone. Preferably the trenches 50 have a width at top between about 25 nm and 75 nm. Of course, a skilled artisan will appreciate that numerous other techniques for pitch multiplication may be used to arrive at the stage shown in Figure 6. Many such techniques will generally include a spacer process, by which physical deposition can achieve a smaller pitch than photolithographic techniques alone. The trenches 50 typically also have an aspect ratio greater than 1:1, and preferably greater than 2:1. Increased depth maximizes available volume and thence conductivity for the word lines, at the expense of difficulty in filling with a suitable material.

[0049] After formation of these trenches 50, the hard mask layer 42 is selectively stripped, by any of a number of methods well known to those of skill in the art. In Figure 7, a gate dielectric layer 54 is blanket deposited or thermally grown over the device, lining the inner surfaces of the trenches 50. The illustrated gate dielectric layer 54 comprises silicon oxide formed by thermal oxidation in a preferred embodiment, but can also be a deposited high K material in other embodiments. A layer of gate material 52, which comprises polysilicon in the illustrated embodiment, may then also be blanket deposited over the entire memory device 10. In one embodiment, the gate layer 52 completely fills the trenches 50 and forms a top surface of the device 10. In a preferred embodiment, this polysilicon is undoped.

[0050] After a series of doping steps to define the drains and sources of transistors, the undoped polysilicon in the trenches 50 is etched back until the top of the gate layer 52 resides beneath the top surface of the substrate 11. This stage of the process is shown in Figure 8. The recessed polysilicon 52 of Figure 8 can serve as the word lines and the gate electrodes for the memory cell transistors if appropriately doped.

[0051] Preferably, however, the gate electrodes in the arrays are formed of a more highly conductive material than traditional polysilicon gates. This is due to the fact that the recessed gates 12 (see Figures 1 and 2) are more narrow than the typical gate electrode. Metallic materials compensate, in whole or in part, for the small volume of the gates in the array, improving lateral signal propagation speed along the word lines. Thus, the undoped polysilicon of Figure 8 can be silicided after recessing by depositing metal thereover and reacting. Metal silicide can have better than 10 times the conductivity of doped polysilicon and demonstrate a suitable work function.

[0052] With reference to Figures 9-12, in another arrangement, rather than being recessed, the polysilicon 52 is initially etched back or planarized down to the gate oxide 54, thus isolating the polysilicon within the trenches 50 without recessing at this stage. The polysilicon of the gate layer 52 within the trenches 50 is subjected to a salicidation (self-aligned silicidation) reaction to form a layer of conductive material 56. A metal layer 55 (Figure 9) may be blanket deposited and an anneal step may form a silicide material 56 (Figure 12) wherever the metal contacts silicon, such as over the polysilicon gate layers 52. In one embodiment, the silicided material comprises silicon and one or more metals, such as, for example, tungsten, titanium, ruthenium, tantalum, cobalt or nickel. A selective metal etch removes the excess metal but does not remove the

silicide 56. The metal silicide 56 thereby forms a self-aligned layer that increases the lateral conductivity along the word line.

[0053] Preferably, the gate layer 52 is fully silicided to maximize lateral conductivity. Full reaction also assures silicide formation down to the bottom of the trenches 50. In the illustrated recessed access devices (RADs), the channel extends across not only the bottom of the gate, but also along the gate's sidewalls. Accordingly, incomplete silicidation would result in different work functions along the length of the RAD channel. Furthermore, full silicidation ensures similar gate work functions across the array, from array to array across a wafer, and from wafer to wafer. It has been found difficult, however, to achieve full silicidation within the tight confines of the illustrated trenches 50, with a single metal to form the conductive material 56. Either nickel or cobalt, for example, tends to form voids in the high-aspect ratio trenches 50. Other metals have demonstrated similar difficulties for full silicidation for recessed access devices. The skilled artisan will appreciate that full silicidation can be challenging for material within other types of recesses, such as contact openings or vias, stacked container shapes for capacitors, capacitor trenches, etc.

[0054] Without wanting to be bound by theory, the voiding appears to be caused by diffusion during the silicidation reaction, in combination with the tight confines of the high aspect ratio trenches 50. Silicon diffuses more readily in cobalt than cobalt does into silicon. Accordingly, silicon tends to migrate during the reaction, leaving voids in the trenches 50. Furthermore, a high temperature phase transformation anneal to convert the silicide from CoSi to the more stable $CoSi_2$. Nickel, on the other hand, diffuses more readily into silicon than silicon does into nickel and so also has a tendency to create voids during the reaction in which NiSi is converted into the $NiSi_2$ phase.

[0055] Accordingly, the metal layer 55 preferably comprises a mixture of metals, where at least two of the metals in the mixture have opposing diffusivities relative to silicon. For example, the metal layer 55 can comprise a mixture of nickel and cobalt, such that the directions of diffusion tend to balance each other and minimize the risk of voiding. In this example, the cobalt preferably comprises less than 50 at. % of the mixed metal 55, and more preferably the mixture comprises about 70-90 at. % Ni and about 10-30 at. % Co. Such a mixture of nickel and cobalt has been found to more readily accomplish full silicidation of the gate layer without voiding, thus increasing signal propagation speeds along the word line. In contrast to partial silicidation, fully silicided

word lines are not only more conductive, but also will ensure consistent work function along the length of the channel. Full silicidation will also demonstrate better consistency from device to device across an array, from array to array, or wafer to wafer, since partial silicidation will tend to leave inconsistent compositions depending upon local temperature variations, etc.

[0056] In one example, a sputtering target comprising 80% Ni and 20% Co is sputtered over the polysilicon 52 to produce the metal layer 55. The substrate is then subjected to a silicidation anneal. While a high temperature (e.g., 800°C) anneal is possible for a shorter time, preferably the anneal is conducted at lower temperatures for a longer time. For example, the substrate is annealed at 400-600°C for 25-35 minutes. In experiments, the silicidation anneal was conducted in a batch furnace under an N_2 environment at 500°C for 30 minutes.

[0057] In view of the disclosure herein, the skilled artisan can readily select other suitable mixtures of metals for full silicidation within trenches. Examples of metals that diffuse more readily in silicon than silicon does in that metal include Ni, Pt and Cu. Examples of metals in which silicon diffuses more readily than the metal diffuses in silicon include Co, Ti and Ta.

[0058] Figures 10A-11B are micrographs showing recessed, fully silicided $Ni_xCo_ySi_z$ gate material within 50 nm wide trenches lined with silicon oxide. Figures 10A and 10B show cross sections across the width of twin trenches, at two different magnifications. Figures 11A and 11B show cross sections along the length of one of the trenches, at two different magnifications. The trenches have a width at the top of about 50 nm and a depth of about 150 nm, such that the aspect ratio of these trenches was about 3:1. A smooth, uniform composition is observed, filling at least a lower portion of the trenches without voiding. In the example of Figures 11-12, after depositing the polysilicon 52 (Figure 7), the polysilicon can be etched back only to the gate dielectric top surface 54, thus isolating the silicon within the trenches without recessing.

[0059] Referring now to Figure 12, the silicided layers 56 can be recessed within the trenches and are then covered by a second insulating layer 58, such as silicon nitride. These insulating layers 58 may be deposited and then etched or planarized. The conductive material 56 thereby forms the word lines 12a, 12b of the completed memory device 10, and the word lines 12a, 12b are separated from the other circuit elements by the insulating layers 58. Thus, as would be well understood by those of skill in the art, the

word lines 12 have been pitch-multiplied, and have a pitch roughly one half of that possible simply using photolithographic techniques. Note, however, that certain aspects of the disclosure herein provide advantages whether or not the word lines are pitch-multiplied.

[0060] Of course, in other embodiments, the pitch-multiplication may take place by any of a variety of processes well-known to those skilled in the art.

[0061] The silicided layers 56 of the illustrated embodiment thus fill lower portions of the trenches 50, preferably filling greater than 50% of the trench heights, more preferably filling greater than 75% of the trench height. In the illustrated embodiment, about 70-90 at % of metal in the metal silicide 56 is nickel and about 10-30 at % of metal in the metal silicide is cobalt.

[0062] As will be appreciated by the skilled artisan, in a preferred embodiment, the logic in the periphery is preferably simultaneously defined as certain of the above steps are completed, thereby making the chip-making process more efficient. In particular, the silicon and metal deposition steps to define recessed word lines preferably simultaneously define gate electrodes over the substrate for the CMOS transistors in the periphery.

[0063] Referring to Figures 13-21, in accordance with another embodiment, different work functions and resistivity can be established for the simultaneously processed gate electrodes in the array and the logic regions in the periphery. In the illustrated embodiment, this is facilitated by etching array RAD trenches through a polysilicon layer, which forms part of the gate stack in the periphery.

[0064] With reference to Figure 13, a polysilicon layer 60 can be deposited over the substrate 11 prior to forming the trenches. The polysilicon layer 60 can be first deposited over a thin dielectric 54a (e.g., grown gate oxide). The substrate can then be patterned with a pitch-doubled mask (not shown), such as that described with respect to Figures 3-6. An etch stop layer 61 is also formed, in the illustrated embodiment comprising about 100-200 Å of TEOS-deposited oxide.

[0065] With reference to Figure 14, the trenches 50 are etched through the overlying etch stop layer 61, the polysilicon layer 60, the underlying dielectric 54a and the substrate 11. The gate dielectric 54b can then be formed over the exposed portions of the substrate 11, such as by oxidation of the trench walls. Due to the pre-existing etch stop

layer 61, no significant further oxide grows over the top surface of the polysilicon 60, as shown.

[0066] Subsequently, as shown in Figure 15, a metallic material 62 can be deposited over the polysilicon 60 and into the trenches 50. As described with respect to Figures 9-12, the trenches 50 are preferably filled with material more conductive than polysilicon. In the illustrated embodiment, the metallic material 62 comprises titanium nitride (TiN).

[0067] With reference to Figure 16, the metallic material 62 is preferably etched back or planarized to leave isolated lines of the conductive material 62 in the trenches 50, stopping on the oxide etch stop layer 61 (see Figure 15). Following etch back, the etch stop layer 61 overlying the polysilicon layer 60 is removed (e.g., using an HF dip for the preferred oxide material of the etch stop layer 61), while the dielectric layer 54b within the trenches 50 is protected by the metallic material 62. Subsequently, metallic layers 64, 66 are deposited over the silicon layer 60. As will be appreciated by the skilled artisan, the first dielectric layer 54a, the polysilicon layer 60, and the overlying metallic layers 64, 66 can serve as the transistor gate stack in the periphery. All these layers are deposited in both regions of interest (in the memory example, in both periphery and memory array regions). Polysilicon can be variably doped to establish a desired transistor work function, such that a single material deposition, and different doping steps, can be used to define gates for both NMOS and PMOS of a CMOS circuit. The overlying metallic layer 66 can serve to improve lateral signal propagation speeds along lines controlling the gates, and comprises tungsten (W) in the illustrated embodiment. The intervening metallic layer 64 can ensure physical and electrical compatibility (e.g., fulfilling adhesion and barrier functions) at the juncture between the polysilicon layer 60 and the overlying metallic layer 66, and in the illustrated embodiment comprises titanium nitride, and more particularly metal-rich metal nitride.

[0068] Referring to Figure 17, the gate stack also includes a cap layer 68, formed of silicon nitride in the illustrated embodiment. Figure 17 shows the trenches 50, filled with the metallic material 62, in a first or memory array region 70 of the substrate. The gate stacks layers 54a, 60, 64, 66 and 68 extend across both the array region 70 and the second or periphery or logic region 72 of the substrate. A photoresist mask 76 is configured for patterning transistor gates in the periphery 72.

[0069] As shown in Figure 18, a series of etch steps etches first through the cap layer 68, including a metal etch to remove the metallic layer(s) 64, 66. Chlorine-based reactive ion etch (RIE), for example, can selectively remove typical metallic materials, such as the illustrated tungsten strapping layer 66 and intervening metal nitride layer 64, while stopping on the underlying polysilicon layer 60. A high degree of selectivity enables continuing the metal etch after exposure of the polysilicon 60 until the metallic material 62 is recessed in the trenches 50, as shown.

[0070] Referring now to Figure 19, the etch chemistry can be switched following recessing of the metallic gate material 62 in the array trenches, and the silicon 60 can be patterned using the same mask 76, completing patterning of the gate stacks 80 for the periphery 72.

[0071] Referring now to Figure 20, following removals of the mask, a spacer layer 84 is deposited over the substrate, coating the gate stacks 80 conformally but filling the recesses at the top of the array trenches 50. In the illustrated embodiment, the spacer layer 84 comprises silicon nitride, but the skilled artisan will appreciate that a number of different insulating materials can be used.

[0072] As shown in Figure 21, a subsequent spacer etch (directional etch) leaves sidewall spacers 86 along sidewalls of the gate stacks 80, allowing self-aligned doping of source/drain areas. In the array 72, however, because the shallow recesses at the top of the trenches are filled with the spacer layer 84 (see Figure 20), the spacer etch merely etches the spacer material back in the array 72, leaving an insulating cap layer 88 burying the gate material 62 within the trenches 50.

[0073] The skilled artisan will appreciate that various doping steps for CMOS transistors, including source/drain, channel enhancement, gate electrode, lightly doped drain (LDD) and halo doping, are omitted in the description herein for simplicity.

[0074] The embodiment of Figures 13-21 thus facilitates simultaneous processing of transistors in the array and the periphery. In the illustrated embodiment, the array transistors are recessed access devices (RADs), whereas the peripheral gates are formed above the substrate 11 as conventional planar MOS transistors. While described in the context of conventional CMOS circuitry in the periphery, the skilled artisan will appreciate that the peripheral transistors can take other forms. Advantageously, in the illustrated embodiment, the metallic layer in the RAD trenches can be recessed at the same time as patterning the peripheral gate stacks. Furthermore, the peripheral sidewall

spacers are simultaneously formed with the insulating cap on the RAD gates or word lines.

[0075] Although not shown, it will be understood that conventional DRAM fabrication techniques may be used to create the other circuit elements shown in Figure 2. For example, different levels of doping may be used to form the drains 18 and source 20 of Figure 2, and the stacked storage capacitors 24 may be formed according to a plurality of deposition and masking steps.

[0076] As a result of the device layout and its method of manufacture, the completed memory device 10 shown in Figures 1 and 2 possesses a number of advantages in comparison to conventional DRAM. For example, the size of each memory cell and the overall size of the memory device 10 may be substantially reduced without a corresponding, substantial reduction in the distance between adjacent sense amplifiers. Moreover, the word lines 12 and digit lines 14 may have substantially different pitches, which enables the digit lines 14 to have far greater separation than the word lines 12. For example, in the preferred embodiment, the word lines 12 have an effective pitch of 1.5F, while the digit lines 14 may have a pitch of 3F. In addition, the steps for forming the digit lines 14 and word lines 12 are simplified by making them substantially linear and generally perpendicular to one another, while realizing space-savings by placing the active areas 16 at an angle to these elements. The word lines 12 in the preferred embodiment are also recessed, and, unlike the layout in conventional DRAM, there is no spacer using up valuable space between the gates and the sources or drains of the active areas (as may be easily seen in Figure 2). Thus, the memory device 10 may be made more dense.

[0077] Furthermore, the use of a mixture of metals facilitates full silicidation of the silicon buried within trenches 50 without the harmful formation of voids. Accordingly, a high conductivity can be achieved for the relatively small volume word lines.

[0078] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the invention. Indeed, the novel methods and devices described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and devices described herein may be made without departing from the spirit of the invention. The accompanying claims and

their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the invention.

We claim:

1. A method of forming a metal silicide structure in an integrated circuit, the method comprising:

providing a recess within a partially fabricated integrated circuit;

depositing silicon into the recess;

depositing a mixture of metals over the recess and in contact with the silicon, the mixture of metals comprising at least two metals having opposing diffusivities relative to silicon; and

reacting the mixture of metals with the silicon in the recess to form a metal silicide within the recess,

wherein the mixture of metals comprises 70-90 at. % nickel and 10-30 at. % cobalt, and wherein the recess has an aspect ratio of greater than 2:1.

2. A method of forming a recessed access device for an integrated circuit, the method comprising:

etching a trench with an aspect ratio greater than 2:1 in a semiconductor structure;

lining the trench with a dielectric layer;

at least partially filling the lined trench with silicon;

depositing a metal layer over the trench and in contact with the silicon; and

fully reacting the silicon within the trench in a silicidation reaction with the metal layer, wherein fully reacting is conducted without voiding, wherein depositing the metal layer comprises depositing a mixture of nickel and cobalt, and wherein the mixture comprises 70 to 90 at. % nickel and 10 to 30 at. % cobalt.

3. The method of Claim 1, wherein reacting comprises annealing the substrate at a temperature between 400°C and 600°C.

4. The method of Claim 1, wherein depositing the mixture of metals comprises simultaneously sputtering the at least two metals over the recess.

5. The method of Claim 4, further comprising forming a thin dielectric layer on surfaces within the recess prior to depositing silicon.

6. The method of Claim 5, wherein the recess defines a recessed access device for a memory array.

7. The method of Claim 6, wherein the recess is an elongated trench defining a word line for the memory array.

8. The method of Claim 7, wherein the recess has a width at a top of the trench between 25 nm and 75 nm.

9. The method of Claim 2, wherein at least partially filling the trench with silicon comprises depositing silicon and etching back the silicon to a top surface of the structure defining the trench.

10. The method of Claim 2, wherein at least partially filling the trench with silicon comprises etching back the silicon until it is recessed within the trench below a top surface of the structure defining the trench.

11. The method of Claim 2, wherein depositing the metal layer comprises sputtering a target comprising a fixed composition of nickel and cobalt.

12. The method of Claim 2, wherein etching a trench with an aspect ratio greater than 2:1 comprises etching a trench with an aspect ratio 3:1.