The invention is based on a recorder for digital signals in accordance with the first part of claim 1. A recorder of this type is known, as a so-called R-DAT (rotational digital audio tape) recorder for example.

Synchronising circuits are required for regenerating the bit, word and block timing rates for the processing of serial data signals in a recorder. Data signals, which stem from the scanning of a recording in subdivided tracks, generally have a run-in signal at the start and a run-out signal at the end of each track. These signal regions are intended, above all, to prevent the actual data signals from being detrimentally affected by any irregularities at the beginning and end of the tape/head contact. Moreover, synchronisation needs to be established during the run-in signal since this is lost by the change of heads.

A special run-in signal, which contains items of information for establishing the block synchronisation and for detecting the beginning of the data transmission, is described in DE-OS 35 33 962. The generation and evaluation of this run-in signal requires additional expenditure on circuitry. A start signal, from the head switching means for example, is supplied to the evaluating circuit for producing the block synchronisation at the beginning of each track.

The object of the invention is to simplify the synchronising circuit for generating the clock rate for the decoding during the reproduction.

This object is achieved by the invention defined in claim 1. Advantageous developments of the invention are specified in the appendant claims.

A special circuit for establishing the block synchronisation during the run-in signal is no longer then required. The same circuit as that which maintains the block synchronisation in the data region can be used. This maintenance circuit is started afresh, upon the occurrence of a drop out for example, if a synchronising signal does not fall in the region of a periodically opened timing window for a certain time. As a result of the missing synchronising signals in the run-out signal, the circuit is also started automatically at the beginning of each run-in signal and the establishment of the block synchronisation is thereby instituted in the run-in region. The supply of a special start signal at the beginning of each track, by the head switching means for example, is no longer required.

The circuit consequently no longer recognises the deviating bit pattern in the run-out signal as a synchronising signal. In principle, the type of deviation of the bit pattern from the

agreed bit pattern is quite arbitrary. It no longer has any function for the purposes of synchronisation since the track is in any case ended during the run-out signal and the synchronisation has to be instituted afresh at the beginning of the new track. A further advantage consists in that circuit elements, such as counters for example, which are already available in the synchronising circuit, can be used in order to institute, in good time, the measures which are required at the start of the track. The head switching voltage does not need to be supplied to the synchronising circuit. The simplification of the circuit thus also consists in that a contact (pin) for an integrated circuit or a conductive track on a circuit board is saved.

The US-A-4 777 542 manifests similar synchronisation patterns (2, 4) in the run-in signal and in the data blocks 3. Furthermore, the evaluation is likewise effected in such a way that the synchronisation is only carried out until a specific number of valid synchronisations have been carried out but that the synchronisation process is started up again if a synchronising pattern cannot be detected.

Run-in signals are not mentioned in the US-A-4 777 542 which does not relate to an R-DAT recorder using subdivided tracks. The simplification of the circuit achieved in accordance with the invention, in which a contact for the supply of the head switching voltage is saved (see page 2, last paragraph), thus cannot arise for the US-A-4 777 542 since the US-A-4 777 542 relates, rather, to a floppy disc control means.

The invention will be explained hereinafter with the help of the drawing. Therein

Fig. 1 shows the signal format of a data block,

Fig. 2 the signal format of a track and

Fig. 3 a block circuit diagram for effecting the synchronisation.

Figs. 1, 2 show a signal format for a helical track recording device for digital signals. Since an 8/10 modulation is provided for the transmission, each data block consists of (3+n)*10 bits, wherein a respective 2*10 bits form a predetermined pattern which serves for the purposes of synchronisation. The 10 ident bits indicate the data block number. n*10 bit data signals follow thereupon. Each track of the recording contains the run-in signal at the beginning, the data blocks in the middle and the run-out signal at the end. The run-in and run-out signal usually consists of a 0101 sequence. However, any other bit pattern which contains sufficiently many level transitions can be used. In accordance

with the invention, only the run-in signal contains synchronising signals corresponding to the data signals. Usually, the synchronising patterns are polarity independent in that they are characterised by the presence and absence of level transitions (NRZI coding).

Fig. 3 shows the basic circuit diagram of a synchronising circuit for the signal format in accordance with Figs. 1, 2. This circuit serves primarily for maintaining the synchronisation following the word and block synchronisation which was established during the run-in signal. The signal Do obtained from a recording medium by scanning and signal equalisation is supplied to the input of the circuit at the terminal 9. The bit rate fo is produced with the help of the PLL circuit 1. If Do is an NRZI signal, the conversion into the NRZ signal occurs in the stage 2. The shift register 3, which is clocked by fo, delivers, with each clock pulse, the last 19 successive bits to the 19 parallel inputs of the comparator 4 which serves for detecting the synchronising pattern. The comparator 4 emits a pulse So having a duration of one bit upon detecting the synchronising pattern. This pulse sets the counter 5, which serves for generating the word clock rate fw and the block clock rate fB, to a defined counting phase. Insofar as the pulse So originates from a correctly detected synchronising pattern, the clock signals fw and fB ensure the correct processing of the data signal which is supplied by the shift register 3 over 10 parallel leads to the 8/10 demodulator.

If the PLL circuit were to constantly deliver the correct bit rate, the synchronising process would only need to be carried out once at the beginning of each track. The counter 5 could thereafter run on uninterruptedly with this bit rate. The transmission of the synchronising pattern in the data region would then be superfluous. However, upon the occurrence of drop outs, there is the danger that the voltage controlled oscillator VCO in the PLL circuit would generate one or more oscillations too many or too few during the period of the drop out. Accordingly, the counter 5 is no longer in the correct counting phase so that the processing of the signals for the rest of the track is not possible if a correction of the synchronisation of the counter 5 is not effected.

Even if the synchronising pattern is selected such that it does not occur in the rest of the signal, the danger exists that, as a result of bit errors, a synchronising pattern is emulated which would then place the counter 5 in a wrong counting phase which would only then be corrected during the next, interference-free, regular synchronising pattern. In order to avoid disturbances of this type, the pulse So is supplied to the synchronising input of the counter 5 via the AND gate 8 which serves as a timing window. The window pulse UB or UF has the block frequency. With a correct

phase setting of the counter 5, the pulse So lies approximately in the centre of the window pulse. The duration of the window pulse depends on the synchronising pattern used and upon the magnitude of the bit slip which can be expected. A synchronising pattern having a length of n bits may, for example, be selected such that the emulation of a pattern displaced by ± n/2 bits due to interference is most unlikely. In the present case, the timing window for the correction of the synchronisation of the counter 5 may then only have a width of 20 bits so that bit slips of up to ± 10 bits are corrected by the next interference-free synchronising signal.

Two requirements have to be fulfilled for this circuit:

1. The timing window has to be ineffective at the beginning of each track since So will probably no longer be in the region of the window after the change of head.

2. The window has to be ineffective after each bit slip, due to which So falls outside the region of the window, in order to make compensation of the bit slip possible.

The logic circuit 6 and the counter 7 serve to fulfil these requirements. The voltage Uc at the output of the counter 7 is at the high level or "1" at the beginning of each track. The gate 8 is thereby not effective as a timing window so that each pulse So sets the counting phase of the counter 5. The logic circuit 6 contains a counter which is started by the rising edge of the voltage Uc. Moreover, this counter is reset each time that a pulse So does not appear during the period of the pulse UB. The counter thus counts the pulses So falling in the timing window in an uninterrupted sequence. The counter 7 is reset as soon as two successive pulses So are located in the timing window. This means that the voltage Uc goes to the low level or to the value "0". The gate 8 is thereby effective as a timing window.

From now on, the counter 7 counts the pulses UB. It is reset however by each pulse So which falls in the timing window. The counter 7 can only then reach the end state i.e. Uc = "1", if a pulse So does not fall in the timing window during a predetermined number m, e.g. m = 12, of pulses UB. One can assume in this case that a bit slip has occurred which was so great that the pulses So no longer fall in the timing window.

The counter 7 thus caters for the fulfilment of the requirement No. 2. In order to fulfil the requirement No. 1, the counter 7 is set to Uc = "1" at the beginning of each track. The signal required for this was previously obtained from the head switching voltage UD which had to be provided to the logic circuit 6 for this purpose.

This provision and the expense involved for the setting of the counter 7 to Uc = "1" can be saved if, in accordance with the invention, the run-in signal contains the synchronising pattern and the run-out signal does not contain a synchronising pattern. It is ensured in this case that the counter 7 automatically goes to Uc = "1" at about the end of the track. The effect of the head switching voltage is thus completely substituted for. The provision of this voltage is no longer required.

A special circuit is required for the evaluation of the synchronising information of the run-in signal in the method described in the DE-OS 35 33 962. The run-in signal specified there additionally contains an item of information for the advance determination of the beginning of the first data block. With the method in accordance with the invention, this item of information can be realised by suitable choice of the ident words in the run-in signal. If, for example, a modulo counter is used for counting the data blocks of the track, then the ident words in the run-in region have to be selected such that each of these words sets the counter such that this counter is at zero at the beginning of the first data block by continuing to count up the blocks. The positive determination of the first data block after the run-in signal then likewise no longer requires any additional expenditure on circuitry.

Claims

1. Recorder for recording digital signals subdivided over a plurality of tracks, wherein the length of each track is short compared with the length of the magnetic tape, including means for recording a run-in signal at the start of a track and a run-out signal at the end of a track and for the recording of synchronising signals which are arranged at regular intervals and which are for the marking of the data blocks which are arranged in the regions of the track located between the run-in signal and the run-out signal, characterised in that, the same synchronising signals as in the data region are recorded in the run-in region and no corresponding synchronising signals are recorded in the run-out region so that the bit patterns of the run-out signal in the time region of the synchronising signals deviate from the bit pattern of the synchronising signals.

2. Recorder in accordance with Claim 1, characterised in that, ident words are also recorded in the run-in region, which words are selected such that a counter for counting the data blocks can be set by each of these ident words such that, by continuing to count at the data block frequency, the counting interval upon reaching the data block region corresponds to the number of the relevant data block.

3. Reproduction circuit for digital signals recorded by a recorder in accordance with Claim 1 or 2 including a counter (5) for generating the data block frequency (fB) whose counting phase is set by the synchronising signals (So), characterised in that, there is provided a circuit (8) which makes the synchronising signals effective for synchronising the counter (5) only during the period of a timing window (UF), that the timing window is switched off and the synchronising signals thus become ineffective for the purposes of synchronisation on each occasion that no synchronising signals have fallen in the timing window for a specific time and that the timing window is switched on again after two or more synchronising signals (So) have been detected in the region of the timing window.

4. Reproduction circuit for a recorder in accordance with Claim 2 including a counter for counting the data blocks, characterised in that, the counter (5) is set during the run-in signal to the counting phase corresponding to the numbering of the data blocks.