

CYCLIC DEVELOPMENT OF METAL OXIDE BASED PHOTORESIST FOR ETCH STOP DETERRENCE

INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0002] The fabrication of semiconductor devices, such as integrated circuits, is a multi-step process involving photolithography. In general, the process includes the deposition of material on a wafer and patterning the material through lithographic techniques to form structural features (e.g., transistors and circuitry) of the semiconductor device. The steps of a typical photolithography process known in the art include: preparing the substrate; applying a photoresist, such as by spin coating; exposing the photoresist to light in a desired pattern, causing the exposed areas of the photoresist to become more or less soluble in a developer solution; developing by applying a developer solution to remove either the exposed or the unexposed areas of the photoresist; and subsequent processing to create features on the areas of the substrate from which the photoresist has been removed, such as by etching or material deposition.

[0003] One challenge in manufacturing devices having such small features is the ability to reliably, and reproducibly, create photolithographic masks of sufficient resolution. Current photolithography processes typically use 193 nm ultraviolet (UV) light to expose a photoresist. The fact that the light has a wavelength significantly greater than the desired size of the features to be produced on the semiconductor substrate creates inherent issues. Achieving feature sizes smaller than the wavelength of the light requires use of complex resolution enhancement techniques, such as multipatterning. Thus, there is significant interest and research effort in developing photolithographic techniques using shorter wavelength light, such as extreme ultraviolet radiation (EUV), having a wavelength of from 10 nm to 15 nm, e.g., 13.5 nm.

[0004] EUV photolithographic processes can present challenges, however, including low power output and loss of light during patterning. Traditional organic chemically amplified resists (CAR) similar to those used in 193 nm UV lithography have potential drawbacks when used in EUV lithography, particularly as they have low absorption coefficients in EUV region

and the diffusion of photo-activated chemical species can result in blur or line edge roughness. Furthermore, in order to provide the etch resistance required to pattern underlying device layers, small features patterned in conventional CAR materials can result in high aspect ratios at risk of pattern collapse. Accordingly, there remains a need for improved EUV photoresist materials, having such properties as decreased thickness, greater absorbance, and greater etch resistance.

[0005] The background description provided herein is for the purpose of generally presenting the context of the present technology. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present technology.

SUMMARY

[0006] Provided are processes for development of metal or metal oxide-based thin film photoresists post-EUV exposure for removal of non-volatile species and deterring etch stop. Repeated cycles of alternating treatment with an etchant and an oxidizing agent; or treatment with an etchant followed by treatment with a wash agent are effective techniques for removal of the undesired unexposed portion of a photoresist.

[0007] Accordingly, in a first aspect, the present invention encompasses a method for processing a semiconductor substrate. In some embodiments, the method of includes providing a photopatterned metal-containing resist on a semiconductor substrate on a pedestal in a process chamber; and developing the photopatterned metal-containing resist by selectively removing a portion of the photopatterned metal-containing resist by exposing the photopatterned metal-containing resist to at least one cycle including a pulse of an etchant and a pulse of an oxidizing agent, delivered alternately, to form a resist mask.

[0008] In some embodiments, the pulse of the etchant and the pulse of the oxidizing agent are temporally separate.

[0009] In some embodiments, the pedestal is at a first temperature during the pulse of the etchant; and the oxidizing agent is delivered to the process chamber at a second temperature.

[0010] In some embodiments, the pedestal is at a first temperature during the pulse of the etchant and the pedestal is at a second temperature during the pulse of the oxidizing agent.

[0011] In some embodiments, a duration of the pulse of the etchant is from about 1 to about 120 seconds and a duration of the pulse of the oxidizing agent is from about 1 to about 120 seconds.

[0012] In some embodiments, the first temperature is from about -60°C to about 120°C.

[0013] In some embodiments, the second temperature is from about 20°C to about 150 °C.

[0014] In some embodiments, the second temperature is from about 50°C to about 250 °C.

[0015] In some embodiments, non-volatile byproducts of the pulse of the etchant are removed from the photopatterned metal-containing resist.

[0016] In some embodiments, the photopatterned metal-containing resist is an organo-metal oxide, a metal oxide, a metal or an organo-metal.

[0017] In some embodiments, the metal oxide is a tin oxide.

[0018] In some embodiments, the etchant is a halide etchant.

[0019] In some embodiments, the halide etchant is a hydrogen halide, hydrogen gas and halogen gas, an organic halide, an acyl halide, a carbonyl halide, a thionyl halide or a combination thereof.

[0020] In some embodiments, the halide etchant is hydrogen fluoride, hydrogen chloride, boron trichloride, hydrogen bromide, hydrogen iodide or a combination thereof.

[0021] In some embodiments, the etchant is an etchant plasma.

[0022] In some embodiments, the etchant plasma is generated remotely.

[0023] In some embodiments, the oxidizing agent is oxygen, ozone, hydrogen peroxide, water, nitrous oxide, nitric oxide, nitrogen dioxide, nitric acid, sulfur dioxide, chlorine, fluorine, bromine, iodine or a combination thereof.

[0024] In some embodiments, the oxidizing agent is a gaseous oxidizing agent of water and oxygen or chlorine.

[0025] In some embodiments, the oxidizing agent is an oxidizing agent plasma.

[0026] In some embodiments, the oxidizing agent plasma is generated remotely.

[0027] In some embodiments, the method also includes exposing the photopatterned metal-containing resist to an inert plasma gas.

[0028] In some embodiments, the method also includes purging the process chamber with an inert gas between the pulse of the etchant and the pulse of the oxidizing agent or after a cycle of a pulse of the etchant and a pulse of the oxidizing agent.

[0029] In some embodiments, developing the photopatterned metal-containing resist by exposure to alternating pulses of an etchant and an oxidizing agent is dry developing the photopatterned metal-containing resist.

[0030] In some embodiments, developing the photopatterned metal-containing resist by exposure to alternating pulses of an etchant and an oxidizing agent is wet developing the photopatterned metal-containing resist.

[0031] In some embodiments, each cycle has the same etchant pulse duration.

[0032] In a second aspect, the present invention encompasses a method of processing a semiconductor substrate. In some embodiments, the method includes providing a photopatterned metal-containing resist on a semiconductor substrate on a pedestal in a process chamber; and developing the photopatterned metal-containing resist by selectively removing a portion of the photopatterned metal-containing resist by exposing the photopatterned metal-containing resist to an etchant, followed by subsequent exposure to a wash agent, to form a resist mask.

[0033] In some embodiments, the wash agent is water, methanol, ethanol, isopropanol, acetone, acetonitrile, tetrahydrofuran, dimethyl sulfide or a combination thereof.

[0034] In some embodiments, a pedestal temperature is from about 10°C to about 50 °C during exposure to the wash agent.

[0035] In some embodiments, the wash agent is a supercritical fluid.

[0036] In some embodiments, the supercritical fluid is a low surface tension supercritical liquid.

[0037] In some embodiments, the low surface tension supercritical liquid is carbon dioxide, sulfur dioxide, dimethyl ether or a combination thereof.

[0038] In some embodiments, a process chamber pressure is from about 5 psi to about 3,000 psi during exposure to the wash agent.

[0039] In some embodiments, non-volatile byproducts from etchant exposure are removed from the photopatterned metal-containing resist.

[0040] In some embodiments, the photopatterned metal-containing resist is an organo-metal oxide, a metal, a metal oxide or an organo-metal.

[0041] In some embodiments, the metal oxide is a tin oxide.

[0042] In some embodiments, the etchant is a halide etchant.

[0043] In some embodiments, the halide etchant is a hydrogen halide, hydrogen gas and halogen gas, an organic halide, an acyl halide, a carbonyl halide, a thionyl halide or a combination thereof.

[0044] In some embodiments, the halide etchant is hydrogen fluoride, hydrogen chloride, boron trichloride, hydrogen bromide, hydrogen iodide or a combination thereof.

[0045] In some embodiments, the etchant is an etchant plasma.

[0046] In some embodiments, the etchant plasma is generated remotely.

[0047] In a third aspect, the present invention encompasses a method of promoting atomic layer etching on a substrate. In some embodiments, the method includes providing a

photopatterned metal-containing resist on a semiconductor substrate on a pedestal in a process chamber; and developing the photopatterned metal-containing resist by selectively removing a portion of the resist by exposing the photopatterned metal-containing resist to at least one cycle including a pulse of an etchant and a pulse of an oxidizing agent, delivered alternately, to form a resist mask; whereby etch stop due to non-volatile byproducts of the etchant pulse is eliminated.

[0048] In a fourth aspect, the present invention encompasses a method of processing a semiconductor substrate. In some embodiments, the method includes providing a dry-deposited photopatterned metal oxide EUV resist on a semiconductor substrate on a pedestal in a process chamber; and dry developing the photopatterned metal oxide EUV resist by selectively removing an EUV-unexposed portion of the EUV resist by exposure to at least one cycle including a pulse of an etchant and a pulse of an oxidizing agent, delivered alternately, to form a resist hard mask.

[0049] In a fifth aspect, the present invention encompasses an apparatus for conducting development of resist. In some embodiments, the apparatus includes a process chamber with a substrate support; a vacuum line coupled to the process chamber; etchant and oxidizing agents lines coupled to the process chamber; and a controller configured with instructions for processing a semiconductor substrate, the instructions including code for: providing a photopatterned metal-containing resist on a semiconductor substrate in a process chamber; and developing the photopatterned metal-containing resist by selectively removing a portion of the resist by exposure to at least one cycle of an etchant pulse and an oxidizing agent pulse, delivered alternately, to form a resist mask.

[0050] In some embodiments, the photopatterned metal-containing resist is a photopatterned metal-containing EUV resist, and wherein the controller configured with instructions including code for developing the photopatterned metal-containing EUV resist has code for selectively removing an EUV-unexposed portion of the EUV resist relative to an EUV-exposed portion with at least one cycle of an etchant pulse and an oxidizing agent pulse, delivered alternately, to form the resist mask.

[0051] In some embodiments, the apparatus also includes one or more heaters coupled to the substrate support, wherein the one or more heaters include a plurality of independently controllable temperature control zones.

[0052] In some embodiments, the apparatus also includes heated oxidizing agent delivery lines.

[0054] These and other features of the disclosed embodiments will be described in detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0055] **FIG. 1** presents a flow diagram of an example cyclic method for depositing and developing a photoresist in accordance with certain disclosed embodiments.

[0056] **FIG. 2** illustrates a pulse sequence for a hydrogen bromide (HBr) etchant and a chlorine (Cl₂) oxidizing agent for developing a photoresist in accordance with certain disclosed embodiments.

[0057] **FIG. 3A** shows a graph of chlorine oxidizing agent effect on residual byproduct thickness as temperature is varied in accordance with certain disclosed embodiments.

[0058] **FIG. 3B** shows a graph of hydrogen bromide etchant effect on residual byproduct thickness as the total exposure time of etchant is fixed but the etchant pulse duration of each cycle is varied in accordance with certain disclosed embodiments.

[0059] **FIG. 3C** shows a graph of chlorine oxidizing agent effect on residual byproduct thickness as oxidizing agent pulse duration is varied in accordance with certain disclosed embodiments.

[0060] **FIG. 4** shows scanning electron microscopy (SEM) images of a photopatterned substrate subjected to dry deposition with an etchant (single DD) in comparison to a photopatterned substrate subjected to cyclic dry development with etchant and chlorine oxidizing agent (cyclic DD) in accordance with certain disclosed embodiments.

[0061] **FIG. 5** shows a graphical comparison of the dry deposition with an etchant (single DD) in comparison to cyclic dry development with etchant and air oxidizing agent (cyclic DD) in accordance with certain disclosed embodiments.

[0062] **FIG. 6** presents a flow diagram of an example method for depositing and developing a photoresist utilizing an etchant in conjunction with a wash agent in accordance with certain disclosed embodiments.

[0063] **FIG. 7** depicts a schematic illustration of an example process station for maintaining a low-pressure environment that is suitable for performing the methods in accordance with certain disclosed embodiments.

[0064] **FIG. 8** depicts a schematic illustration of an example multi-station processing tool suitable for implementation of various operations in accordance with certain disclosed embodiments.

[0065] FIG. 9 shows a cross-sectional schematic view of an example inductively-coupled plasma apparatus for implementing certain operations in accordance with certain disclosed embodiments.

[0066] FIG. 10 depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition and patterning modules that interface with a vacuum transfer module, suitable for implementations of methods in accordance with certain disclosed embodiments.

DETAILED DESCRIPTION

[0067] In the following description, numerous specific details are set forth to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. While the disclosed embodiments will be described in conjunction with the specific embodiments, it will be understood that it is not intended to limit the disclosed embodiments.

[0068] The implementations disclosed below describe deposition of a material on a substrate such as a wafer, substrate, or other work piece. The work piece may be of various shapes, sizes, and materials. In this application, the terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate,” and “partially fabricated integrated circuit” are used interchangeably. One of ordinary skill in the art would understand that the term “partially fabricated integrated circuit” can refer to a silicon wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, or 300 mm, or 450 mm. Unless otherwise stated, the processing details recited herein (e.g., flow rates, power levels, etc.) are relevant for processing 300 mm diameter substrates, or for treating chambers that are configured to process 300 mm diameter substrates and can be scaled as appropriate for substrates or chambers of other sizes. In addition to semiconductor wafers, other work pieces that may be used implementations disclosed herein include various articles such as printed circuit boards and the like. The processes and apparatuses can be used in the fabrication of semiconductor devices, displays, LEDs, photovoltaic panels and the like.

[0069] By halide is meant an anion of F, Cl, Br or I.

[0070] As used herein, the term “about” means +/-10% of any recited value, unless otherwise specified. As used herein, this term modifies any recited value, range of values, or endpoints of one or more ranges.

[0071] As used herein, the terms “top,” “bottom,” “upper,” “lower,” “above,” and “below” are used to provide a relative relationship between structures. The use of these terms does not indicate or require that a particular structure must be located at a particular location in the apparatus.

[0072] As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A OR B OR C), using a non-exclusive logical OR, and should not be construed to mean ‘at least one of A, at least one of B, and at least one of C.’

[0073] By “atomic layer deposition” (ALD) is meant a vapor deposition process in which deposition cycles, preferably a plurality of consecutive deposition cycles, are conducted in a process chamber (i.e., a deposition chamber). Typically, during each cycle, the precursor is chemisorbed to a deposition surface (i.e., a substrate assembly surface or a previously deposited underlying surface such as material from a previous ALD cycle) forming a monolayer or sub-monolayer that does not readily react with additional precursor (i.e., a self-limiting reaction). Thereafter, if necessary, a reactant (i.e., another precursor or reaction gas) may be introduced into the process chamber for use in converting the chemisorbed precursor to the desired material on the deposition surface. Typically, this reactant is capable of reaction with the already chemisorbed precursor. Further, purging steps may also be utilized during each cycle to remove excess precursor from the process chamber and/or remove excess reactant and/or reaction by-products from the process chamber after conversion of the chemisorbed precursor.

[0074] By “deposition” or “vapor deposition” is meant a process in which a metal layer is formed on one or more surfaces of a substrate from vaporized precursor composition(s) including one or more metal containing compounds. The metal-containing compounds are vaporized and directed to and/or contacted with one or more surfaces of a substrate (i.e., semiconductor substrate or semiconductor assembly) placed in a deposition chamber. Typically, the substrate is heated. These metal containing compounds form a non-volatile, thin, uniform metal-containing layer on the surface(s) of the substrate. One operation of the method is one cycle, and the process can be repeated for as many cycles necessary to obtain the desired metal thickness.

[0075] By “etchant” is meant any compound used to remove a material such as a layer, byproduct or contaminant from a surface.

[0076] By “water” is meant a material which may include a substrate and a substrate layer to be etched. In some embodiments, the substrate layer includes an ashable hard mask such as spin-on carbon (SoC) or other material, e.g., silicon, silicon oxide, silicon nitride, silicon carbide, etc. In some embodiments, the substrate layer may be a layer stack disposed on the substrate.

[0077] By “photopatterned metal-containing resist film” is meant a thin film which may have an organo-metal-containing layer disposed on a substrate layer to be etched. The photopatterned metal-containing EUV resist film may have a thickness between about 5 nm and about 50 nm or between about 10 nm and about 30 nm. The photopatterned metal-containing EUV resist film may be provided in a process chamber after photopatterning in an EUV scanner and/or after a PEB treatment as described above. The photopatterned metal-containing EUV resist film includes non-EUV exposed regions and EUV exposed regions. Non-EUV exposed regions of the photopatterned metal-containing EUV resist film can be removed in a dry development process by exposure to flows of dry development chemistry without striking a plasma. The dry development chemistry may include a halide-containing chemistry such as a hydrogen halide or hydrogen and halogen gas. A resist mask is formed after development by removal of the non-EUV exposed regions. Thereafter, the substrate layer to be etched may be etched using the resist mask to provide the desired structure.

[0078] By “byproduct” is meant any compound which may be an impurity, a decomposition product or contaminant of the gas being delivered to the deposition chamber.

[0079] By “delivery lines” is meant any process equipment such as piping, tubes, or conduits that may be utilized to transport or convey a gas (e.g., reactant(s) and/or precursor(s)). In the semiconductor manufacturing process, precursor delivery lines may be used to transport precursors to a deposition chamber and may be formed from stainless steel or nickel alloys.

[0080] This disclosure relates generally to the field of semiconductor processing. In some aspects, the disclosure is directed to processes and apparatuses for development of photoresists (e.g., EUV-sensitive metal and/or metal oxide-containing photoresists) using etchants 1) in combination with an oxidizing agent in a cyclic dry development process, or 2) in combination with a wash agent, to form a patterning mask in the context of EUV patterning. Such processes may advantageously widen the process window of dry development and/or may extend the applicability of dry development to different metal or metal-oxide based photoresist systems.

[0081] Reference is made herein in detail to specific embodiments of the disclosure. Examples of the specific embodiments are illustrated in the accompanying drawings. While the disclosure will be described in conjunction with these specific embodiments, it will be understood that it is not intended to limit the disclosure to such specific embodiments. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the disclosure. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. The present disclosure may be practiced without some or all of these specific details. In other

instances, well known process operations have not been described in detail so as to not unnecessarily obscure the present disclosure.

[0082] Patterning of thin films in semiconductor processing is often an important step in the fabrication of semiconductors. Patterning involves lithography. In conventional photolithography, such as 193 nm photolithography, patterns are printed by emitting photons from a photon source onto a mask and printing the pattern onto a photosensitive photoresist, thereby causing a chemical reaction in the photoresist that, after development, removes certain portions of the photoresist to form the pattern.

[0083] Advanced technology nodes (as defined by the International Technology Roadmap for Semiconductors) include nodes 22 nm, 16 nm, and beyond. In the 16 nm node, for example, the width of a typical via or line in a Damascene structure is typically no greater than about 30 nm. Scaling of features on advanced semiconductor integrated circuits (ICs) and other devices is driving lithography to improve resolution.

[0084] Extreme ultraviolet (EUV) lithography can extend lithography technology by moving to smaller imaging source wavelengths than would be achievable with conventional photolithography methods. EUV light sources at approximately 10–20 nm, or 11–14 nm wavelength, for example 13.5 nm wavelength, can be used for leading-edge lithography tools, also referred to as scanners. The EUV radiation is strongly absorbed in a wide range of solid and fluid materials including quartz and water vapor, and so operates in a vacuum.

[0085] EUV lithography makes use of EUV resists that are patterned to form masks for use in etching underlying layers. EUV resists may be polymer-based chemically amplified resists (CARs) produced by liquid-based spin-on techniques. An alternative to CARs is directly photopatternable metal oxide-containing films, such as those available from Inpria, Corvallis, OR, and described, for example, in US Patent Publications US 2017/0102612, US 2016/021660 and US 2016/0116839, incorporated by reference herein at least for their disclosure of photopatternable metal oxide-containing films. Such films may be produced by spin-on techniques or dry vapor-deposited. The metal oxide-containing film can be patterned directly (i.e., without the use of a separate photoresist) by EUV exposure in a vacuum ambient providing sub-30 nm patterning resolution, for example as described in US Patent 9,996,004, issued June 12, 2018 and titled EUV PHOTOPATTERNING OF VAPOR-DEPOSITED METAL OXIDE-CONTAINING HARDMASKS, and/or in Application PCT/US19/31618, filed May 9, 2019, and titled METHODS FOR MAKING EUV PATTERNABLE HARD MASKS, the disclosures of which at least relating to the composition, deposition, and patterning of directly photopatternable metal oxide films to form

EUV resist masks is incorporated by reference herein. Generally, the patterning involves exposure of the EUV resist with EUV radiation to form a photo pattern in the resist, followed by development to remove a portion of the resist according to the photo pattern to form the mask.

[0086] It should also be understood that the while present disclosure relates to lithographic patterning techniques and materials exemplified by EUV lithography, it is also applicable to other next generation lithographic techniques. In addition to EUV, which includes the standard 13.5 nm EUV wavelength currently in use and development, the radiation sources most relevant to such lithography are DUV (deep-UV), which generally refers to use of 248 nm or 193 nm excimer laser sources, X-ray, which formally includes EUV at the lower energy range of the X-ray range, as well as e-beam, which can cover a wide energy range. The specific methods may depend on the particular materials and applications used in the semiconductor substrate and ultimate semiconducting device. Thus, the methods described in this application are merely exemplary of the methods and materials that may be used in present technology.

[0087] Directly photopatternable EUV resists may be composed of or contain metals and/or metal oxides mixed within organic components. The metals/metal oxides are highly promising in that they can enhance the EUV photon adsorption and generate secondary electrons and/or show increased etch selectivity to an underlying film stack and device layers. To date, these resists have been developed using a wet (solvent) approach, which requires the wafer to move to the track, where it is exposed to developing solvent, dried and baked. Wet development does not only limit productivity but can also lead to line collapse due to surface tension effects and/or delamination.

[0088] Dry development techniques have been proposed to overcome these issues by eliminating substrate delamination and interface failures. Dry development can improve performance (e.g., prevent line collapse due to surface tension and delamination in wet development) and enhance throughput (e.g., by avoiding wet development track). Other advantages may include eliminating the use of organic solvent developers, reduced sensitivity to adhesion issues, increased EUV absorption for improved dose efficiency, and a lack of solubility-based limitations. Dry development can also provide more tunability and give further critical dimension (CD) control and scum removal.

[0089] Dry development has its own challenges, including etch selectivity between unexposed and EUV exposed resist material which can lead to a higher dose to size requirement for effective resist exposure when compared to wet development. Suboptimal selectivity can also

cause PR corner rounding due to longer exposures under etching gas, which may increase line CD variation in the following transfer etch step.

Development of EUV Resist

[0090] According to various aspects of the present disclosure, a photopatterned metal-containing photoresist is developed by exposure to halide-containing chemistries. An EUV-sensitive metal or metal oxide-containing film, e.g., an organotin oxide, is disposed on a semiconductor substrate. The EUV-sensitive metal or metal oxide-containing film is patterned directly by EUV exposure in vacuum ambient. A pattern is then developed to form a resist mask using a development chemistry. In some embodiments, the development chemistry is a dry development chemistry. In some embodiments, the dry development chemistry includes hydrogen and a halide. Such dry development techniques may be done while using either a gentle plasma (high pressure, low power) or a thermal process while flowing a hydrogen and halide dry development chemistry. This disclosure provides processes and apparatus configured for development of a metal-containing resist as part of a resist mask formation process.

[0091] Metal and/or metal oxide photoresists are attractive material candidates for advanced photolithography. Their capability to operate with higher resolution, high etch selectivity and lower dose enables photo adsorption enhancement and secondary electrons generation. After EUV exposure, a wet development is conventionally applied to remove undesired materials. However, this process may lead to increased defects due to interface failure and/or line collapse caused by surface tension.

[0092] A dry development helps overcome these issues by eliminating substrate delamination and interface failures. Yet the complete removal of undesired unexposed portion of photoresist relies on the generation of a volatile and stable byproduct of dry development. The volatility and stability of byproducts from dry development may be impacted by the organic ligands utilized in the metal and/or metal oxide photoresist system. In some cases, the byproduct is either non-volatile, or volatile but non-stable. If the byproduct is volatile but non-stable, it can further decompose into a non-volatile species. Non-volatile byproducts result in an etch stop and incomplete development, increasing the risk of high surface roughness and defect formation.

[0093] An optional post-application bake (PAB) is performed after deposition of the EUV-patternable film and prior to EUV exposure. The PAB treatment may involve a combination of thermal treatment, chemical exposure, and moisture to increase the EUV sensitivity of the EUV-patternable film, reducing the EUV dose to develop a pattern in the EUV-patternable

film. The PAB treatment temperature may be tuned and optimized for increasing the sensitivity of the EUV-patternable film. For example, the treatment temperature may be between about 90°C and about 200°C or between about 150°C and about 190°C. In some embodiments, the PAB treatment may be conducted with a pressure between atmospheric and vacuum, and a treatment duration of about 1 to 15 minutes, for example about 2 minutes. In some embodiments, the PAB treatment is conducted at a temperature between about 100°C to 200°C for about 1 minute to 2 minutes.

[0094] The metal-containing EUV resist film is exposed to EUV radiation to develop a pattern. Generally speaking, the EUV exposure causes a change in the chemical composition and cross-linking in the metal-containing EUV resist film, creating a contrast in etch selectivity that can be exploited for subsequent development.

[0095] The metal-containing EUV resist film may then be patterned by exposing a region of the film to EUV light, typically under relatively high vacuum. EUV devices and imaging methods among those useful herein include methods known in the art. In particular, as discussed above, exposed areas of the film are created through EUV patterning that have altered physical or chemical properties relative to unexposed areas. For example, in exposed areas, metal-carbon bond cleavage may occur, as through a beta-hydride elimination, leaving behind reactive and accessible metal hydride functionality that can be converted to hydroxide and cross-linked metal oxide moieties via metal-oxygen bridges during a subsequent post-exposure bake (PEB) step. This process can be used to create chemical contrast for development as a negative tone resist. In general, a greater number of beta-H in the alkyl group results in a more sensitive film. This can also be explained as weaker Sn-C bonding with more branching. Following exposure, the metal-containing EUV resist film may be baked, so as to cause additional cross-linking of the metal oxide film. The difference in properties between exposed and unexposed areas may be exploited in subsequent processing, such as to dissolve unexposed areas or to deposit materials on the exposed areas. For example, the pattern can be developed using a dry method to form a metal oxide-containing mask.

[0096] In particular, in various embodiments, the hydrocarbyl-terminated tin oxide present on the surface is converted to hydrogen-terminated tin oxide in the exposed region(s) of an imaging layer, particularly when the exposure is performed in a vacuum using EUV. However, removing exposed imaging layers from vacuum into air, or the controlled introduction of oxygen, ozone, H₂O₂, or water, can result in the oxidation of surface Sn-H into Sn-OH. The difference in properties between exposed and unexposed regions may be exploited in subsequent processing, such as by reacting the irradiated region, the unirradiated region, or

both, with one or more reagents to selectively add material to or remove material from the imaging layer.

[0097] Without limiting the mechanism, function or utility of present technology, EUV exposure, for example, at doses of from 10 mJ/cm² to 100 mJ/cm² results in the cleavage of Sn- C bonds resulting in loss of the alkyl substituent, alleviating steric hindrance and allowing the low-density film to collapse. In addition, reactive metal-H bond generated in the beta-hydride elimination reactions can react with neighboring active groups such as hydroxyls in the film, leading to further cross-linking and densification, and creating chemical contrast between exposed and unexposed region(s).

[0098] Following exposure of the metal-containing EUV resist film to EUV light, a photopatterned metal-containing EUV resist is provided. The photopatterned metal-containing EUV resist includes EUV-exposed and unexposed regions.

[0099] An optional post-exposure bake (PEB) is performed to further increase contrast in etch selectivity of the photopatterned metal-containing EUV resist. The photopatterned metal-containing EUV resist can be thermally treated in the presence of various chemical species to facilitate cross-linking of the EUV-exposed regions or simply baked on a hot plate in ambient air, for example between 150°C and 250°C for between one and five minutes (e.g., 190°C for two minutes).

[0100] In various embodiments, a bake strategy involves careful control of the bake ambient, introduction of reactive gases, and/or careful control of the ramping rate of the bake temperature. Examples of useful reactive gases include e.g., air, H₂O, H₂O₂ vapor, CO₂, CO, O₂, O₃, CH₄, CH₃OH, N₂, H₂, NH₃, N₂O, NO, alcohol, acetyl acetone, formic acid, Ar, He, or their mixtures. The PEB treatment is designed to (1) drive complete evaporation of organic fragments that are generated during EUV exposure and (2) oxidize any Sn-H, Sn-Sn, or Sn radical species generated by EUV exposure into metal hydroxide, and (3) facilitate cross-linking between neighboring Sn-OH groups to form a more densely crosslinked SnO₂-like network. The bake temperature is carefully selected to achieve optimal EUV lithographic performance. Too low a PEB temperature would lead to insufficient cross-linking, and consequently less chemical contrast for development at a given dose. Too high a PEB temperature would also have detrimental impacts, including severe oxidation and film shrinkage in the unexposed region (the region that is removed by development of the patterned film to form the mask in this example), as well as, undesired interdiffusion at the interface between the photopatterned metal-containing EUV resist and an underlayer, both of which can contribute to loss of chemical contrast and an increase in defect density due to insoluble scum.

The PEB treatment temperature may be between about 100°C and about 300°C, between about 170°C and about 290°C, or between about 200°C and about 240°C. In some embodiments, the PEB treatment may be conducted with a pressure between atmospheric and vacuum, and a treatment duration of about 1 to 15 minutes, for example about 2 minutes. In some embodiments, PEB thermal treatment may be repeated to further increase etch selectivity.

[0101] The photopatterned metal-containing EUV resist is developed to form a resist mask. In various embodiments, the exposed regions are removed (positive tone) or the unexposed regions are removed (negative tone). In some embodiments, development may include selective deposition on either the exposed or unexposed regions of the photopatterned metal-containing EUV resist, followed by an etching operation. In various embodiments, these processes may be dry processes or wet processes. The development may be done without striking a plasma in some embodiments. Or development may be done with flows of hydrogen and halide (e.g., H₂ and Cl₂ and/or Br₂) activated in a remote plasma source or activated by exposure to remote UV radiation. The photoresist for development may include an element selected from the group consisting of tin, hafnium, tellurium, bismuth, indium, antimony, iodine, and germanium. The element may have a high patterning radiation-absorption cross-section. In some embodiments, the element may have a high EUV-absorption cross-section. In some embodiments, the metal-containing EUV resist may have an overall absorption greater than 30%. In an all-dry lithography process, this provides more efficient utilization of EUV photons, enabling development of thicker and more EUV-opaque resists.

[0102] Examples of processes for development involve an organotin oxide-containing EUV-sensitive photoresist thin film (e.g., 10–30 nm thick, such as 20 nm), subjected to a EUV exposure dose and post-exposure bake, and then developed. The photoresist film may be, for example, deposited based on a gas phase reaction of an organotin precursor such as isopropyl(tris)(dimethylamino)tin and water vapor, or may be a spin-on film comprising tin clusters in an organic matrix.

[0103] The photopatterned metal-containing EUV resist is developed by exposure to a development chemistry, where the development chemistry is a halide-containing chemistry. In some embodiments, the development chemistry includes hydrogen and halide, such as a hydrogen halide (e.g., HBr or HCl) or hydrogen and halogen gases (e.g., H₂ and Cl₂). In some embodiments, the development chemistry includes a hydrogen halide, hydrogen and halogen gases, boron trichloride, or combinations thereof. Development of the EUV resist can be done by wet development using halide-containing chemistries or dry development using hydrogen halide-containing chemistries. In embodiments where the EUV resist is developed using wet

development, the wet development may be combined with other wet processing operations such as wet deposition (e.g., spin-on deposition) of the metal-containing EUV resist film. Alternatively, the wet development may be combined with other dry processing operations such as vapor deposition (e.g., CVD) of the metal-containing EUV resist film. In embodiments where the EUV resist is developed using dry development, the dry development may be combined with other dry processing operations such as dry deposition (e.g., CVD) of the metal-containing EUV resist film. In alternative embodiments where the EUV resist is developed using dry development, the dry development may be combined with other wet processing operations such as wet deposition (e.g., spin-on deposition) of the metal-containing EUV resist film.

[0104] In some embodiments, processing of the semiconductor substrate may combine all dry steps including film formation by vapor deposition, EUV lithographic patterning, and dry development. In fact, each of the operations 102–112 in the process 100 may be dry processing operations. Such processing operations may avoid material and productivity costs associated with wet processing operations such as wet development. Dry processing can provide more tunability and add further critical dimension (CD) control and scum removal. Wet processing generally involves moisture and/or oxygen, which more easily leads to scum formation. Wet development is limited by solubility and cluster size, whereas dry development is not limited by solubility and cluster size. Wet development is more prone to pattern collapse and delamination issues that dry development avoids. In addition, employing all-dry processing operations may facilitate integration within interconnected vacuum processing chamber without exposure to and contamination by ambient air or trace contaminants contained therein. For example, the PEB thermal treatment during which exposed regions undergo further crosslinking may be conducted in the same chamber as development, though it will be understood that the PEB thermal treatment may be performed in another chamber.

[0105] Development processes can be done by delivering development chemistry in a liquid or vapor phase. In some embodiments, dry development processes can be done by using either a gentle plasma (high pressure, low power) or a thermal process while flowing a hydrogen halide-containing dry development chemistry such as HF, HCl, HBr, or HI. For example, dry development can be carried out in a thermal process using dry development chemistry such as HCl or HBr. In some embodiments, the hydrogen halide-containing chemistry is able to quickly remove the unexposed material, leaving behind a pattern of the exposed film that can be transferred into the underlying layers by plasma-based etch processes, for example conventional etch processes.

[0106] In thermal development processes, the substrate is exposed to development chemistry (e.g., a Lewis Acid) in a process chamber (e.g., oven). In some embodiments, a vacuum line is coupled to the process chamber for pressure control, and a development chemistry line may be coupled to the process chamber for delivery of development chemistry into the process chamber. The process chamber may include one or more heaters for temperature control, such as heaters coupled to a substrate support in the process chamber for substrate temperature control. In some embodiments, the chamber interior can be coated with corrosion resistant films, such as organic polymers or inorganic coatings. One such coating is polytetrafluoroethylene (PTFE), e.g., Teflon 1M. Such materials can be used in thermal processes of this disclosure without risk of removal by plasma exposure.

[0107] In thermal development processes, the photopatterned metal-containing EUV resist is exposed to development chemistry at a temperature that is optimized for etch selectivity between exposed and unexposed regions. Lower temperatures may increase contrast in etch selectivity while higher temperatures may decrease contrast in etch selectivity. In some embodiments, a temperature may be between about -60°C and about 120°C, between about -20°C and about 60°C, or between about -20°C and about 20°C, such as about -10°C. Chamber pressure may be tuned, where chamber pressure may influence etch selectivity between exposed and unexposed regions during development. In some embodiments, the chamber pressure may be relatively low and accompanied without dilution, where the chamber pressure may be between about 0.1 mTorr and about 300 mTorr, between about 0.2 mTorr and about 100 mTorr, or between about 0.5 mTorr and about 50 mTorr. In some embodiments, the chamber pressure may be between about 20 mTorr and about 800 mTorr, or between about 20 mTorr and about 500 mTorr, such as about 300 mTorr. In some embodiments, the chamber pressure may be relatively high with high flow and accompanied by dilution, where the chamber pressure may be between about 100 Torr and about 760 Torr or between about 200 Torr and about 760 Torr. Reactant flow rate may be tuned, where reactant flow may influence etch selectivity between exposed and unexposed regions during development. In some embodiments, reactant flow may be between about 50 sccm and about 2000 sccm, between about 100 sccm and about 2000 sccm, or between about 100 sccm and about 1000 sccm, such as about 500 sccm. In instances with high flow, reactant flow may be between about 1 L and about 10 L. Duration of exposure may be tuned in the thermal development process. The duration of exposure may depend on how much resist is desired to be removed, development chemistry, amount of crosslinking in the resist, and composition and properties of the resist, among other factors. In some embodiments, duration of exposure may be between about 5

seconds and about 5 minutes, between about 10 seconds and about 3 minutes, or between about 10 seconds and about 1 minute.

[0108] Thermal development processes may expose the photopatterned metal-containing EUV resist to certain halide-containing chemistries in the vapor or liquid phase. In some embodiments, the development chemistry includes a hydrogen halide, hydrogen and halogen gas, boron trichloride, an organic halide, an acyl halide, a carbonyl halide, a thionyl halide, or mixtures thereof. A hydrogen halide can include but is not limited to HF, HCl, HBr, and HI. For example, the hydrogen halide can be HCl or HBr. Hydrogen and halogen gas can include but is not limited to hydrogen gas (H₂) mixed with F₂, Cl₂, Br₂, or I₂. Boron trichloride (BCl₃) may be used in combination with any of the aforementioned hydrogen halides or hydrogen and halogen gases. An organic halide can include but is not limited to C_xH_yF_z, C_xH_yCl_z, C_xH_yBr_z, and C_xH_yI_z, where x, y, and z are values equal to or greater than 0. An acyl halide can include but is not limited to CH₃COF, CH₃COCl, CH₃COBr, and CH₃COI. A carbonyl halide can include but is not limited to COF₂, COCl₂, COBr₂, and COI₂. A thionyl halide can include but is not limited to SOF₂, SOCl₂, SOBr₂, and SOI₂. In some embodiments, the halide-containing chemistry may be flowed with or without inert/carrier gas such as He, Ne, Ar, Xe, and N₂.

[0109] In the formation of semiconductor devices, various layers may be selectively etched. Atomic layer etching may be used to provide an etch with high selectivity. In an atomic layer etch (ALE), a cyclical process is provided. The cyclical process may have a first step of modifying part of an etch layer and a second step of removing the modified part of the etch layer. Such an ALE may use a self-limiting process to modify part of the etch layer. The self-limiting process may modify a few monolayers of the etch layer forming a self-limiting layer. In such a case, the removing of the modified part of the etch layer may remove just a few atomic layers of the etch layer. As a result, many cycles are needed in order to etch a substantial part of the etch layer. Each cycle may be more than 12 seconds long. As a result, an ALE process may take a long time in order to etch a substantial part of an etch layer.

[0110] ALE processes used to etch carbon containing etch layers, such as amorphous carbon, use low bias voltages. In such processes, the low bias voltages may be applied for several seconds in order to provide an ALE while preventing or reducing sputtering caused by higher biases. Some of the drawbacks to such processes using a low bias are that such ALE processes are slower and the ions under a low bias for the ALE process are not highly directional. Since the ions are not highly directional, the resulting features do not have a high height to width aspect ratio.

[0111] Atomic layer etching processes are described in US Patent 10,566,212, entitled “Designer Atomic Layer Etching,” by Kanarik, issued February 18, 2020; US 10,763,083, entitled “High Energy Atomic Layer Etching,” by Yang et al., issued September 1, 2020; US 2021/0005425A1, entitled “Atomic Layer Etching and Smoothing of Refractory Metals and Other High Surface Binding Energy Materials,” by Yang et al., published January 2, 2021; WO 2020/223152A1, entitled “Atomic Layer Etching for Subtractive Metal Etch,” by Yang et al., published on November 5, 2020; and U.S. Provisional Patent Application Serial No. 63/322,535, entitled “Fast Atomic Layer Etch”, filed on March 22, 2022, which are all incorporated by references for all purposes.

[0112] The thermal development process may be done without plasma. By applying a non-plasma thermal approach, productivity can be significantly improved as multiple wafers can be batch developed, at the same time in a low-cost thermal vacuum chamber/oven. However, in some embodiments, the thermal development process may be followed by exposure to plasma. Subsequent exposure to plasma may occur for desorption, descumming, smoothing, or other processing operations.

[0113] In plasma development processes, the photopatterned metal-containing EUV resist is exposed to development chemistry including radicals/ions of one or more gases. A process chamber for processing the semiconductor substrate may be a plasma-generating chamber or coupled to a plasma-generating chamber remote from the process chamber. Dry development may occur by remote plasma in some embodiments. The plasma-generating chamber may be an inductively-coupled plasma (ICP) reactor, transformer-coupled plasma (TCP) reactor, or capacitively-coupled plasma (CCP) reactor, employing equipment and techniques among those known in the art. An electromagnetic field acts on the one or more gases to produce a plasma in the plasma-generating chamber. Ions and/or radicals from the remote plasma may interact with the photopatterned metal-containing EUV resist. In some embodiments, a vacuum line is coupled to the process chamber for pressure control, and a development chemistry line may be coupled to the plasma-generating chamber for delivery of the one or more gases into the plasma-generating chamber. The process chamber may include one or more heaters for temperature control, such as heaters coupled to a substrate support in the process chamber for substrate temperature control. In some embodiments, the process chamber interior can be coated with corrosion resistant films, such as organic polymers or inorganic coatings. One such coating is polytetrafluoroethylene (PTFE), e.g., Teflon 1M. Such materials can be used in thermal processes of this disclosure without risk of removal by plasma exposure.

[0114] In plasma development processes, the photopatterned metal-containing EUV resist is exposed to remote plasma under conditions that are optimized for etch selectivity between exposed and unexposed regions. The conditions may be optimized for generating a gentle plasma, where a gentle plasma can be characterized by high pressure and low power. Chamber pressure may be tuned, where chamber pressure may influence etch selectivity between exposed and unexposed regions during development. In some embodiments, the chamber pressure may be equal to or greater than about 5 mTorr, or equal to or greater than about 15 mTorr. In some embodiments, the chamber pressure may be relatively high with high flow and accompanied by dilution, where the chamber pressure may be between about 100 Torr and about 760 Torr or between about 200 Torr and about 760 Torr. RF power levels may be tuned, where RF power may affect etch selectivity, roughness, descumming, and other characteristics of development. In some embodiments, the RF power may be equal to or less than about 1000 W, equal to or less than about 800 W, or equal to or less than about 500 W. Temperature may be tuned, where temperature may influence various aspects of development such as etch selectivity. In some embodiments, a temperature may be between about -60°C and about 300°C, between about 0°C and about 300°C, or between about 30°C and about 120°C. Gas flow rate may be tuned, where gas flow may influence etch selectivity between exposed and unexposed regions during development. In some embodiments, gas flow rate is between about 50 sccm and about 2000 sccm, between about 100 sccm and about 2000 sccm, or between about 200 sccm and about 1000 sccm, such as about 500 sccm. Duration of exposure may be tuned in the plasma development process. The duration of exposure may depend on how much resist is desired to be removed, development chemistry, amount of crosslinking in the resist, and composition and properties of the resist, among other factors. In some embodiments, duration of exposure may be between about 1 second and about 50 minutes, between about 3 seconds and about 20 minutes, or between about 10 seconds and about 6 minutes.

[0115] Plasma development processes may expose the photopatterned metal-containing EUV resist to radicals of certain halide-containing gases. In some embodiments, the radicals are generated from a remote plasma source. For example, the plasma development may expose the photopatterned metal-containing EUV resist to radicals of hydrogen and halide gases generated from the remote plasma source. In some embodiments, a halide-containing gas includes a hydrogen halide, hydrogen and halogen gas, boron trichloride, an organic halide, an acyl halide, a carbonyl halide, a thionyl halide, or mixtures thereof. A hydrogen halide can include but is not limited to hydrogen fluoride (HF), hydrogen chloride (HCl), hydrogen bromide (HBr), and hydrogen iodide (HI). For example, the hydrogen halide may be HCl or

HBr. Hydrogen and halogen gas can include but is not limited to hydrogen gas (H_2) mixed with fluorine gas (F_2), chlorine gas (Cl_2), bromine gas (Br_2), or iodine gas (I_2). An organic halide can include but is not limited to $C_xH_yF_z$, $C_xH_yCl_z$, $C_xH_yBr_z$, and $C_xH_yI_z$, where x, y, and z are values equal to or greater than 0. An acyl halide can include but is not limited to CH_3COF , CH_3COCl , CH_3COBr , and CH_3COI . A carbonyl halide can include but is not limited to COF_2 , $COCl_2$, $COBr_2$, and COI_2 . A thionyl halide can include but is not limited to SOF_2 , $SOCl_2$, $SOBr_2$, and SOI_2 . In some embodiments, the halide-containing gas may be flowed with or without inert/carrier gas such as He, Ne, Ar, Xe, and N_2 .

[0116] In addition, or in the alternative to plasma activation, activation of the one or more gases in a dry development process may occur by photoactivation. In some embodiments, the photoactivation may be achieved by exposure to ultraviolet (UV) radiation. For example, the process chamber may include a lamp such as a UV lamp configured to generate UV radiation. Exposing the one or more gases to UV radiation may generate radicals of the one or more gases that can be used in dry development of the photopatterned metal-containing EUV resist. Exposure of the one or more gases to UV radiation may occur in a manner without exposing the photopatterned resist to UV radiation. In other words, the photopatterned resist is out-of-sight with respect to the UV lamp. Hence, the UV lamp may be remote from the process chamber or positioned in a manner that avoids exposing the photopatterned resist to UV radiation.

[0117] It will be understood that the aforementioned methods of thermal development, plasma development, and photoactivation development may be combined together. Such development methods may be applied simultaneously or sequentially. The development methods may be applied while flowing dry development chemistry in the liquid or vapor phase, where the dry development chemistry can include a compound of the formula R_xZ_y , where $R = B, Al, Si, C, S, SO$ with $x > 0$ and $Z = Cl, H, Br, F, CH_4$ and $y > 0$. The development can result in a positive or a negative tone, in which the R_xZ_y species selectively removes either the unexposed or the exposed material, leaving behind the exposed or unexposed counterpart as a mask.

[0118] As described above, etch selectivity during dry development is tunable by controlling process conditions such as temperature, pressure, gas flow, gas composition, and plasma power, among other tunable process conditions. Tuning etch selectivity in a single step or multiple steps may achieve desired patterned characteristics. In some embodiments, etch selectivity during dry development is tuned across one or more steps to influence EUV resist profile. More specifically, the amount of taper or a re-entrant angle in the EUV resist profile can be controlled by applying development chemistry of different etch selectivity over one or

more steps. Descumming, photoresist reworking, curing, smoothing, and cleaning operations may also be tuned according to a tunable etch selectivity.

[0119] FIG. 1 presents a flow diagram of an example method for depositing and developing a photoresist according to some embodiments. The operations of a process 100 may be performed in different orders and/or with different, fewer, or additional operations. One or more operations of the process 100 may be performed using an apparatus described in any one of **FIGS. 7-10**. In some embodiments, the operations of the process 100 may be implemented, at least in part, according to software stored in one or more non-transitory computer readable media.

[0120] In operation 102 of the process 100, a photopatterned metal containing resist is provided. The resist may be deposited either by a dry deposition process such as a vapor deposition process or by a wet process such as a spin-on deposition process.

[0121] The photoresist may be a metal-containing EUV resist. An EUV-sensitive metal or metal oxide-containing film may be deposited on a semiconductor substrate by any suitable technique, including wet (e.g., spin-on) or dry (e.g., CVD) deposition techniques. For example, described processes have been demonstrated for EUV photoresist compositions based on organotin oxides, being applicable to both commercially spin-coatable formulations and formulations applied using dry vacuum deposition techniques, further described below.

[0122] Semiconductor substrates may include any material construct suitable for photolithographic processing, particularly for the production of integrated circuits and other semiconducting devices. In some embodiments, semiconductor substrates are silicon wafers. Semiconductor substrates may be silicon wafers upon which features have been created ("underlying features"), having an irregular surface topography. As referred to herein, the "surface" is a surface onto which a film of the present disclosure is to be deposited or that is to be exposed to EUV during processing. Underlying features may include regions in which material has been removed (e.g., by etching) or regions in which materials have been added (e.g., by deposition) during processing prior to conducting a method of this disclosure. Such prior processing may include methods of this disclosure or other processing methods in an iterative process by which two or more layers of features are formed on the substrate.

[0123] EUV-sensitive thin films may be deposited on the semiconductor substrate, such films being operable as resists for subsequent EUV lithography and processing. Such EUV-sensitive thin films comprise materials which, upon exposure to EUV, undergo changes, such as the loss of bulky pendant substituents bonded to metal atoms in low density M-OH rich materials, allowing their crosslinking to denser M-O-M bonded metal oxide materials. Through EUV

patterning, areas of the film are created that have altered physical or chemical properties relative to unexposed areas. These properties may be exploited in subsequent processing, such as to dissolve either unexposed or exposed areas, or to selectively deposit materials on either the exposed or unexposed areas. In some embodiments, the unexposed film has a more hydrophobic surface than the exposed film under the conditions at which such subsequent processing is performed. For example, the removal of material may be performed by leveraging differences in chemical composition, density and cross-linking of the film. Removal may be by wet processing or dry processing, as further described below.

[0124] The thin films are, in various embodiments, organometallic materials, for example organotin materials comprising tin oxide, or other metal oxide materials/moieties. The organometallic compounds may be made in a vapor phase reaction of an organometallic precursor with a counter reactant. In various embodiments, the organometallic compounds are formed through mixing specific combinations of organometallic precursors having bulky alkyl groups or fluoroalkyl groups with counter-reactants and polymerizing the mixture in the vapor phase to produce a low-density, EUV-sensitive material that deposits onto the semiconductor substrate.

[0125] In various embodiments, organometallic precursors comprise at least one alkyl group on each metal atom that can survive the vapor-phase reaction, while other ligands or ions coordinated to the metal atom can be replaced by the counter-reactants. Organometallic precursors include those of the formula:



wherein: M is an element with a high patterning radiation-absorption cross-section; R is alkyl, such as C_nH_{2n+1} , preferably wherein $n \geq 2$; L is a ligand, ion or other moiety which is reactive with the counter-reactant; $a \geq 1$; $b \geq 1$; and $c \geq 1$.

[0126] In various embodiments, M has an atomic absorption cross section equal to or greater than $1 \times 10^7 \text{ cm}^2/\text{mol}$. M may be, for example, selected from the group consisting of tin, hafnium, tellurium, bismuth, indium, antimony, germanium, and combinations thereof. In some embodiments, M is tin. R may be fluorinated, e.g., having the formula $C_nF_xH_{(2n+1)}$. In various embodiments, R has at least one beta-hydrogen or beta-fluorine. For example, R may be selected from the group consisting of ethyl, i-propyl, n-propyl, t-butyl, i-butyl, n-butyl, sec-butyl, n-pentyl, i-pentyl, t-pentyl, sec-pentyl, and mixtures thereof. L may be any moiety readily displaced by a counter-reactant to generate an M-OH moiety, such as a moiety selected

from the group consisting of amines (such as dialkylamino, monoalkylamino), alkoxy, carboxylates, halogens, and mixtures thereof.

[0127] Organometallic precursors may be any of a wide variety of candidate metal-organic precursors. For example, where M is tin, such precursors include t-butyl tris(dimethylamino) tin, i-butyl tris(dimethylamino) tin, n-butyl tris(dimethylamino) tin, sec-butyl tris(dimethylamino) tin, i-propyl(tris)dimethylamino tin, n-propyl tris(dimethylamino) tin, ethyl tris(dimethylamino) tin and analogous alkyl(tris)(t-butoxy) tin compounds such as t-butyl tris(t-butoxy) tin. In some embodiments, the organometallic precursors are partially fluorinated.

[0128] Counter-reactants have the ability to replace the reactive moieties, ligands or ions (e.g., L in Formula 1, above) so as to link at least two metal atoms via chemical bonding. Counter-reactants can include water, peroxides (e.g., hydrogen peroxide), di- or polyhydroxy alcohols, fluorinated di- or polyhydroxy alcohols, fluorinated glycols, and other sources of hydroxyl moieties. In various embodiments, a counter-reactant reacts with the organometallic precursor by forming oxygen bridges between neighboring metal atoms. Other potential counter-reactants include hydrogen sulfide and hydrogen disulfide, which can crosslink metal atoms via sulfur bridges.

[0129] The thin films may include optional materials in addition to an organometallic precursor and counter-reactants to modify the chemical or physical properties of the film, such as to modify the sensitivity of the film to EUV or enhancing etch resistance. Such optional materials may be introduced, such as by doping during vapor phase formation prior to deposition on the semiconductor substrate, after deposition of the thin film, or both. In some embodiments, a gentle remote H₂ plasma may be introduced so as to replace some Sn-L bonds with Sn-H, which can increase reactivity of the resist under EUV.

[0130] In various embodiments, the EUV-patternable films are made and deposited on the semiconductor substrate using vapor deposition equipment and processes among those known in the art. In such processes, the polymerized organometallic material is formed in vapor phase or *in situ* on the surface of the semiconductor substrate. Suitable processes include, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), and ALD with a CVD component, such as a discontinuous, ALD-like process in which metal precursors and counter-reactants are separated in either time or space.

[0131] In general, methods comprise mixing a vapor stream of an organometallic precursor with a vapor stream of a counter-reactant so as to form a polymerized organometallic material, and depositing the organometallic material onto the surface of the semiconductor substrate. In

some embodiments, more than one organometallic precursor is included in the vapor stream. In some embodiments, more than one counter-reactant is included in the vapor stream. As will be understood by one of ordinary skill in the art, the mixing and depositing aspects of the process may be concurrent, in a substantially continuous process.

[0132] In an example continuous CVD process, two or more gas streams, in separate inlet paths, of organometallic precursor and source of counter-reactant are introduced to the deposition chamber of a CVD apparatus, where they mix and react in the gas phase, to form agglomerated polymeric materials (e.g., via metal-oxygen-metal bond formation). The streams may be introduced, for example, using separate injection inlets or a dual-plenum showerhead. The apparatus is configured so that the streams of organometallic precursor and counter-reactant are mixed in the chamber, allowing the organometallic precursor and counter-reactant to react to form a polymerized organometallic material. Without limiting the mechanism, function, or utility of present technology, it is believed that the product from such vapor-phase reaction becomes heavier in molecular weight as metal atoms are crosslinked by counter-reactants, and is then condensed or otherwise deposited onto the semiconductor substrate. In various embodiments, the steric hindrance of the bulky alkyl groups prevents the formation of densely packed network and produces smooth, amorphous, low-density films.

[0133] The CVD process is generally conducted at reduced pressures, such as from 10 milliTorr to 10 Torr. In some embodiments, the process is conducted at from 0.5 to 2 Torr. In some embodiments, the temperature of the semiconductor substrate is at or below the temperature of the reactant streams. For example, the substrate temperature may be from 0°C to 250°C, or from ambient temperature (e.g., 23°C) to 150°C. In various processes, deposition of the polymerized organometallic material on the substrate occurs at rates inversely proportional to surface temperature.

[0134] In some embodiments, the EUV-patternable films are made and deposited on the semiconductor substrate using wet deposition equipment and processes among those known in the art. For example, the organometallic material is formed by spin-coating on the surface of the semiconductor substrate.

[0135] The thickness of the EUV-patternable film formed on the surface of the semiconductor substrate may vary according to the surface characteristics, materials used, and processing conditions. In various embodiments, the film thickness may range from 0.5 nm to 100 nm, and may be a sufficient thickness to absorb most of the EUV light under the conditions of EUV patterning. The EUV-patternable film may be able to accommodate absorption equal to or greater than 30%, thereby having significantly fewer EUV photons available towards the

bottom of the EUV-patternable film. Higher EUV absorption leads to more cross-linking and densification near the top of an EUV-exposed film compared to the bottom of the EUV-exposed film. Though insufficient cross-linking may cause the resist to be more prone to liftoff or collapse in wet development, such as risk is not as present in dry development. An all-dry lithography approach may facilitate more efficient utilization of EUV photons by more opaque resist films. Though efficient utilization of EUV photons may occur with EUV-patternable films having higher overall absorption, it will be understood that in some instances, the EUV-patternable film may be less than about 30%. For comparison, the maximum overall absorption of most other resist films is less than 30% (e.g., 10% or less, or 5% or less) so that the resist material at the bottom of the resist film is sufficiently exposed. In some embodiments, the film thickness is from 10 nm to 40 nm or from 10 nm to 20 nm. Without limiting the mechanism, function, or utility of present disclosure, it is believed that, unlike wet, spin-coating processes of the art, the processes of the present disclosure have fewer restrictions on the surface adhesion properties of the substrate, and therefore can be applied to a wide variety of substrates. Moreover, as discussed above, the deposited films may closely conform to surface features, providing advantages in forming masks over substrates, such as substrates having underlying features, without "filling in" or otherwise planarizing such features.

[0136] Returning to **FIG. 1**, in operation 104, the photopatterned metal-containing resist is exposed to a pulse of etchant. A pulse as used herein refers to a specific amount of gas flow for a specified period of time. In some embodiments, the etchant pulse duration is from about 1 to about 120 seconds. In some embodiments, the etchant pulse duration is from about 5 to about 30 seconds. In some embodiments, the etchant pulse duration is from about 1 to about 20 seconds. In some embodiments, the etchant flow rate is from about 50 to about 3,000 sccm.

[0137] In some embodiments, operation 104 is a thermal process, wherein the etchant is delivered to the process chamber in gas form. In other embodiments, the etchant may be delivered to the process chamber in plasma form. The etchant plasma may include reactive species such as electrons, positive ions, neutral species, radicals and other plasma species. In some embodiments, the etchant is a halide etchant such as hydrogen bromide or hydrogen chloride; or a mixture of hydrogen and halogen such as hydrogen and chlorine (Cl₂) or hydrogen and bromine (Br₂).

[0138] Operation 104 can be done by using either a gentle plasma (high pressure, low power) or a thermal process while flowing a dry development etchant such as BCl₃ (boron trichloride) or other Lewis Acid. In some embodiments, BCl₃ is able to quickly remove the unexposed

material, leaving behind a pattern of the exposed film that can be transferred into the underlying layers by plasma-based etch processes, for example conventional etch processes.

[0139] Plasma processes include transformer coupled plasma (TCP), inductively coupled plasma (ICP) or capacitively coupled plasma (CCP), employing equipment and techniques among those known in the art. For example, a process may be conducted at a pressure of >5 mT (e.g., > 15 mT), at a power level of <1000 W (e.g., <500 W). Temperatures may be from 0 to 300 °C (e.g., 30 to 120 °C), at flow rate of 100 to 1000 standard cubic centimeters per minute (sccm), e.g., about 500 sccm, for from 1 to 3000 seconds (e.g., $10 - 600$ seconds).

[0140] In thermal development processes, the substrate is exposed to dry development chemistry (e.g., a Lewis Acid) in a vacuum chamber (e.g., oven). Suitable chambers can include a vacuum line, a dry development chemistry gas (e.g., BCl_3) line, and heaters for temperature control. In some embodiments, the chamber interior can be coated with corrosion resistant films, such as organic polymers or inorganic coatings. One such coating is polytetrafluoroethylene (PTFE), e.g., Teflon 1M). Such materials can be used in thermal processes of this technology without risk of removal by plasma exposure.

[0141] During the etchant pulse, the pressure of the process chamber may be from about 5 mTorr to about 1 Torr in some embodiments. In some embodiments, the pedestal temperature in the process chamber may be from about -60 °C to about 120 °C during the etchant pulse. Moreover, the etch selectivity can be tuned from between $5:1$ to greater than $50:1$ between the unexposed and EUV exposed photoresist by adjusting gas flow, hydrogen to halogen ratio, pressure, temperature or RF power.

[0142] In operation 106, an optional purge is performed after the exposure to etchant by flowing an inert carrier gas through the process chamber in some embodiments. Purge or carrier gases are selected to be non-reactive with the etchant. Gases such as helium, argon, nitrogen or combinations thereof may be utilized.

[0143] In operation 108, the resist etched in operation 104 is cleaned with a pulse of an oxidizing agent. The oxidizing agent is used to clear non-volatile byproducts which may be formed during the etchant pulse which create an undesirable etch stop on the resist. The non-volatile by-products are etch resistant residues, and can impede further processing. In some embodiments, the non-volatile byproducts are at the bottom of the unexposed photoresist. Treatment with oxidizing agent can render the non-volatile byproducts volatile, thus enabling further etching.

[0144] The oxidizing agent may be oxygen, ozone, hydrogen peroxide, water, nitrous oxide, nitric oxide, nitrogen dioxide, nitric acid, sulfur dioxide, chlorine, fluorine, bromine, iodine or

a combination thereof. In some embodiments, the oxidizing agent is air; water and oxygen; or chlorine (Cl_2).

[0145] In some embodiments, operation 108 is a thermal process, wherein the oxidizing agent is delivered to the process chamber in gas form. In other embodiments, the oxidizing agent may be delivered to the process chamber in plasma form. The etchant plasma may include reactive species such as electrons, positive ions, neutral species, radicals and other plasma species.

[0146] In some embodiments, operation 108 occurs at a higher temperature than operation 104. The elevated temperature may be achieved either by delivering the oxidizing agent as a hot gas, or by heating the pedestal in the process chamber to a second temperature higher than the first temperature utilized for operation 104. If delivered as a hot gas, the temperature of the gas may be from about 50°C to about 250°C . If the pedestal of the process chamber is heated for the oxidizing agent pulse, the pedestal may be heated to a temperature of from about 20°C to about 150°C .

[0147] In operation 108, an oxidizing agent is delivered as a pulse, for a certain duration of time at a certain flow rate. The duration of the pulse may be from about 1 to about 60 seconds. The ratio of oxidizing agent to etchant may be 1:1. In some embodiments, the oxidizing agent flow rate is from about 50 to about 3,000 sccm.

[0148] Operation 108 and operation 104 are temporally separate pulses, meaning pulses separated in time. A pulse of etchant in operation 104 and a pulse of oxidizing agent delivered to the process chamber is one cycle. The cycle 114 can be repeated as many times as desired to effect complete byproduct removal. In addition, the etchant and oxidizing agent delivery for every cycle may have the same pulse duration; or the pulse durations may be varied after a specified number of cycles. The timing of the pulse sequencing of exemplary etchant HBr and exemplary oxidizing agent Cl_2 with optional argon purge with relationship to temperature is illustrated in graphically in **FIG. 2**.

[0149] Returning to **FIG. 1**, in operation 110, an optional purge may be performed after one cycle of operations 104 and operation 108 by flowing an inert carrier gas through the process chamber in some embodiments. Purge or carrier gases are selected to be non-reactive with the etchant. Gases such as helium, argon, nitrogen or combinations thereof may be utilized. If the optional purge is utilized after a cycle, the next cycle begins with exposure to an etchant as illustrated at 116.

[0150] In operation 112, a resist mask is formed. Plasma may be utilized to help harden the exposed photoresist.

[0151] In some instances, there may be residue or scum remaining after development. Residue may result from slower etching components in less homogeneous EUV resist formulations, including those applied by spin-coating techniques. Such scum may contain high metal concentrations, which may be problematic during subsequent pattern transfer.

[0152] Additionally, or alternatively, roughness may form after development on sidewalls of etched features in a developed pattern. Some of this may be attributed to stochastics or non-optimal Gaussian distribution of the light resulting in partially or fully exposed material in areas where the resist should remain unexposed or vice versa.

[0153] In some embodiments, dry development may be accompanied by a descum/smoothing operation. In some embodiments, a descumming and smoothing operation may be an inert gas plasma desorption operation. For example, the inert gas plasma desorption operation may be a helium plasma desorption operation. The inert gas plasma desorption operation may be performed after dry development or cycled with dry development.

[0154] Various embodiments include combining all dry operations by vapor deposition, EUV lithographic patterning, and dry development. Various other embodiments include a combination of wet and dry processing operations, for example, spin-on EUV photoresists (wet process) may be combined with dry development or other wet or dry processes as described herein. Also described are various post-deposition (or post-application) processes such as bevel and backside cleaning, chamber cleaning, descum, smoothing, and curing to modify and enhance film characteristics, and photoresist rework processing.

[0155] **FIGS 3A - 3C** are graphical illustrations for some parameters of certain embodiments of the methods described herein. **FIG. 3A** demonstrates that without any oxidizing agent, etch stop occurs and a remaining thickness of an initial 25 nm thick EUV unexposed layer is 10 nm. Higher purge temperature of Cl₂ oxidizing agent is more effective for byproduct removal.

[0156] **FIG. 3B** illustrates that a shorter pulse of HBr etchant at a 20°C process temperature with a greater number of cycles, in conjunction with Cl₂ oxidizing agent pulses in a cyclic dry development process leads to greater removal of byproducts.

[0157] **FIG. 3C** illustrates that longer Cl₂ oxidizing agent purge times at 40°C process temperature, in conjunction with HBr etchant pulses in a cyclic dry development process, are more effective at reducing remaining thickness.

[0158] **FIG. 4** shows scanning electron microscopic images of patterned photoresist surfaces, comparing a conventional dry development utilizing only an etchant in comparison to a cyclic dry development process with sequential, alternating pulses of etchant and oxidizing agent. HBr etchant was utilized under the process conditions of: a 500 sccm flow rate, 300 mTorr

pressure and 20°C temperature. A cleaner unexposed area in both open and dense area and better edge roughness are achieved after applying 5 cycles of the cyclic dry development process.

[0159] FIG. 5 illustrates the limitations of a single dry development process (HBr etchant alone) versus the cyclic process. For a 25 nm unexposed photoresist film, etch stop occurs with slightly less than 15 nm of remaining thickness when etchant alone is utilized. By contrast, utilization of a cyclic process (240 seconds total time) results in far greater removal of the unexposed photoresist film with either Cl₂ or air oxidizing agent.

[0160] FIG. 6 presents a flow diagram of an exemplary alternative method for depositing and developing a photoresist according to some embodiments. The operations of a process 200 may be performed in different orders and/or with different, fewer, or additional operations. One or more operations of the process 200 may be performed using an apparatus described in any one of FIGS. 7-10. In some embodiments, the operations of the process 200 may be implemented, at least in part, according to software stored in one or more non-transitory computer readable media.

[0161] In operation 202 of the process 200, a photopatterned metal containing resist is provided.

[0162] In operation 204, the photopatterned metal-containing resist is exposed to an etchant.

[0163] In operation 206, after treatment with etchant, a wash agent is utilized to dissolve any non-volatile byproducts. In some embodiments, the wash agent may be a suitable polar solvent such as water, methanol, ethanol, isopropanol, acetone, acetonitrile, tetrahydrofuran, dimethyl sulfide or a combination thereof. In some embodiments, the wash agent may be supercritical fluid, such as a low surface tension supercritical liquid. Suitable liquids include, but are not limited to, carbon dioxide, sulfur dioxide, dimethyl ether or a combination thereof.

[0164] During the cleaning process with a wash agent, the temperature of the pedestal in the process chamber is from about 10°C to about 50 °C in some embodiments. In some embodiments, the process chamber pressure is from about 5 psi to about 3,000 psi during exposure to the wash agent.

[0165] In operation 208, a resist mask is formed. Plasma may be utilized to help harden the exposed photoresist, improve surface roughness and de-scum.

[0166] Process conditions for a descumming and smoothing operations may be controlled during or after development. In some embodiments, reactant flow may be between about 50 sccm and about 1000 sccm or between about 100 sccm and about 500 sccm, such as about 500 sccm He. In some embodiments, a temperature may be between about -60°C and about 120°C,

between about -20°C and about 60°C, or between about 20°C and about 40°C, such as about 20°C. In some embodiments, chamber pressure may be between about 1 mTorr and about 300 mTorr, between about 5 mTorr and about 100 mTorr, between about 5 mTorr and about 20 mTorr, such as about 10 mTorr. The plasma power may be relatively low with high ion energy. In some embodiments, plasma power may be between about 50 W and about 1000 W, between about 100 W and about 500 W, or between about 100 W and about 300 W, such as about 300 W. In some embodiments, the wafer bias is between about 10 V and about 500 V, between about 50 V and about 300 V, such as about 200 V. The plasma may be generated using a high RF frequency. In some embodiments, the RF frequency is 13.56 MHz. The duration of exposure to inert gas plasma may be relatively short so as to avoid excess exposure to UV radiation during plasma exposure. In some embodiments, the duration of exposure is between about 0.5 seconds and about 5 seconds, between about 1 second and about 3 seconds, such as about 2 seconds.

[0167] The inert gas plasma treatment for descumming and cleaning of the unexposed resist residue can have the collateral benefit of curing the exposed resist to harden it, thereby enhancing its hard mask function in subsequent operations to etch the underlying substrate. This resist hardening is achieved by exposure of the EUV exposed resist to UV radiation generated by the inert gas plasma, which may be continued after the descum/smoothing is complete with the bias turned off. The inert gas plasma curing may alternatively be performed if no descum/smoothing is needed or performed.

[0168] In some embodiments, inert gas plasma desorption descum and smoothing may be used with a wet development process. Wet development has very high selectivity and has been shown to exhibit clear on/off behavior, resulting in inability of a wet development process to remove areas exposed by “stray” EUV photons. The remaining residues are then left after the wet development process, resulting in scumming and high line edge and width roughness. Interestingly, due to the tunability of the dry development process in which the etch rate and selectivity can be tuned based on multiple knobs (e.g., time, temperature, pressure, gas/flow), inert gas plasma and/or dry development can be further applied to descum and smooth-metal containing resist lines by removing these partially exposed residues.

[0169] De-scumming and smoothing operations may be performed after wet development or dry development.

Apparatus

[0170] An apparatus of the present disclosure is configured for development of EUV resist. The apparatus may be configured to perform other processing operations such as deposition,

bevel and backside cleaning, post-application baking, EUV scanning, post-exposure baking, photoresist reworking, descum, smoothing, curing, and other operations. In some embodiments, the apparatus is configured to perform all dry operations. In some embodiments, the apparatus is configured to perform all wet operations. In some embodiments, the apparatus is configured to perform a combination of wet and dry operations. The apparatus may include a single wafer chamber or multiple stations in the same process chamber. With multiple stations in the same process chamber, various processing operations such as those described in the present disclosure may be performed in different stations in the same process chamber. For instance, PEB thermal treatment may be performed in one station and development in another station.

[0171] The apparatus configured for development of EUV resist includes a process chamber with a substrate support. The apparatus may include a vacuum line coupled to the process chamber for pressure control and a development chemistry line coupled to the process chamber for delivery of development chemistry. In some embodiments, the development chemistry includes halide-containing gases or radicals of halide-containing gases. In some embodiments, the process chamber is a plasma-generating chamber or coupled to a plasma-generating chamber that functions as a remote plasma source. The plasma-generating chamber may be an ICP, TCP, or CCP reactor. The apparatus may include one or more heaters for temperature control. Such heaters may be provided in the process chamber and/or in the substrate support.

[0172] In some embodiments, the process chamber interior is coated with corrosion-resistant films, such as polymers or inorganic coatings. In one example, the process chamber interior is coated with anodized alumina. In another example, the process chamber interior is coated with yttrium oxide (Y_2O_3).

[0173] In some embodiments, the process chamber is made of an inexpensive material such as plastic. The process chamber does not have to necessarily be made of metal or ceramic. The plastic material may be sufficient to withstand halide-containing chemistries during development. Vacuum lines and/or development chemistry lines may be coupled to a plastic chamber.

[0174] In some embodiments, the substrate support may be used to process a substrate using a temperature distribution having radial and azimuthal components. The substrate support may include a plurality of independently controllable temperature control zones arranged in proximity to substrate locations above the temperature control zones. This allows the one or more heaters in a substrate support to more precisely and locally control temperature. The temperature control zones may be arranged in a defined pattern such as a rectangular grid,

hexagonal grid, or other suitable pattern for generating a temperature profile as desired. In some embodiments, the temperature control zones may be spatially arranged in an electrostatic chuck to correct azimuthal non-uniformity or localized CD non-uniformity.

[0175] In some embodiments, the apparatus may further include a showerhead for delivery of one or more gases into the process chamber. In some embodiments, the showerhead may supply multiple separate gases to a reaction area while keeping the gases largely segregated within the showerhead. The showerhead may include multiple plenum volumes. This permits segregation of precursor gases, carrier gases, development gases, and cleaning gases, among other chemistries.

[0176] Removal of water or moisture from the process chamber may speed up the reaction of a photopatterned metal-containing EUV resist with development chemistry. In some embodiments, a cold trap may be coupled to the process chamber for removal of byproduct water vapor. The cold trap may condense the byproduct water vapor into liquid or solid form.

[0177] In some embodiments, the apparatus may further include a UV source such as a UV lamp and/or an IR source such as an IR lamp for resist curing and dehalogenation. The UV source and/or IR source may provide exposure to radiation to cure the EUV resist. Additionally or alternatively, the UV source may assist in photoactivation of development chemistries. Additionally or alternatively, the UV source may assist in halogen removal. Halogen residues may form on the semiconductor substrate or chamber surfaces that can be removed by UV exposure.

[0178] **FIG. 7** depicts a schematic illustration of an embodiment of process station 700 having a process chamber body 702 for maintaining a low-pressure environment that is suitable for embodiment of described dry development, clean, rework, descum and smoothing embodiments. A plurality of process stations 700 may be included in a common low-pressure process tool environment. In some embodiments, one or more hardware parameters of the process station 700 including those discussed in detail below may be adjusted programmatically by one or more computer controllers 750.

[0179] A process station may be configured as a module in a cluster tool. **FIG. 10** depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition and patterning modules suitable for implementation of the embodiments described herein. Such a cluster process tool architecture can include resist deposition, resist exposure (EUV scanner), resist development and etch modules, as described above and further below with reference to **FIGS. 9 and 10**.

[0180] In some embodiments, certain of the processing functions can be performed consecutively in the same module, for example dry development and etch. And embodiments of this disclosure are directed to methods and apparatus for receiving a wafer, including a photopatterned EUV resist thin film layer disposed on a layer or layer stack to be etched, to a dry development/etch chamber following photopatterning in an EUV scanner; dry developing photopatterned EUV resist thin film layer; and then etching the underlying layer using the patterned EUV resist as a mask, as described herein.

[0181] Returning to **FIG. 7**, process station 700 fluidly communicates with reactant delivery system 701 for delivering process gases to a distribution showerhead 706. Reactant delivery system 701 optionally includes a mixing vessel 704 for blending and/or conditioning process gases, for delivery to showerhead 706. One or more mixing vessel inlet valves 720 may control introduction of process gases to mixing vessel 704. Where plasma exposure is used, plasma may also be delivered to the showerhead 706 or may be generated in the process station 700. As noted above, in at least some embodiments, non-plasma thermal exposure is favored.

[0182] **FIG. 7** includes an optional vaporization point 703 for vaporizing liquid reactant to be supplied to the mixing vessel 704. In some embodiments, a liquid flow controller (LFC) upstream of vaporization point 703 may be provided for controlling a mass flow of liquid for vaporization and delivery to process station 700. For example, the LFC may include a thermal mass flow meter (MFM) located downstream of the LFC. A plunger valve of the LFC may then be adjusted responsive to feedback control signals provided by a proportional-integral-derivative (PID) controller in electrical communication with the MFM.

[0183] Showerhead 706 distributes process gases toward substrate 712. In the embodiment shown in **FIG. 7**, the substrate 712 is located beneath showerhead 706 and is shown resting on a pedestal 708. Showerhead 706 may have any suitable shape and may have any suitable number and arrangement of ports for distributing process gases to substrate 712.

[0184] In some embodiments, pedestal 708 may be raised or lowered to expose substrate 712 to a volume between the substrate 712 and the showerhead 706. It will be appreciated that, in some embodiments, pedestal height may be adjusted programmatically by a suitable computer controller 750. In some embodiments, the showerhead 706 may have multiple plenum volumes with multiple temperature controls.

[0185] In some embodiments, pedestal 708 may be temperature controlled via heater 710. In some embodiments, the pedestal 708 may be heated to a temperature of greater than 0°C and up to 300°C or more, for example 50 to 120°C, such as about 65 to 80°C, during non-plasma thermal exposure of a photopatterned resist to hydrogen halide dry development chemistry,

such as HBr or HCl, as described in disclosed embodiments. In some embodiments, the heater 710 of the pedestal 708 may include a plurality of independently controllable temperature control zones.

[0186] Further, in some embodiments, pressure control for process station 700 may be provided by a butterfly valve 718. As shown in the embodiment of **FIG. 7**, butterfly valve 718 throttles a vacuum provided by a downstream vacuum pump (not shown). However, in some embodiments, pressure control of process station 700 may also be adjusted by varying a flow rate of one or more gases introduced to the process station 1200.

[0187] In some embodiments, a position of showerhead 706 may be adjusted relative to pedestal 708 to vary a volume between the substrate 712 and the showerhead 706. Further, it will be appreciated that a vertical position of pedestal 708 and/or showerhead 706 may be varied by any suitable mechanism within the scope of the present disclosure. In some embodiments, pedestal 708 may include a rotational axis for rotating an orientation of substrate 712. It will be appreciated that, in some embodiments, one or more of these example adjustments may be performed programmatically by one or more suitable computer controllers 750.

[0188] Where plasma may be used, for example in gentle plasma-based dry development embodiments and/or etch operations conducted in the same chamber, showerhead 706 and pedestal 708 electrically communicate with a radio frequency (RF) power supply 714 and matching network 716 for powering a plasma. In some embodiments, the plasma energy may be controlled by controlling one or more of a process station pressure, a gas concentration, an RF source power, an RF source frequency, and a plasma power pulse timing. For example, RF power supply 714 and matching network 716 may be operated at any suitable power to form a plasma having a desired composition of radical species. Examples of suitable powers are up to about 500W.

[0189] In some embodiments, instructions for a controller 750 may be provided via input/output control (IOC) sequencing instructions. In one example, the instructions for setting conditions for a process phase may be included in a corresponding recipe phase of a process recipe. In some cases, process recipe phases may be sequentially arranged, so that all instructions for a process phase are executed concurrently with that process phase. In some embodiments, instructions for setting one or more reactor parameters may be included in a recipe phase. For example, a recipe phase may include instructions for setting a flow rate of a dry development chemistry reactant gas, such as HBr or HCl, and time delay instructions for

the recipe phase. In some embodiments, the controller 750 may include any of the features described below with respect to system controller 850 of **FIG. 8**.

[0190] As described above, one or more process stations may be included in a multi-station processing tool. **FIG. 8** shows a schematic view of an embodiment of a multi-station processing tool 800 with an inbound load lock 802 and an outbound load lock 804, either or both of which may include a remote plasma source. A robot 806 at atmospheric pressure is configured to move wafers from a cassette loaded through a pod 808 into inbound load lock 802 via an atmospheric port 810. A wafer is placed by the robot 806 on a pedestal 812 in the inbound load lock 802, the atmospheric port 810 is closed, and the load lock is pumped down. Where the inbound load lock 802 includes a remote plasma source, the wafer may be exposed to a remote plasma treatment to treat the silicon nitride surface in the load lock prior to being introduced into a processing chamber 814. Further, the wafer also may be heated in the inbound load lock 802 as well, for example, to remove moisture and adsorbed gases. Next, a chamber transport port 816 to processing chamber 814 is opened, and another robot (not shown) places the wafer into the reactor on a pedestal of a first station shown in the reactor for processing. While the embodiment depicted in **FIG. 8** includes load locks, it will be appreciated that, in some embodiments, direct entry of a wafer into a process station may be provided.

[0191] The depicted processing chamber 814 includes four process stations, numbered from 1 to 4 in the embodiment shown in **FIG. 8**. Each station has a heated pedestal (shown at 818 for station 1), and gas line inlets. It will be appreciated that in some embodiments, each process station may have different or multiple purposes. For example, in some embodiments, a process station may be switchable between dry development and etch process modes. Additionally, or alternatively, in some embodiments, processing chamber 814 may include one or more matched pairs of dry development and etch process stations. While the depicted processing chamber 814 includes four stations, it will be understood that a processing chamber according to the present disclosure may have any suitable number of stations. For example, in some embodiments, a processing chamber may have five or more stations, while in other embodiments a processing chamber may have three or fewer stations.

[0192] **FIG. 8** depicts an embodiment of a wafer handling system 890 for transferring wafers within processing chamber 814. In some embodiments, wafer handling system 890 may transfer wafers between various process stations and/or between a process station and a load lock. It will be appreciated that any suitable wafer handling system may be employed. Non-limiting examples include wafer carousels and wafer handling robots. **FIG. 8** also depicts

an embodiment of a system controller 850 employed to control process conditions and hardware states of process tool 800. System controller 850 may include one or more memory devices 856, one or more mass storage devices 854, and one or more processors 852. Processor 852 may include a CPU or computer, analog, and/or digital input/output connections, stepper motor controller boards, etc.

[0193] In some embodiments, system controller 850 controls all of the activities of process tool 800. System controller 850 executes system control software 858 stored in mass storage device 854, loaded into memory device 856, and executed on processor 852. Alternatively, the control logic may be hard coded in the controller 850. Applications Specific Integrated Circuits, Programmable Logic Devices (e.g., field-programmable gate arrays, or FPGAs) and the like may be used for these purposes. In the following discussion, wherever “software” or “code” is used, functionally comparable hard coded logic may be used in its place. System control software 858 may include instructions for controlling the timing, mixture of gases, gas flow rates, chamber and/or station pressure, chamber and/or station temperature, wafer temperature, target power levels, RF power levels, substrate pedestal, chuck and/or susceptor position, and other parameters of a particular process performed by process tool 800. System control software 858 may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operation of the process tool components used to carry out various process tool processes. System control software 858 may be coded in any suitable computer readable programming language.

[0194] In some embodiments, system control software 858 may include input/output control (IOC) sequencing instructions for controlling the various parameters described above. Other computer software and/or programs stored on mass storage device 854 and/or memory device 856 associated with system controller 850 may be employed in some embodiments. Examples of programs or sections of programs for this purpose include a substrate positioning program, a process gas control program, a pressure control program, a heater control program, and a plasma control program.

[0195] A substrate positioning program may include program code for process tool components that are used to load the substrate onto pedestal 818 and to control the spacing between the substrate and other parts of process tool 800.

[0196] A process gas control program may include code for controlling halide-containing gas composition (e.g., HBr or HCl gas as described herein) and flow rates and optionally for flowing gas into one or more process stations prior to deposition in order to stabilize the pressure in the process station. A pressure control program may include code for controlling

the pressure in the process station by regulating, for example, a throttle valve in the exhaust system of the process station, a gas flow into the process station, etc.

[0197] A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas (such as helium) to the substrate.

[0198] A plasma control program may include code for setting RF power levels applied to the process electrodes in one or more process stations in accordance with the embodiments herein.

[0199] A pressure control program may include code for maintaining the pressure in the reaction chamber in accordance with the embodiments herein.

[0200] In some embodiments, there may be a user interface associated with system controller 850. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0201] In some embodiments, parameters adjusted by system controller 850 may relate to process conditions. Non-limiting examples include process gas composition and flow rates, temperature, pressure, plasma conditions (such as RF bias power levels), etc. These parameters may be provided to the user in the form of a recipe, which may be entered utilizing the user interface.

[0202] Signals for monitoring the process may be provided by analog and/or digital input connections of system controller 850 from various process tool sensors. The signals for controlling the process may be output on the analog and digital output connections of process tool 800. Non-limiting examples of process tool sensors that may be monitored include mass flow controllers, pressure sensors (such as manometers), thermocouples, etc. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain process conditions.

[0203] System controller 850 may provide program instructions for implementing the above-described deposition processes. The program instructions may control a variety of process parameters, such as DC power level, RF bias power level, pressure, temperature, etc. The instructions may control the parameters to operate development and/or etch processes according to various embodiments described herein.

[0204] The system controller 850 will typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a method in accordance with disclosed embodiments. Machine-readable media containing

instructions for controlling process operations in accordance with disclosed embodiments may be coupled to the system controller 850.

[0205] In some embodiments, the system controller 850 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The system controller 850, depending on the processing conditions and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0206] Broadly speaking, the system controller 850 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the system controller 850 in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0207] The system controller 850, in some embodiments, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the system controller 850 may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress

of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the system controller 850 receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the system controller 850 is configured to interface with or control. Thus, as described above, the system controller 850 may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0208] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, an EUV lithography chamber (scanner) or module, a development chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0209] As noted above, depending on the process step or steps to be performed by the tool, the system controller 850 might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0210] Inductively coupled plasma (ICP) reactors which, in certain embodiments, may be suitable for etch operations suitable for implementation of some embodiments, are now

described. Although ICP reactors are described herein, in some embodiments, it should be understood that capacitively coupled plasma reactors may also be used.

[0211] **FIG. 9** schematically shows a cross-sectional view of an inductively coupled plasma apparatus 900 appropriate for implementing certain embodiments or aspects of embodiments such as dry development and/or etch. In other embodiments, other tools or tool types having the functionality to conduct the dry development and/or etch processes described herein may be used for implementation.

[0212] The inductively coupled plasma apparatus 900 includes an overall process chamber 924 structurally defined by chamber walls 901 and a window 911. The chamber walls 901 may be fabricated from stainless steel, aluminum, or plastic. The window 911 may be fabricated from quartz or other dielectric material. An optional internal plasma grid 950 divides the overall process chamber into an upper sub-chamber 902 and a lower sub-chamber 903. In most embodiments, plasma grid 950 may be removed, thereby utilizing a chamber space made of sub-chambers 902 and 903. A chuck 917 is positioned within the lower sub-chamber 903 near the bottom inner surface. The chuck 917 is configured to receive and hold a semiconductor wafer 919 upon which the etching and deposition processes are performed. The chuck 917 can be an electrostatic chuck for supporting the wafer 919 when present. In some embodiments, an edge ring (not shown) surrounds chuck 917 and has an upper surface that is approximately planar with a top surface of the wafer 919, when present over chuck 917. The chuck 917 also includes electrostatic electrodes for chucking and dechucking the wafer 919. A filter and DC clamp power supply (not shown) may be provided for this purpose. Other control systems for lifting the wafer 919 off the chuck 917 can also be provided. The chuck 917 can be electrically charged using an RF power supply 923. The RF power supply 923 is connected to matching circuitry 921 through a connection 927. The matching circuitry 921 is connected to the chuck 917 through a connection 925. In this manner, the RF power supply 923 is connected to the chuck 917. In various embodiments, a bias power of the electrostatic chuck may be set at about 50V or may be set at a different bias power depending on the process performed in accordance with disclosed embodiments. For example, the bias power may be between about 20 Vb and about 100 V, or between about 30 V and about 150 V.

[0213] Elements for plasma generation include a coil 933 is positioned above window 911. In some embodiments, a coil is not used in disclosed embodiments. The coil 933 is fabricated from an electrically conductive material and includes at least one complete turn. The example of a coil 933 shown in **FIG. 9** includes three turns. The cross sections of coil 933 are shown with symbols, and coils having an “X” extend rotationally into the page, while coils having a

“●” extend rotationally out of the page. Elements for plasma generation also include an RF power supply 941 configured to supply RF power to the coil 933. In general, the RF power supply 941 is connected to matching circuitry 939 through a connection 945. The matching circuitry 939 is connected to the coil 933 through a connection 943. In this manner, the RF power supply 941 is connected to the coil 933. An optional Faraday shield 949 is positioned between the coil 933 and the window 911. The Faraday shield 949 may be maintained in a spaced apart relationship relative to the coil 933. In some embodiments, the Faraday shield 949 is disposed immediately above the window 911. In some embodiments, the Faraday shield 949 is between the window 911 and the chuck 917. In some embodiments, the Faraday shield 949 is not maintained in a spaced apart relationship relative to the coil 933. For example, the Faraday shield 949 may be directly below the window 911 without a gap. The coil 933, the Faraday shield 949, and the window 911 are each configured to be substantially parallel to one another. The Faraday shield 949 may prevent metal or other species from depositing on the window 911 of the process chamber 924.

[0214] Process gases may be flowed into the process chamber through one or more main gas flow inlets 960 positioned in the upper sub-chamber 902 and/or through one or more side gas flow inlets 970. Likewise, though not explicitly shown, similar gas flow inlets may be used to supply process gases to a capacitively coupled plasma processing chamber. A vacuum pump, e.g., a one or two stage mechanical dry pump and/or turbomolecular pump 940, may be used to draw process gases out of the process chamber 924 and to maintain a pressure within the process chamber 924. For example, the vacuum pump may be used to evacuate the lower sub-chamber 903 during a purge operation of ALD. A valve-controlled conduit may be used to fluidically connect the vacuum pump to the process chamber 924 so as to selectively control application of the vacuum environment provided by the vacuum pump. This may be done employing a closed loop-controlled flow restriction device, such as a throttle valve (not shown) or a pendulum valve (not shown), during operational plasma processing. Likewise, a vacuum pump and valve controlled fluidic connection to the capacitively coupled plasma processing chamber may also be employed.

[0215] During operation of the apparatus 900, one or more process gases may be supplied through the gas flow inlets 960 and/or 970. In certain embodiments, process gas may be supplied only through the main gas flow inlet 960, or only through the side gas flow inlet 970. In some cases, the gas flow inlets shown in the figure may be replaced by more complex gas flow inlets, one or more showerheads, for example. The Faraday shield 949 and/or optional grid 950 may include internal channels and holes that allow delivery of process gases to the

process chamber 924. Either or both of Faraday shield 949 and optional grid 950 may serve as a showerhead for delivery of process gases. In some embodiments, a liquid vaporization and delivery system may be situated upstream of the process chamber 924, such that once a liquid reactant or precursor is vaporized, the vaporized reactant or precursor is introduced into the process chamber 924 via a gas flow inlet 960 and/or 970.

[0216] Radio frequency power is supplied from the RF power supply 941 to the coil 933 to cause an RF current to flow through the coil 933. The RF current flowing through the coil 933 generates an electromagnetic field about the coil 933. The electromagnetic field generates an inductive current within the upper sub-chamber 902. The physical and chemical interactions of various generated ions and radicals with the wafer 919 etch features of and selectively deposit layers on the wafer 919.

[0217] If the plasma grid 950 is used such that there is both an upper sub-chamber 902 and a lower sub-chamber 903, the inductive current acts on the gas present in the upper sub-chamber 902 to generate an electron-ion plasma in the upper sub-chamber 902. The optional internal plasma grid 1450 limits the amount of hot electrons in the lower sub-chamber 903. In some embodiments, the apparatus 900 is designed and operated such that the plasma present in the lower sub-chamber 903 is an ion-ion plasma.

[0218] Both the upper electron-ion plasma and the lower ion-ion plasma may contain positive and negative ions, though the ion-ion plasma will have a greater ratio of negative ions to positive ions. Volatile etching and/or deposition byproducts may be removed from the lower sub-chamber 903 through port 922. The chuck 917 disclosed herein may operate at elevated temperatures ranging between about 10°C and about 250°C. The temperature will depend on the process operation and specific recipe.

[0219] Apparatus 900 may be coupled to facilities (not shown) when installed in a clean room or a fabrication facility. Facilities include plumbing that provide processing gases, vacuum, temperature control, and environmental particle control. These facilities are coupled to apparatus 900, when installed in the target fabrication facility. Additionally, apparatus 900 may be coupled to a transfer chamber that allows robotics to transfer semiconductor wafers into and out of apparatus 900 using typical automation.

[0220] In some embodiments, a system controller 930 (which may include one or more physical or logical controllers) controls some or all of the operations of a process chamber 924. The system controller 930 may include one or more memory devices and one or more processors. In some embodiments, the apparatus 900 includes a switching system for controlling flow rates and durations when disclosed embodiments are performed. In some

embodiments, the apparatus 900 may have a switching time of up to about 500 ms, or up to about 750 ms. Switching time may depend on the flow chemistry, recipe chosen, reactor architecture, and other factors.

[0221] In some embodiments, the system controller 930 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be integrated into the system controller 930, which may control various components or subparts of the system or systems. The system controller, depending on the processing parameters and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0222] Broadly speaking, the system controller 930 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication or removal of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0223] The system controller 930, in some embodiments, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The

computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the system controller 930 receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the system controller 930 may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0224] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an ALD chamber or module, an ALE chamber or module, an ion implantation chamber or module, a track chamber or module, an EUV lithography chamber (scanner) or module, a dry development chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0225] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0226] EUVL patterning may be conducted using any suitable tool, often referred to as a scanner. The EUVL patterning tool may be a standalone device from which the substrate is

moved into and out of for deposition and etching as described herein. Or, as described below, the EUVL patterning tool may be a module on a larger multi-component tool. **FIG. 10** depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition, EUV patterning and dry development/etch modules that interface with a vacuum transfer module, suitable for implementation of the processes described herein. While the processes may be conducted without such vacuum integrated apparatus, such apparatus may be advantageous in some embodiments.

[0227] **FIG. 10** depicts a semiconductor process cluster tool architecture 1000 with vacuum-integrated deposition and patterning modules that interface with a vacuum transfer module, suitable for implementation of processes described herein. The arrangement of transfer modules to “transfer” wafers among multiple storage facilities and processing modules may be referred to as a “cluster tool architecture” system. Deposition and patterning modules are vacuum-integrated, in accordance with the requirements of a particular process. Other modules, such as for etch, may also be included on the cluster.

[0228] A vacuum transport module (VTM) 1038 interfaces with four processing modules 1020a–1020d, which may be individually optimized to perform various fabrication processes. By way of example, processing modules 1020a–1020d may be implemented to perform deposition, evaporation, ELD, dry development, etch, strip, and/or other semiconductor processes. For example, module 1020a may be an ALD reactor that may be operated to perform in a non-plasma, thermal atomic layer depositions as described herein. It should be understood that the figure is not necessarily drawn to scale.

[0229] Airlocks 1042 and 1046, also known as a loadlocks or transfer modules, interface with the VTM 1038 and a patterning module 1040. This tool architecture allows for work pieces, such as semiconductor substrates or wafers, to be transferred under vacuum so as not to react before exposure. Integration of the deposition modules with the lithography tool is facilitated by the fact that EUVL also requires a greatly reduced pressure given the strong optical absorption of the incident photons by ambient gases such as H₂O, O₂, etc.

[0230] As noted above, this integrated architecture is just one possible embodiment of a tool for implementation of the described processes. The processes may also be implemented with a more conventional stand-alone EUVL scanner and a deposition reactor, either stand alone or integrated in a cluster architecture with other tools, such as etch, strip etc., as modules, for example as described with reference to **FIG. 10** but without the integrated patterning module.

[0231] Airlock 1042 may be an “outgoing” loadlock, referring to the transfer of a substrate out from the VTM 1038 serving a deposition module 1020a to the patterning module 1040, and

airlock 1046 may be an “ingoing” loadlock, referring to the transfer of a substrate from the patterning module 1040 back in to the VTM 1038. The ingoing loadlock 1046 may also provide an interface to the exterior of the tool for access and egress of substrates. Each process module has a facet that interfaces the module to VTM 1038. For example, deposition process module 1020a has facet 1036. Inside each facet, sensors, for example, sensors 1–18 as shown, are used to detect the passing of wafer 1026 when moved between respective stations. Patterning module 1040 and airlocks 1042 and 1046 may be similarly equipped with additional facets and sensors, not shown.

[0232] Main VTM robot 1022 transfers wafer 1026 between modules, including airlocks 1042 and 1046. In one embodiment, robot 1022 has one arm, and in another embodiment, robot 1022 has two arms, where each arm has an end effector 1024 to pick wafers such as wafer 1026 for transport. Front-end robot 1044, in is used to transfer wafers 1026 from outgoing airlock 1042 into the patterning module 1040, from the patterning module 1040 into ingoing airlock 1046. Front-end robot 1044 may also transport wafers 1026 between the ingoing loadlock and the exterior of the tool for access and egress of substrates. Because ingoing airlock module 1046 has the ability to match the environment between atmospheric and vacuum, the wafer 1026 is able to move between the two pressure environments without being damaged.

[0233] It should be noted that a EUVL tool typically operates at a higher vacuum than a deposition tool. If this is the case, it is desirable to increase the vacuum environment of the substrate during the transfer between the deposition to the EUVL tool to allow the substrate to degas prior to entry into the patterning tool. Outgoing airlock 1042 may provide this function by holding the transferred wafers at a lower pressure, no higher than the pressure in the patterning module 1040, for a period of time and exhausting any off-gassing, so that the optics of the patterning tool 1040 are not contaminated by off-gassing from the substrate. A suitable pressure for the outgoing, off-gassing airlock is no more than $1\text{E-}8$ Torr.

[0234] In some embodiments, a system controller 1050 (which may include one or more physical or logical controllers) controls some or all of the operations of the cluster tool and/or its separate modules. It should be noted that the controller can be local to the cluster architecture, or can be located external to the cluster architecture in the manufacturing floor, or in a remote location and connected to the cluster architecture via a network. The system controller 1050 may include one or more memory devices and one or more processors. The processor may include a central processing unit (CPU) or computer, analog and/or digital input/output connections, stepper motor controller boards, and other like components. Instructions for implementing appropriate control operations are executed on the processor.

These instructions may be stored on the memory devices associated with the controller or they may be provided over a network. In certain embodiments, the system controller executes system control software.

[0235] The system control software may include instructions for controlling the timing of application and/or magnitude of any aspect of tool or module operation. System control software may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operations of the process tool components necessary to carry out various process tool processes. System control software may be coded in any suitable compute readable programming language. In some embodiments, system control software includes input/output control (IOC) sequencing instructions for controlling the various parameters described above. For example, each phase of a semiconductor fabrication process may include one or more instructions for execution by the system controller. The instructions for setting process conditions for condensation, deposition, evaporation, patterning and/or etching phase may be included in a corresponding recipe phase, for example.

[0236] In various embodiments, an apparatus for forming a negative pattern mask is provided. The apparatus may include a processing chamber for patterning, deposition and etch, and a controller including instructions for forming a negative pattern mask. The instructions may include code for, in the processing chamber, patterning a feature in a chemically amplified (CAR) resist on a semiconductor substrate by EUV exposure to expose a surface of the substrate, developing the photopatterned resist, and etching the underlying layer or layer stack using the patterned resist as a mask. Development may be performed using a halide-containing chemistry.

[0237] It should be noted that the computer controlling the wafer movement can be local to the cluster architecture, or can be located external to the cluster architecture in the manufacturing floor, or in a remote location and connected to the cluster architecture via a network. A controller as described above with respect to any of **FIGS. 7, 8 or 9** may be implemented with the tool in **FIG. 10**.

Conclusion

[0238] It is understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art. Although various details have been omitted for clarity's sake, various design alternatives may be implemented. Therefore, the present examples are to be considered

as illustrative and not restrictive, and the disclosure is not to be limited to the details given herein, but may be modified within the scope of the disclosure.

CLAIMS

What is claimed is:

1. A method of processing a semiconductor substrate comprising:
providing a photopatterned metal-containing resist on a semiconductor substrate on a pedestal in a process chamber; and
developing the photopatterned metal-containing resist by selectively removing a portion of the photopatterned metal-containing resist by exposing the photopatterned metal-containing resist to at least one cycle comprising a pulse of an etchant and a pulse of an oxidizing agent, delivered alternately, to form a resist mask.
2. The method of claim 1, wherein the pulse of the etchant and the pulse of the oxidizing agent are temporally separate.
3. The method of claim 1, wherein the pedestal is at a first temperature during the pulse of the etchant; and the oxidizing agent is delivered to the process chamber at a second temperature.
4. The method of claim 1, wherein the pedestal is at a first temperature during the pulse of the etchant and the pedestal is at a second temperature during the pulse of the oxidizing agent.
5. The method of claim 1, wherein a duration of the pulse of the etchant is from about 1 to about 120 seconds and a duration of the pulse of the oxidizing agent is from about 1 to about 120 seconds.
6. The method of claim 3, wherein the first temperature is from about -60°C to about 120°C.
7. The method of claim 4, wherein the second temperature is from about 20°C to about 150 °C.
8. The method of claim 3, wherein the second temperature is from about 50°C to about 250 °C.

9. The method of claim 1, whereby non-volatile byproducts of the pulse of the etchant are removed from the photopatterned metal-containing resist.
10. The method of claim 1, wherein the photopatterned metal-containing resist comprises an organo-metal oxide, a metal, a metal oxide or an organo-metal.
11. The method of claim 10, wherein the metal oxide comprises a tin oxide.
12. The method of claim 1, wherein the etchant is a halide etchant.
13. The method of claim 12, wherein the halide etchant comprises a hydrogen halide, hydrogen gas and halogen gas, an organic halide, an acyl halide, a carbonyl halide, a thionyl halide or a combination thereof.
14. The method of claim 12, wherein the halide etchant comprises hydrogen fluoride, hydrogen chloride, boron trichloride, hydrogen bromide, hydrogen iodide or a combination thereof.
15. The method of claim 1, wherein the etchant comprises an etchant plasma.
16. The method of claim 15, wherein the etchant plasma is generated remotely.
17. The method of claim 1, wherein the oxidizing agent comprises oxygen, ozone, hydrogen peroxide, water, nitrous oxide, nitric oxide, nitrogen dioxide, nitric acid, sulfur dioxide, chlorine, fluorine, bromine, iodine or a combination thereof.
18. The method of claim 17, wherein the oxidizing agent is a gaseous oxidizing agent comprising water and oxygen or chlorine.
19. The method of claim 1, wherein the oxidizing agent comprises an oxidizing agent plasma.
20. The method of claim 19, wherein the oxidizing agent plasma is generated remotely.

21. The method of claim 1, further comprising exposing the photopatterned metal-containing resist to an inert plasma gas.

22. The method of claim 1, further comprising purging the process chamber with an inert gas between the pulse of the etchant and the pulse of the oxidizing agent or after a cycle of a pulse of the etchant and a pulse of the oxidizing agent.

23. The method of claim 1, wherein developing the photopatterned metal-containing resist by exposure to alternating pulses of an etchant and an oxidizing agent comprises dry developing the photopatterned metal-containing resist.

24. The method of claim 1, wherein developing the photopatterned metal-containing resist by exposure to alternating pulses of an etchant and an oxidizing agent comprises wet developing the photopatterned metal-containing resist.

25. The method of claim 1, wherein each cycle has the same etchant pulse duration.

26. A method of processing a semiconductor substrate comprising:
providing a photopatterned metal-containing resist on a semiconductor substrate on a pedestal in a process chamber; and
developing the photopatterned metal-containing resist by selectively removing a portion of the photopatterned metal-containing resist by exposing the photopatterned metal-containing resist to an etchant, followed by subsequent exposure to a wash agent, to form a resist mask.

27. The method of claim 26, wherein the wash agent comprises water, methanol, ethanol, isopropanol, acetone, acetonitrile, tetrahydrofuran, dimethyl sulfide or a combination thereof.

28. The method of claim 26, wherein a pedestal temperature is from about 10°C to about 50 °C during exposure to the wash agent.

29. The method of claim 26, wherein the wash agent comprises a supercritical fluid.

30. The method of claim 29, wherein the supercritical fluid is a low surface tension supercritical liquid.

31. The method of claim 30, wherein the low surface tension supercritical liquid comprises carbon dioxide, sulfur dioxide, dimethyl ether or a combination thereof.

32. The method of claim 29, wherein a process chamber pressure is from about 5 psi to about 3,000 psi during exposure to the wash agent.

33. The method of claim 26, whereby non-volatile byproducts from etchant exposure are removed from the photopatterned metal-containing resist.

34. The method of claim 26, wherein the photopatterned metal-containing resist comprises an organo-metal oxide, a metal, a metal oxide or an organo-metal.

35. The method of claim 34, wherein the metal oxide comprises a tin oxide.

36. The method of claim 26, wherein the etchant is a halide etchant.

37. The method of claim 36, wherein the halide etchant comprises a hydrogen halide, hydrogen gas and halogen gas, an organic halide, an acyl halide, a carbonyl halide, a thionyl halide or a combination thereof.

38. The method of claim 36, wherein the halide etchant comprises hydrogen fluoride, hydrogen chloride, boron trichloride, hydrogen bromide, hydrogen iodide or a combination thereof.

39. The method of claim 26, wherein the etchant comprises an etchant plasma.

40. The method of claim 39, wherein the etchant plasma is generated remotely.

41. A method of promoting atomic layer etching on a substrate comprising:
providing a photopatterned metal-containing resist on a semiconductor substrate on a pedestal in a process chamber; and

developing the photopatterned metal-containing resist by selectively removing a portion of the resist by exposing the photopatterned metal-containing resist to at least one cycle comprising a pulse of an etchant and a pulse of an oxidizing agent, delivered alternately, to form a resist mask;

whereby etch stop due to non-volatile byproducts of the etchant pulse is eliminated.

42. A method of processing a semiconductor substrate, the method comprising:
providing a dry-deposited photopatterned metal oxide EUV resist on a semiconductor substrate on a pedestal in a process chamber; and
dry developing the photopatterned metal oxide EUV resist by selectively removing an EUV-unexposed portion of the EUV resist by exposure to at least one cycle comprising a pulse of an etchant and a pulse of an oxidizing agent, delivered alternately, to form a resist hard mask.

43. An apparatus for conducting development of resist, the apparatus comprising:
a process chamber with a substrate support;
a vacuum line coupled to the process chamber;
etchant and oxidizing agents lines coupled to the process chamber; and
a controller configured with instructions for processing a semiconductor substrate, the instructions comprising code for:
providing a photopatterned metal-containing resist on a semiconductor substrate in a process chamber; and
developing the photopatterned metal-containing resist by selectively removing a portion of the resist by exposure to at least one cycle comprising an etchant pulse and an oxidizing agent pulse, delivered alternately, to form a resist mask.

44. The apparatus of claim 43, wherein the photopatterned metal-containing resist is a photopatterned metal-containing EUV resist, and wherein the controller configured with instructions comprising code for developing the photopatterned metal-containing EUV resist comprises code for selectively removing an EUV-unexposed portion of the EUV resist relative to an EUV-exposed portion with at least one cycle comprising an etchant pulse and an oxidizing agent pulse, delivered alternately, to form the resist mask.

45. The apparatus of claim 43, further comprising:
one or more heaters coupled to the substrate support, wherein the one or more heaters include a plurality of independently controllable temperature control zones.
46. The apparatus of claim 45, further comprising heated oxidizing agent delivery lines.