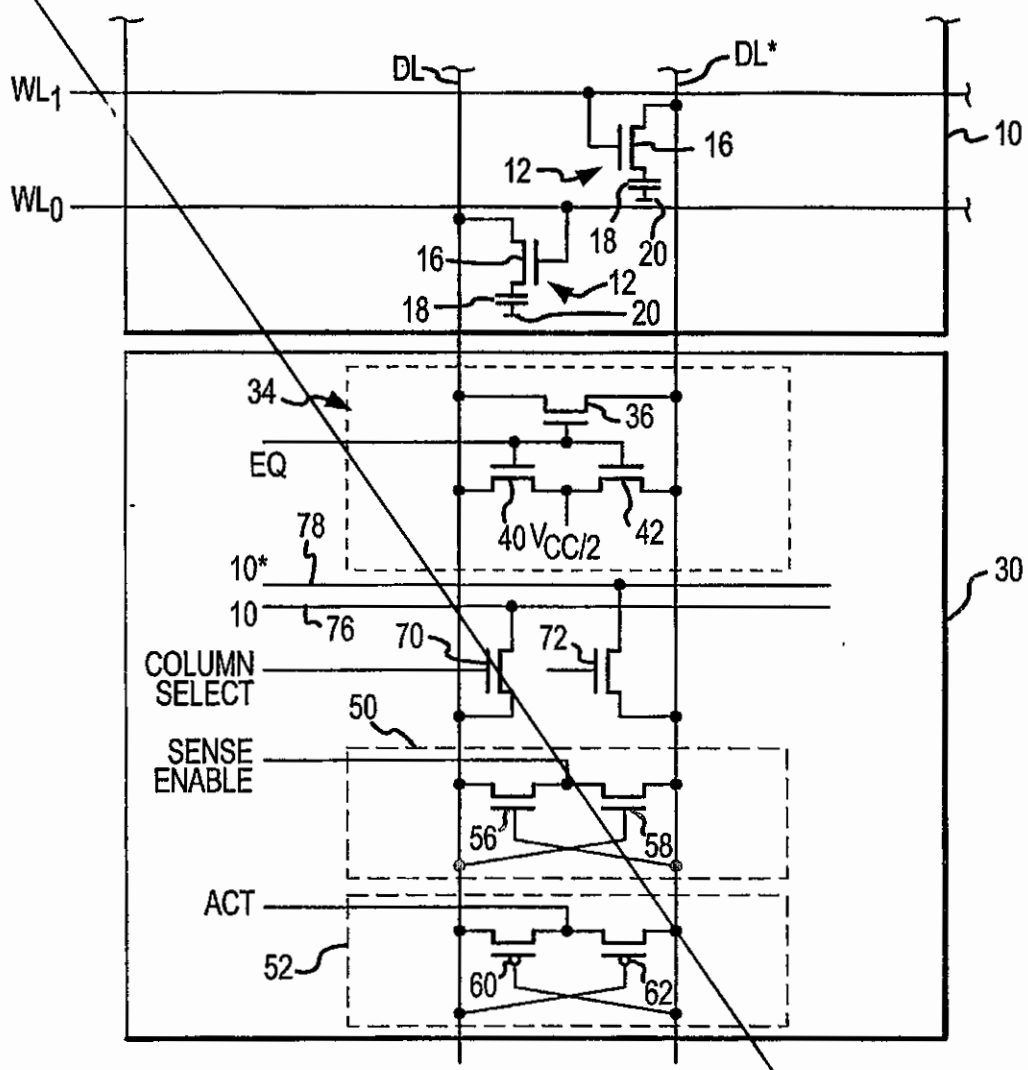


(PRIOR ART)

FIG.1

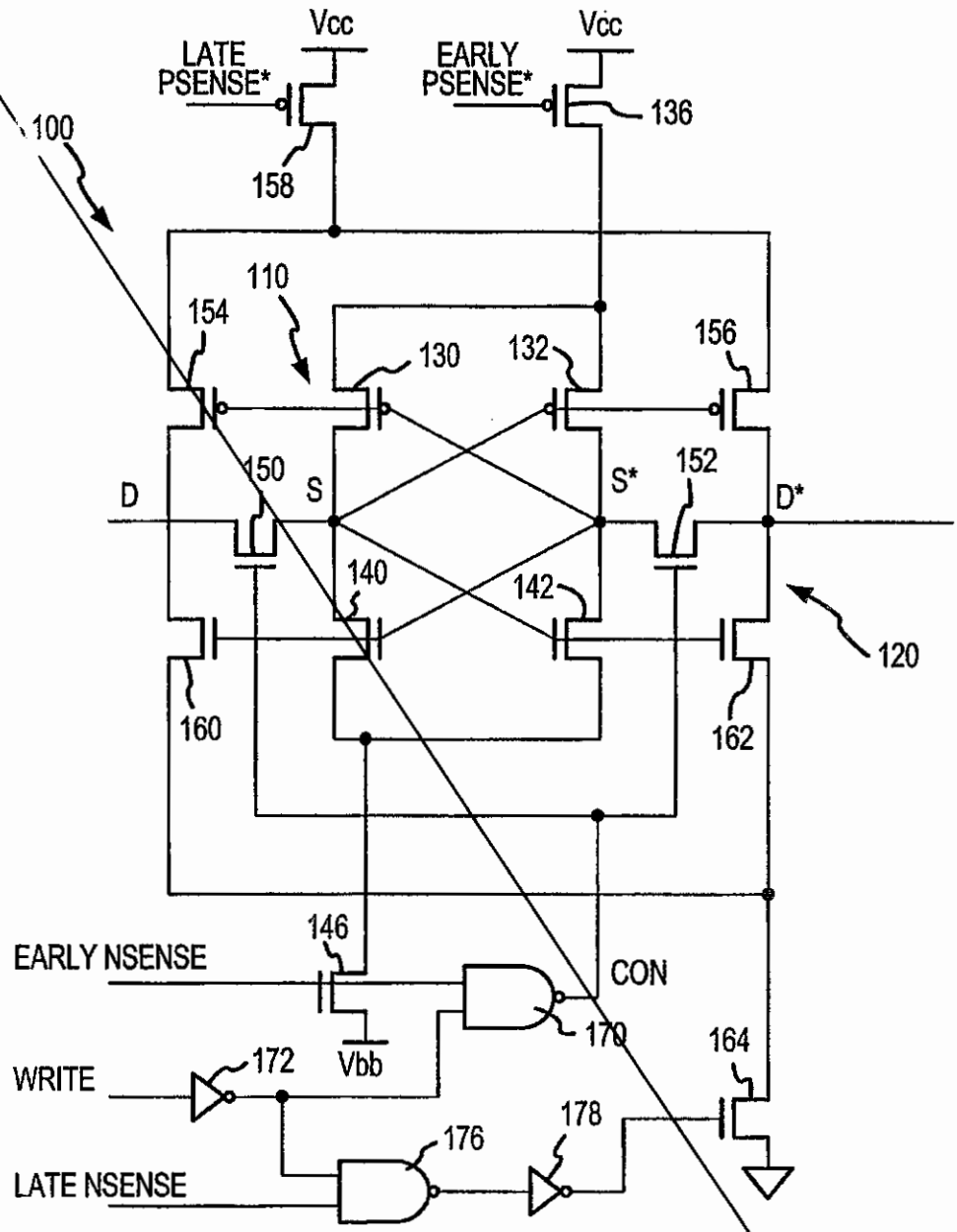

Vcc
Vcc
LATE PSENSE*
EARLY PSENSE*
136
158
100
110
154
130
132
156
150
D
S
S*
152
D*
140
142
120
160
162
146
EARLY NSENSE
CON
170
164
WRITE
172
Vbb
178
176
LATE NSENSE

FIG.2

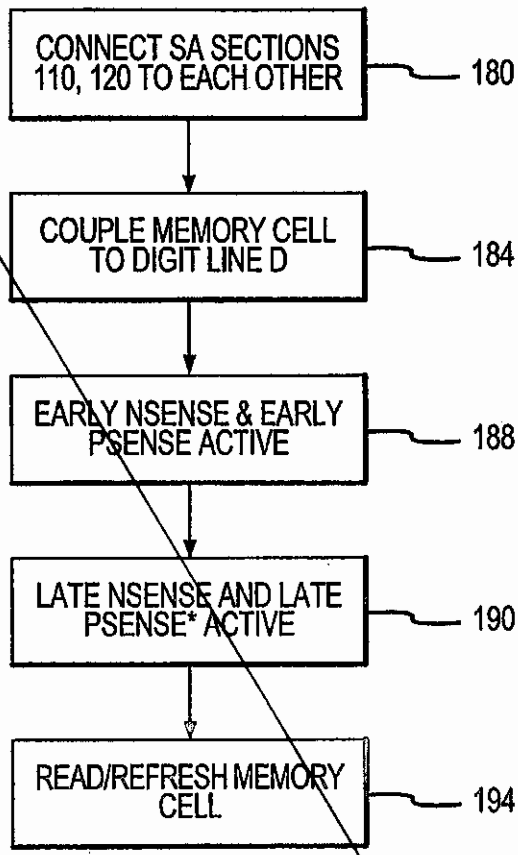

CONNECT SA SECTIONS 110, 120 TO EACH OTHER
180
COUPLE MEMORY CELL TO DIGIT LINE D
184
EARLY NSENSE & EARLY PSENSE ACTIVE
188
LATE NSENSE AND LATE PSENSE* ACTIVE
190
READ/REFRESH MEMORY CELL
194

FIG.3

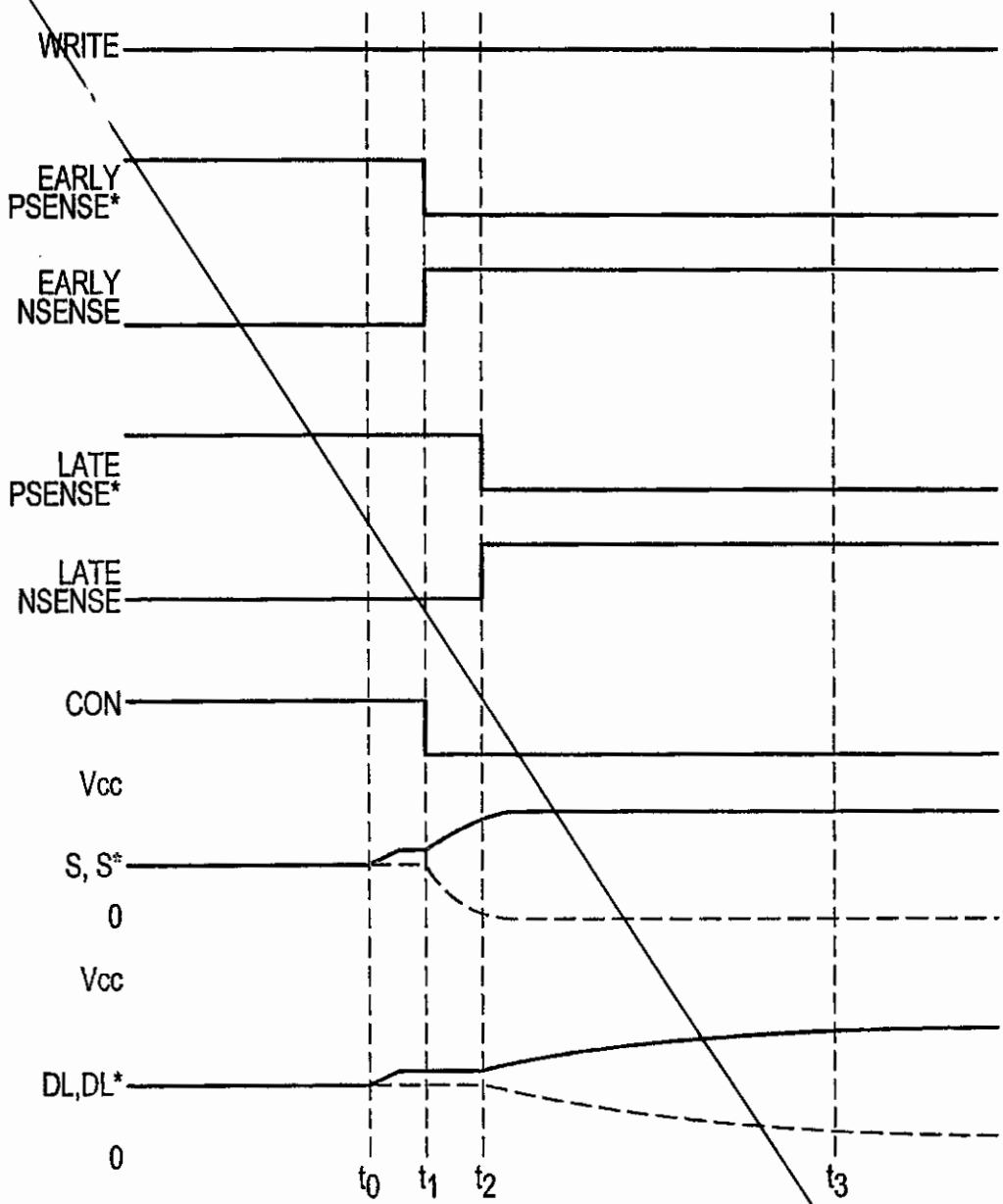

WRITE
EARLY PSENSE*
EARLY NSENSE
LATE PSENSE*
LATE NSENSE
CON
Vcc
S, S*
0
Vcc
DL,DL*
0
t0
t1
t2
t3

FIG.4

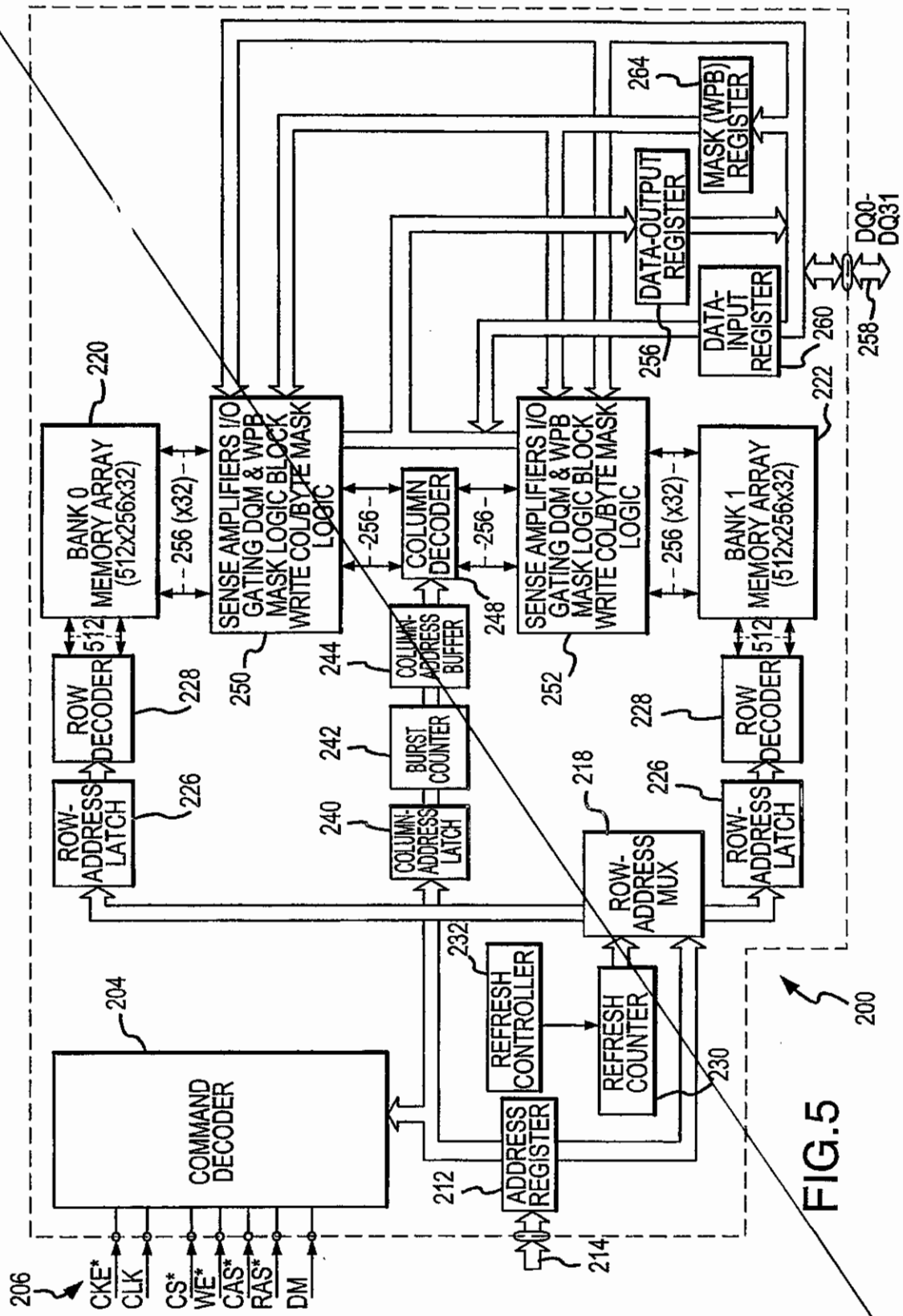

BANK 0 MEMORY ARRAY (512x256x32)
220
256 (x32)
SENSE AMPLIFIERS I/O GATING DQM & WPB MASK LOGIC BLOCK WRITE COL/BYTE MASK LOGIC
250
256
COLUMN DECODER
248
COLUMN-ADDRESS BUFFER
244
BURST COUNTER
242
COLUMN-ADDRESS LATCH
240
ROW-ADDRESS LATCH
226
ROW DECODER
228
512
264
MASK (WPB) REGISTER
DATA-OUTPUT REGISTER
DATA-INPUT REGISTER
256
260
258
DQ0-DQ31
222
BANK 1 MEMORY ARRAY (512x256x32)
252
ROW-ADDRESS MUX
218
REFRESH CONTROLLER
232
REFRESH COUNTER
230
COMMAND DECODER
204
ADDRESS REGISTER
212
214
206
CKE*
CLK
CS*
WE*
CAS*
RAS*
DM
200

FIG.5

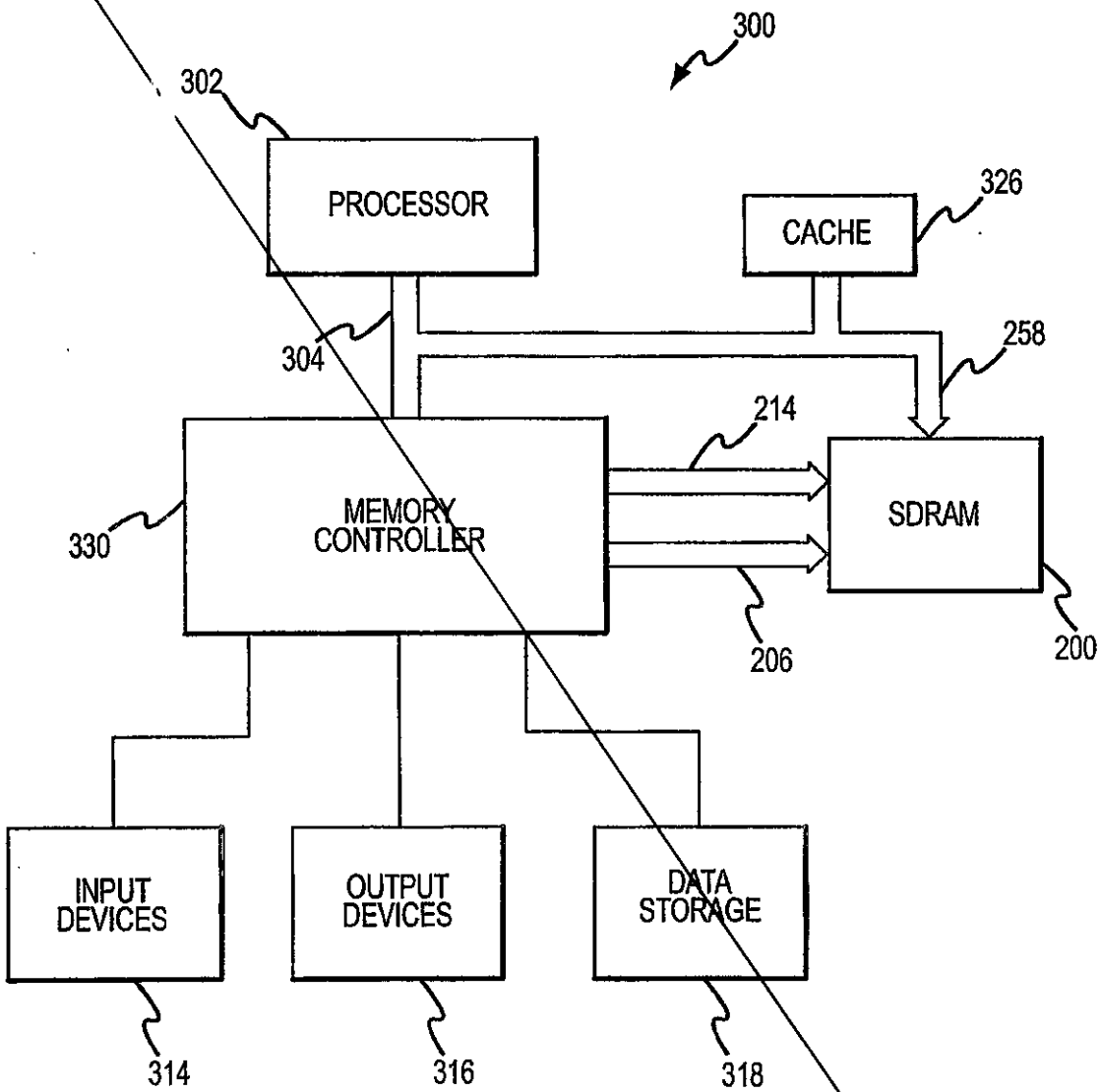
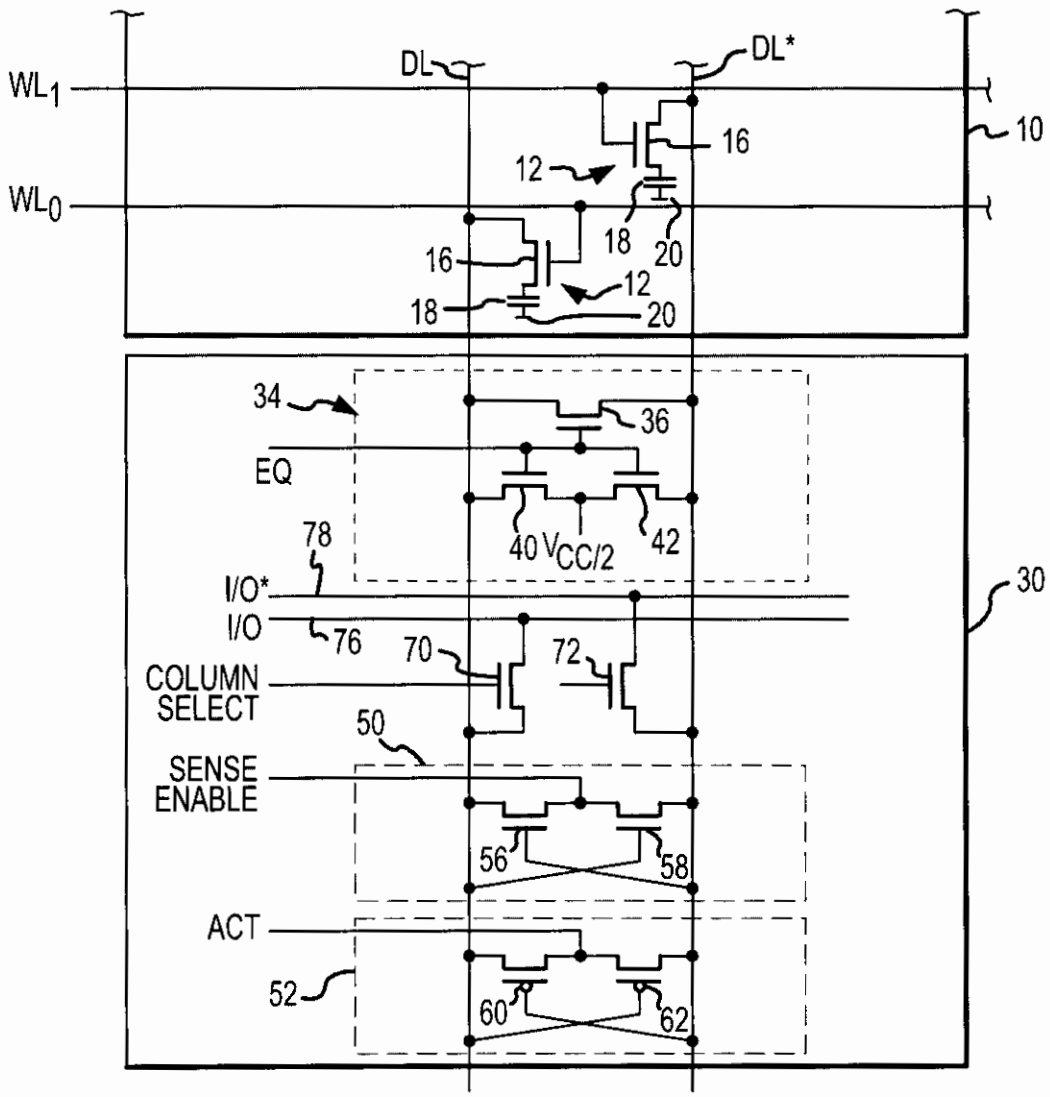

300
302
PROCESSOR
326
CACHE
304
258
214
330
MEMORY CONTROLLER
SDRAM
206
200
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE
314
316
318

FIG.6



(PRIOR ART)

FIG.1

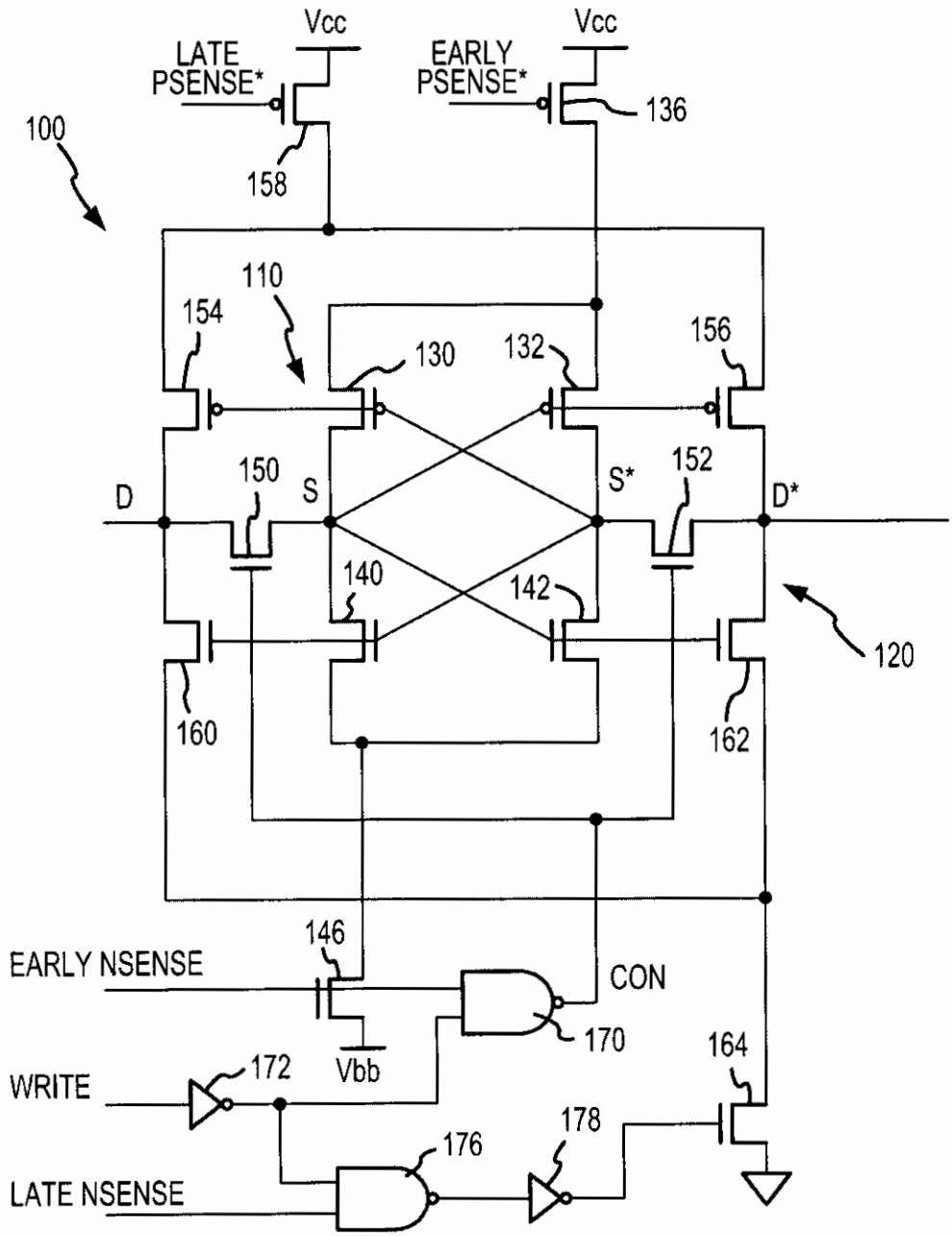

Vcc
Vcc
LATE PSENSE*
EARLY PSENSE*
136
100
158
110
154
130
132
156
D
150
S
S*
152
D*
140
142
120
160
162
EARLY NSENSE
146
CON
170
164
WRITE
172
Vbb
178
176
LATE NSENSE

FIG.2

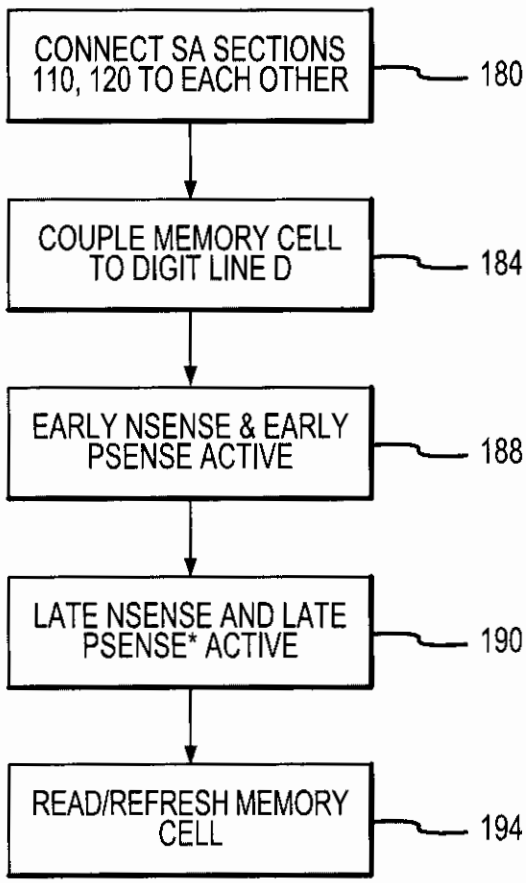

CONNECT SA SECTIONS 110, 120 TO EACH OTHER
180
COUPLE MEMORY CELL TO DIGIT LINE D
184
EARLY NSENSE & EARLY PSENSE ACTIVE
188
LATE NSENSE AND LATE PSENSE* ACTIVE
190
READ/REFRESH MEMORY CELL
194

FIG.3

REPLACEMENT SHEET
08 NOV 2006

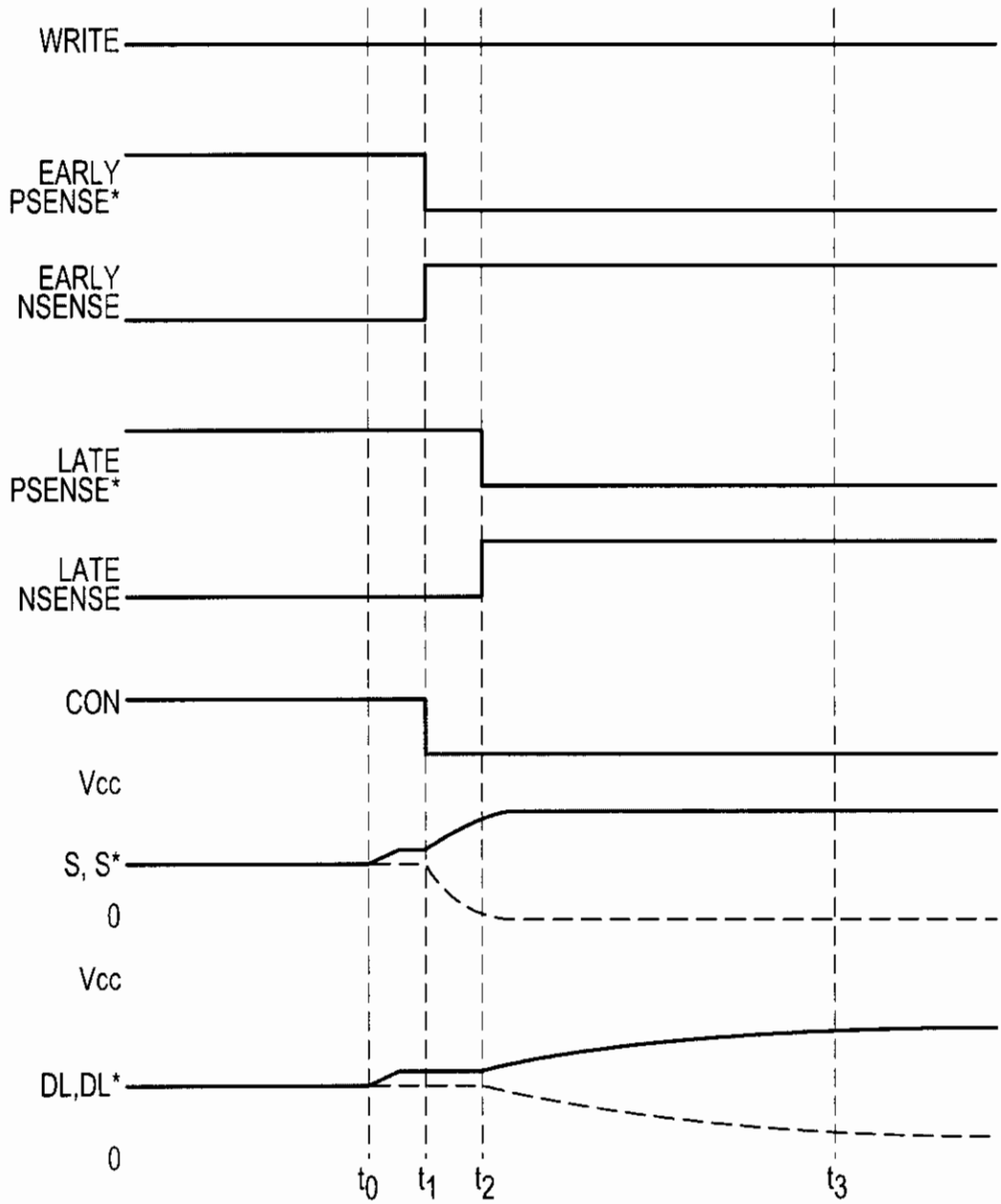


FIG.4

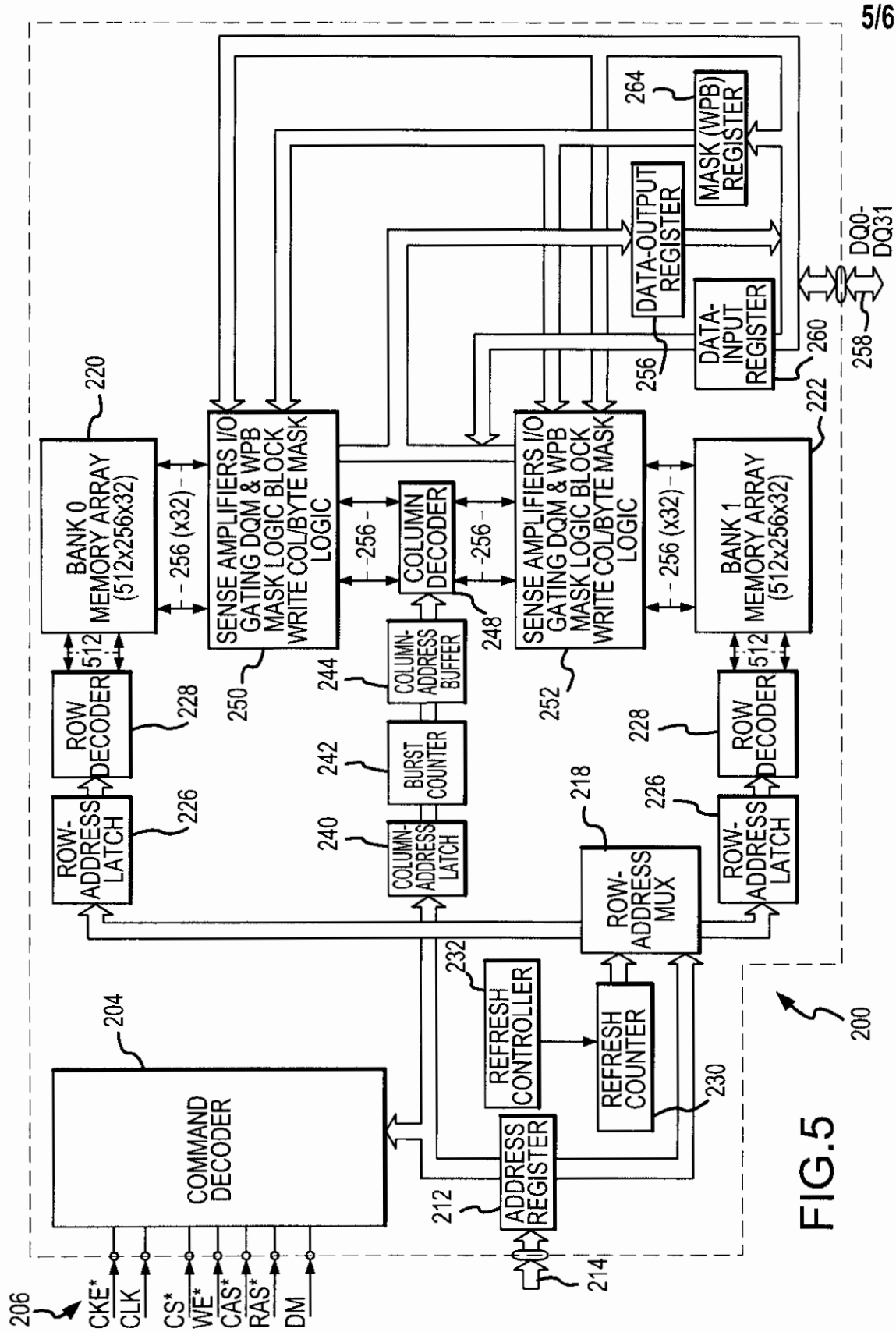

206
CKE*
CLK
CS*
WE*
CAS*
RAS*
DM
COMMAND DECODER
204
ADDRESS REGISTER
212
214
REFRESH CONTROLLER
232
REFRESH COUNTER
230
ROW-ADDRESS MUX
218
ROW-ADDRESS LATCH
226
ROW DECODER
228
BANK 0 MEMORY ARRAY (512x256x32)
220
512
256 (x32)
SENSE AMPLIFIERS I/O GATING DQM & WPB MASK LOGIC BLOCK WRITE COL/BYTE MASK LOGIC
250
256
COLUMN DECODER
248
COLUMN-ADDRESS BUFFER
244
BURST COUNTER
242
COLUMN-ADDRESS LATCH
240
SENSE AMPLIFIERS I/O GATING DQM & WPB MASK LOGIC BLOCK WRITE COL/BYTE MASK LOGIC
252
BANK 1 MEMORY ARRAY (512x256x32)
222
DATA-OUTPUT REGISTER
254
MASK (WPB) REGISTER
264
DATA-INPUT REGISTER
256
260
DQ0-DQ31
258
200

FIG.5

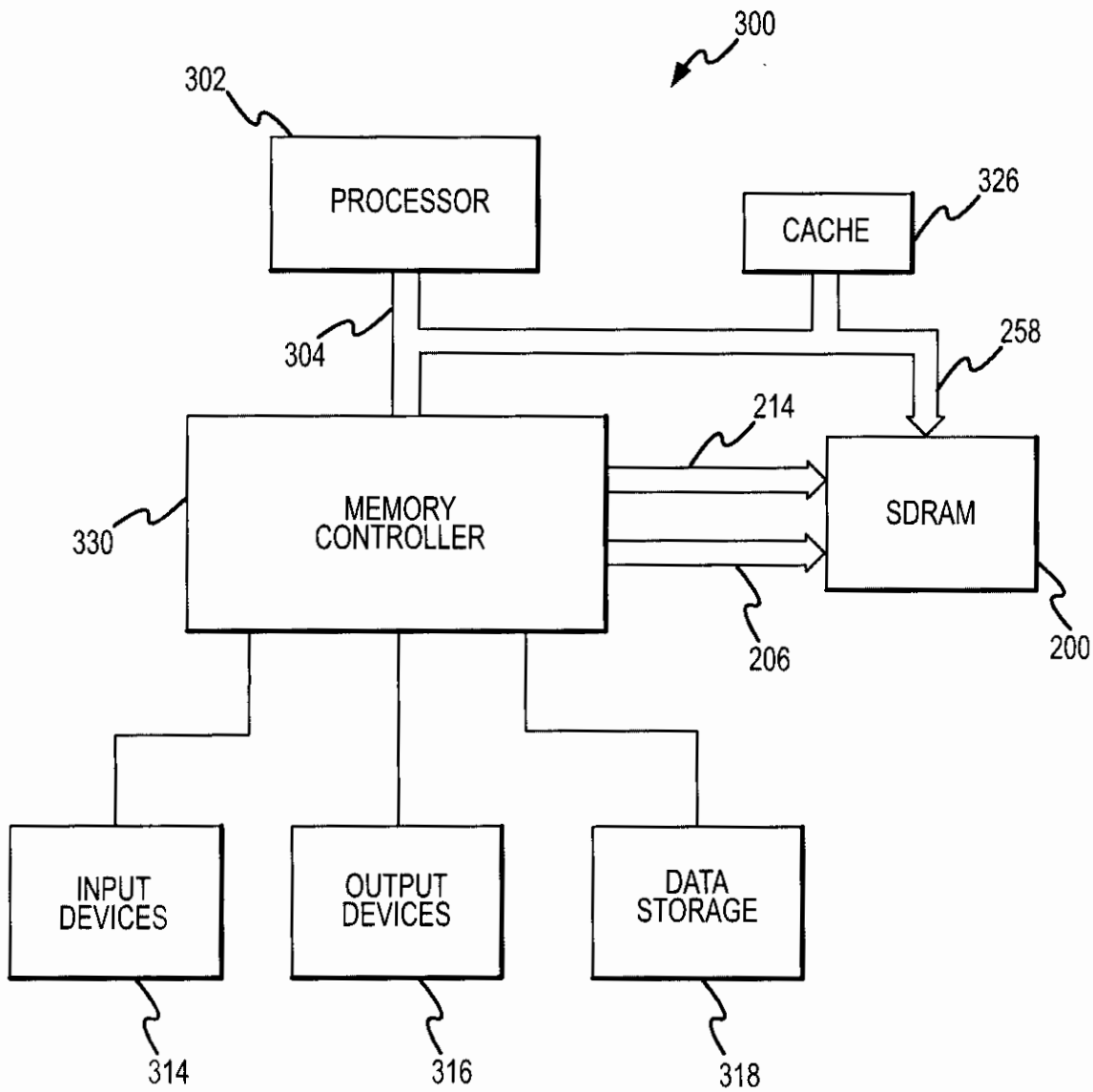

300
302
PROCESSOR
326
CACHE
304
258
214
330
MEMORY CONTROLLER
SDRAM
206
200
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE
314
316
318

FIG.6