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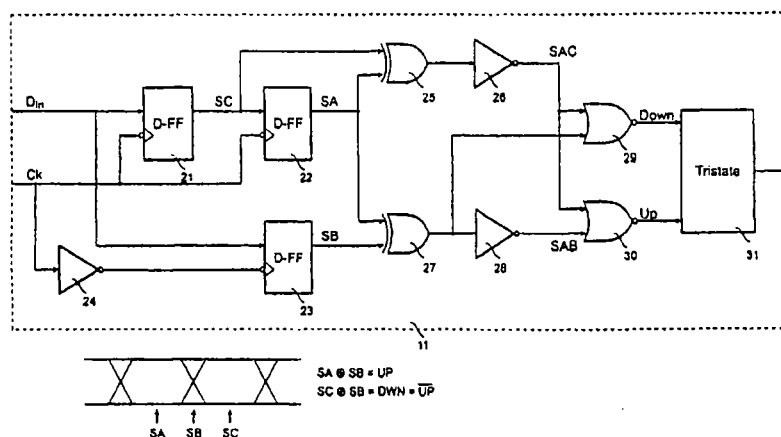
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(54) Title: A PHASE DETECTOR



(57) Abstract: The present invention relates to a phase detector and utilisation of the phase detector for synchronisation of a digital signal with a clock signal. It is an object of the present invention to provide a phase detector with improved characteristics including jitter tolerance and jitter transfer. It is another object of the invention to provide a phase detector that generates an output signal that, when used as a control signal in a phase or frequency locked loop, keeps the gain of the control loop substantially invariant to the transition density of the phase detector input signals. According to the invention, these aspects are fulfilled by provision of a phase detector for detection of a phase difference between a first signal and a second signal. The phase detector comprises a first logic circuit for detection of a data transition of the first signal and a second logic circuit that generates a logic output signal of a first logic value upon detection of a data transition of the first signal if a transition of the second signal occurs before the transition of the first signal and of a second logic value if the transition of the second signal occurs after the transition of the first signal.

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