ABSTRACT

A semiconductor memory device, includes, a cell array including a plurality of memory banks, a command decoder configured to decode a read/write command, a read command, and a write command input from outside of the semiconductor memory device, an address decoder receiving a read address and a write address, an input receiver configured to transmit write data input through a write data pad to a global input/output driver of a memory bank corresponding to the write address, and an output driver configured to transmit read data output from an input/output sense amplifier of a memory bank corresponding to the read address to a read data pad. The write data is input via the write data pad in a single data rate method and transmitted to the global input/output driver without deserialization processing. The read data is transmitted from the input/output sense amplifier to the read data pad without serialization processing.

FIG. 4