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Description

Method of producing a package for semiconductor chips

The present invention relates to a method of producing a package for semiconductor chips. The present invention relates in particular to a method of producing miniature packages or miniature housings for semiconductor chips.

With the increasing integration in information and communication technology, the requirements imposed on the constructing and connecting techniques are becoming ever greater. Ever higher requirements are imposed in particular on the package of the semiconductor chips. The package is the main medium for connecting the integrated circuit on the semiconductor chip to the rest of the system. A further reduction in the size of the structures on the semiconductor chip would be largely senseless if there were not a corresponding development in the packaging of the semiconductor chips.

To satisfy this high requirement on the packaging of the semiconductor chips, in recent years packaging methods for semiconductor chips have been proposed and developed under the designation "Chip Size Packaging" (CSP), in which the space requirement of the packaged semiconductor chip is not greater than approximately 1.2 times the unpackaged semiconductor chip. Accordingly, the integration density on the system board can be increased and parasitic effects of the package reduced, whereby ultimately the speed of the end product is significantly increased.

In the production of miniature housings for semiconductor chips, generally a specially preprocessed carrier substrate is used. This carrier substrate may

in this case be designed such that it is both relatively flexible and relatively rigid. Generally serving for attaching the semiconductor chip on the carrier substrate are full-area chip bonding tapes or elastomer layers, which in addition to fixing the semiconductor chip also serve for minimizing mechanical stresses of the overall arrangement. In particular, in the case of these technologies, the semiconductor chip is permanently connected to the carrier substrate by means of the double-sided adhesive chip bonding tapes or elastomer layers.

At the same time, packages of this type often have to satisfy extreme requirements with respect to stress absorption. In particular, it is necessary to compensate largely for thermally induced stresses, caused by different coefficients of expansion (CTE) of individual components of the package. In this respect it is generally attempted to reduce the thermomechanical stresses by means of the double-sided adhesive chip bonding tapes or elastomer layers, which to a certain extent have stress-absorbing properties. Unfortunately, so far there is no known method or material that satisfies this requirement satisfactorily. Therefore, instances of delamination in the package or damage to the semiconductor chip are repeatedly encountered.

The present invention is therefore based on the object of providing a method of producing a package for semiconductor chips which largely avoids the difficulties mentioned and which makes possible, in particular, a low-cost, virtually stress-free electrical bonding of the chip for miniature housings.

This object is achieved by the method of producing a package for semiconductor chips according to the independent patent claim 1. Further advantageous

embodiments, refinements and aspects of the present invention emerge from the dependent patent claims, the description and the accompanying drawings.

According to the invention, a method of producing a package for semiconductor chips with the following steps is provided:

a) a carrier substrate is provided,

b) at least one adhesive layer, which loses its adhesive property when it is heated above a defined temperature, is applied to the carrier substrate,

c) a semiconductor chip is applied to the carrier substrate and fixed by the adhesive layer,

d) a curable composition is applied and at least one heat treatment is carried out, the temperature of the heat treatment lying at least temporarily above the temperature at which the adhesive layer loses its adhesive property, so that the adhesive layer loses its adhesive property and the curable composition cures.

The method according to the invention has the advantage that, during the completion of the package, the mechanical connection between the semiconductor chip and the carrier substrate is released again. The mechanical connection necessary for establishing the electrical contacts between the semiconductor chip and the carrier substrate takes place only temporarily. As a result, a critical interface in the package is removed, which has the consequence of a significant reduction in the thermomechanical stresses. Accordingly, the completed package is significantly more reliable, which is in turn reflected in a reduction in the costs. With the method according to

the invention, miniature packages or miniature housings for semiconductor chips (CSP) can be produced in particular.

According to a preferred embodiment of the method according to the invention, a carrier substrate with nubbins arranged on it is provided and the adhesive layer is applied to the nubbins. The use of nubbins makes it easier for the curable composition to be applied later.

According to a preferred embodiment of the method according to the invention, in step d) a curable composition is applied and a first heat treatment is carried out, so that the curable composition solidifies, the temperature of the first heat treatment lying below the temperature at which the adhesive layer loses its adhesive property, and subsequently a second heat treatment is carried out, the temperature of the second heat treatment lying above the temperature at which the adhesive layer loses its adhesive property, so that the adhesive layer loses its adhesive property and the curable composition cures. This preferred embodiment of the method according to the invention has the advantage that, in the second heat treatment, the process parameters can be set exactly as required for a reliable and permanent release of the adhesive layer. At the same time, the second heat treatment acts like a post-curing process for the curable composition.

According to a further preferred embodiment of the method according to the invention, before step d), the semiconductor chip is electrically connected to the carrier substrate by wire or film-carrier bonding (lead bonding, TAB), the bonding temperature lying below the temperature at which the adhesive layer loses its adhesive property.

According to a further preferred embodiment of the method according to the invention, in step b) the adhesive layer is applied by a punching process. Furthermore, it is preferred if, in step b), a first adhesive layer, a base layer and a second adhesive layer is applied, at least the second adhesive layer losing its adhesive property when it is heated above a defined temperature. In this case, it is preferred in particular if the first adhesive layer, the base layer and the second adhesive layer are jointly applied in the form of a film.

According to a further preferred embodiment of the method according to the invention, a polyimide, BT or FR4 substrate is used as the carrier substrate. Furthermore, it is preferred if the carrier substrate has at least one bonding channel.

According to a further preferred embodiment of the method according to the invention, a mixture of silicone and epoxy resin is used as the curable composition. The use of a mixture of silicone and epoxy resin has the advantage over the use of pure epoxy resin that the encapsulating composition has a significantly higher flexibility even after curing. If, however, the production of a relatively rigid package is the aim, it is advantageous to use pure epoxy resin as the curable composition.

According to a further preferred embodiment of the method according to the invention, in step d) the first heat treatment is carried out at a temperature between 130° and 150°C and subsequently a second heat treatment is carried out at a temperature between 150° and 170°C.

According to a further preferred embodiment of the method according to the invention, the nubbins are applied to the carrier substrate by a printing process

and a subsequent heat treatment. Furthermore, it is preferred if the curable composition is applied by a printing process or a compression-molding process.

The invention is presented in more detail below on the basis of figures of the drawing, in which:

Figures 1 - 6 show an embodiment of the method according to the invention of producing a package for semiconductor chips, and

Figure 7 shows a plan view of a package produced in this way.

Figures 1 - 6 show an embodiment of the method according to the invention of producing a package for semiconductor chips. For this purpose, in a first step a carrier substrate 1, for example a polyimide substrate, which, for later receiving bonding wires, has a central channel 5 (slot) (figure 1), is provided. Furthermore, interconnects and landing pads (not shown) for the micro-ball grid array to be produced later are provided on one side of the carrier substrate (underside), whereby the carrier substrate 1 are connected for example to a system board. In this case, the structure shown in figure 1 generally represents only a detail of a larger carrier substrate 1, which serves for the simultaneous attachment of a number of semiconductor chips. For reasons of overall clarity, however, only the conditions for one semiconductor chip at a time are shown below.

Subsequently, nubbins 3 are applied to the carrier substrate 1, for example by means of a printing process, and are cured in an oven process. Silicone is used with preference as the material for the nubbins 3. These nubbins 3 also serve for assisting the later wire bonding. Consequently, a carrier substrate 1 with

nubbins 3 arranged on it is prepared. The resulting situation is represented in figure 2.

Subsequently, an adhesive layer 4 that is released under the influence of a defined temperature is applied to the nubbins 3. In this respect, in the case of this embodiment of the method according to the invention, the adhesive layer 4 is applied to the nubbins 3 as part of a film by a punching process. A film of this type generally comprises in addition to the adhesive layer 4 a base layer (not shown), for example polyester, and a further adhesive layer (not shown), the base layer being arranged between the two adhesive layers. Films of this type are available, for example, under the designation "Revalpha" from the company Nitto Denko. The situation resulting from this is represented in figure 3.

After that, a semiconductor chip 2 is attached on the carrier substrate 1 by means of the adhesive layer 4 (figure 4) and the electrical connection between the semiconductor chip 2 and the carrier substrate 1 is made in the bonding channel 5 by means of fine connecting wires (not shown), for example gold wires. The bonding temperature in this case lies below what is known as the "heat release" temperature, at which the adhesive layer 4 loses its adhesive property.

The overall construction is then encapsulated in a curable composition or encapsulating composition 6 adapted to the coefficient of thermal expansion of the semiconductor chip. For this purpose, the encapsulating composition 6 is applied to the structure shown in figure 4 by a printing process. A mixture of silicone and epoxy resin is used as the encapsulating composition 6. The use of a mixture of silicone and epoxy resin has the advantage over the use of pure epoxy resin that the encapsulating composition 6 has a

significantly higher flexibility even after curing. Alternatively, instead of a mixture of silicone and epoxy resin, other materials, for example pure epoxy resin, may also be used as what is known as a molding composition, in what is known as a compression-molding process.

For the curing of the encapsulating compound 6, after that a first heat treatment is carried out, so that the encapsulating composition 6 solidifies, the temperature of the first heat treatment lying below the temperature at which the adhesive layer 4 loses its adhesive property. The first heat treatment is preferably carried out at a temperature between 130° and 150°C for approximately one to two hours.

After that, a second heat treatment is carried out, the temperature of the second heat treatment lying above the temperature at which the adhesive layer 4 loses its adhesive property, so that the adhesive layer 4 loses its adhesive property and the encapsulating composition 6 fully cures. The second heat treatment is preferably carried out at a temperature between 150° and 170°C for approximately 10 to 15 minutes. This procedure has the advantage that, during the second heat treatment, the process parameters can be set exactly as required for a reliable and permanent release of the adhesive layer 4. At the same time, the second heat treatment acts like a post-curing process for the encapsulating composition 6.

After that, a micro-ball grid array 7 (or some other connecting means) is produced on the side of the carrier substrate 1 lying opposite the semiconductor chip 2, said array serving for the electrical and mechanical bonding of the complete arrangement on a printed circuit board which is not represented (figure

6). Figure 7 shows a plan view of a package produced in this way.

The method according to the invention has the advantage that, during the completion of the package, the mechanical connection between the semiconductor chip and the carrier substrate is released again. The mechanical connection necessary for establishing the electrical contacts between the semiconductor chip and the carrier substrate takes place only temporarily. As a result, a critical interface in the package is removed, which has the consequence of a significant reduction in the thermomechanical stresses.

Patent Claims

1. A method of producing a package for semiconductor chips with the steps that:

   a) a carrier substrate (1) is provided,

   b) at least one adhesive layer (4), which loses its adhesive property when it is heated above a defined temperature, is applied to the carrier substrate (1),

   c) a semiconductor chip (2) is applied to the carrier substrate (1) and fixed by the adhesive layer (4),

   d) a curable composition (6) is applied and at least one heat treatment is carried out, the temperature of the heat treatment lying at least temporarily above the temperature at which the adhesive layer (4) loses its adhesive property, so that the adhesive layer (4) loses its adhesive property and the curable composition (6) cures.

2. The method as claimed in claim 1, characterized in that a carrier substrate (1) with nubbins (3) arranged on it is provided and the adhesive layer is applied to the nubbins (3).

3. The method as claimed in claim 1 or 2, characterized in that in step d) a curable composition (6) is applied and a first heat treatment is carried out, so that the curable composition (6) solidifies, the temperature of the first heat treatment lying below the temperature at which the adhesive layer (4) loses its adhesive property, and subsequently a second heat treatment

is carried out, the temperature of the second heat treatment lying above the temperature at which the adhesive layer (4) loses its adhesive property, so that the adhesive layer (4) loses its adhesive property and the curable composition (6) cures.

4. The method as claimed in one of claims 1 to 3, characterized in that, before step d), the semiconductor chip (2) is electrically connected to the carrier substrate (1) by wire or film-carrier bonding, the bonding temperature lying below the temperature at which the adhesive layer (4) loses its adhesive property.

5. The method as claimed in one of claims 1 to 4, characterized in that in step b) the adhesive layer (4) is applied by a punching process.

6. The method as claimed in one of claims 1 to 5, characterized in that in step b) a first adhesive layer, a base layer and a second adhesive layer (4) are applied, at least the second adhesive layer (4) losing its adhesive property when it is heated above a defined temperature.

7. The method as claimed in claim 6, characterized in that the first adhesive layer, the base layer and the second adhesive layer (4) are jointly applied in the form of a film.

8. The method as claimed in one of claims 1 to 7, characterized in that a polyimide, BT or FR4 substrate is used as the carrier substrate (1).

9. The method as claimed in one of claims 1 to 8, characterized in that the carrier substrate (1) has at least one bonding channel (5).

10. The method as claimed in one of claims 1 to 9, characterized in that a mixture of silicone and epoxy resin or pure epoxy resin is used as the curable composition (6).

11. The method as claimed in claim 10, characterized in that in step d) the first heat treatment is carried out at a temperature between 130° and 150°C and subsequently a second heat treatment is carried out at a temperature between 150° and 170°C.

12. The method as claimed in one of claims 1 to 11, characterized in that the curable composition (6) is applied by a printing process or a compression-molding process.

13. The method as claimed in one of claims 2 to 12, characterized in that the nubbins (3) are applied to the carrier substrate (1) by a printing process and a subsequent heat treatment.