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(54) GAIN CONTROLLED AMPLIFIER

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, New York 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates, in general, to automatic gain control (AGC) systems for radio signal receiving apparatus and, in particular, to AGC systems for use in superheterodyne receivers incorporating intermediate frequency (I.F.) amplifiers fabricated using integrated circuit techniques.

Integrated circuit IF amplifiers with AGC are known. These prior-art IF amplifiers have comprised a cascade connection of transistor amplifier stages. A cascade connection of amplifier stages is a connection in which the input of each succeeding amplifier stage is connected to the output of its preceding amplifier stage. The gain of various of the IF amplifier stages and in many cases the gain of a preliminary radio frequency (R.F.) amplifier have been controlled by the AGC system. The AGC system maintains the signal swing at the output of the final IF amplifier essentially constant for all input signal levels except for the very smallest levels. The variations of the gains of the IF and the RF amplifier stages by the AGC system are designed to maintain an acceptable signal-to-noise ratio of the detected signal as received signal level varies. To do this, the gain of the RF amplifier stage is not reduced until the received signal is of sufficient amplitude that the noise contribution of the RF amplifier stage (and any networks which precede it) is insignificant compared to the received signal level. Thus, when the received signal level is low, the RF amplifier stage is maintained in a relatively high gain condition and each IF amplifier stage is gain controlled. The signal-to-noise ratio of the detected signal then will be determined primarily by the noise contribution of the receiver RF amplifier stage. At higher signal levels the gain of the RF amplifier stage will be reduced to obtain further gain control. This reduction of signal level in the RF amplifier stage will prevent overly large input signals to the subsequent IF amplifier stages and avoid overloading them. The procedure of maintaining the controlled RF amplifier stage gain high in the presence of smaller signal levels is commonly referred to as "delayed AGC".

In vacuum-tube gain-controlled amplifier design it is known to be preferable to use remote cut-off vacuum tubes rather than sharp cut-off vacuum tubes. In a sharp cut-off amplifying device output current is sharply reduced as input voltage swing exceeds a certain value in the direction to reduce output current. In a remote cut-off amplifying device the reduction of output current is gradual as input voltage swings in the direction to reduce output current. Transistors are sharp cut-off amplifying devices. A sharp cut-off amplifying device does not have the capability of accepting large input signals in its reduced gain condition without appreciable distortion in its output signal. Such distortion of the output signal is undesirable and is a common shortcoming of prior art gain-controlled transistor amplifiers.

The present invention concerns the parallel connection of an automatic-gain-controlled first amplifier stage with a second amplifier stage, both stages comprising a common-emitter transistor configuration. Amplifier stages are considered to be connected in parallel connections when their inputs are arranged for connection to the same source of signals and when their outputs are arranged to be coupled to the same load circuit. The maximum gain of the first amplifier stage is arranged to be higher than the gain of the second amplifier. To do this the second amplifier can be provided with degenerative feedback. This increases the capability of the second amplifier to accommodate large input signals without

having distortion in its output signals. In addition, the gain-controlled first stage is arranged to have less minimum gain than the second stage.

When small input signals are received, the automatic-gain-controlled first amplifier stage will exhibit maximum gain. The high gain of the first amplifier stage will cause the gain of the parallel amplifier combination to be high. When large input signals are received, the gain of the first amplifier is reduced and the gain of the parallel amplifier combination is predominantly determined by the second amplifier. The AGC does not reduce the gain of the second amplifier as effectively as it can the gain of the first amplifier. Therefore, the gain of the first amplifier will be reduced more rapidly than it would be in the absence of the second amplifier. The output signal of the parallel amplifier combination will for high-level input signals be composed predominantly of output from the second, degenerated amplifier. Therefore, the output signals will be essentially undistorted despite the high level of the input signals. The parallel amplifier combination will form a gain-controlled amplifier which has the desirable characteristics of a gain-controlled amplifier employing a remote cut-off device.

For very high frequency operation (e.g., 45 MHz) it is desirable to couple a variable-gain common-emitter amplifier transistor to its collector load via a common-base amplifier transistor. This mode of connection is termed a cascode connection. The cascode connection reduces the harmful effects of the collector-to-base, collector-to-emitter and collector-to-substrate capacitances of the common-emitter amplifier transistor upon the high-frequency response of the amplifier. However, these capacitances provide an effective emitter by-pass capacitor for the higher frequency components of the noise generated internally in the common-base amplifier transistor. Consequently, the internal noise of the common-base amplifier degrades the signal-to-noise ratio of the cascode connection.

A further aspect of the present invention is that, when the first and second amplifiers in parallel combination are each a cascode amplifier, the common-emitter amplifier transistor of the first amplifier may be a large area device as compared to the common-emitter amplifier transistor of the second amplifier. The larger area common-emitter transistor in the first amplifier can provide high signal gain at high quiescent current levels. The smaller area common-emitter transistor will contribute minimally to the degradation of output signals caused by the phenomenon described in the previous paragraph

In accordance with an embodiment of the present invention, an intermediate-frequency amplifier is arranged for automatic gain control operation over a range from a relatively high gain control operation over a range from a relatively high gain to a voltage gain equal to or less than unity (i.e. 1). The form of the amplifier is such that it is suited to construction in integrated circuit form. The integrated circuit structure and the resulting circuit configuration can be arranged to provide improved signal-to-noise characteristics for such low gain operation.

A specific embodiment of the present invention is a gain-controlled IF amplifier built in integrated ciriuit form. This gain-controlled IF amplifier comprises the parallel combination of two cascode amplifiers. A dual-emitter transistor is used to provide the common-base amplifier stage of each of the two cascode amplifiers. The first emitter of the dual-emitter transistor is provided signal from the collector electrode of a first input transistor. This first input transistor is connected as a grounded-emitter amplifier stage. The second emitter of the dual-emitter transistor is provided signal from the collector electrode of a second input transistor. This second input transistor is provided with a negative feedback emitter resistor and arranged to provide unity gain. Signals and AGC potential are supplied to the input of each of the first and second transistors such that, for low signal levels, relatively high controllable gain is provided by the cascode configuration including the first transistor. For higher signal levels, the gain of the first transistor is reduced ultimately to zero and the cascode configuration includes only the second transistor and the dual-emitter output transistor, thereby providing substantially unity voltage gain. Furthermore, the physical size and geometry of the first and second input transistors are selected (1) to provide a relatively wide gain range and (2) to present a relatively small capacitance load to the common-base dual-emitter transistor under low gain conditions.

In accordance with another aspect of the invention, the gain of the IF amplifier is capable of reduction below unity voltage gain by attenuator action. Such attenuator action is provided by means of a fourth transistor coupled to supply input signals to the first and second input (common-emitter) transistors. The fourth transistor is arranged to operate, when reverse-biased, as a variable capacitor (that is, as a varactor diode) to provide, in conjunction with an associated impedance, a controllable voltage divider across the inputs of the first and second input transistors.

Another aspect of the present invention is the provision of an automatic gain con-

trol (AGC) circuit immune to the deleterious effects of impulse noise which may be present in a received television signal. A source of keying pulses which occur in time coincidence with the synchronizing pulse components of a detected video signal are applied to the input circuit of an AGC transistor. Switch means responsive to the synchronizing signal components of the detected video signal is coupled across the input circuit to control the amplitude of keying pulses applied to the AGC transistor. A means responsive to the impulse noise accompanying the detected video signal is coupled to the keying pulse source to control the amplitude of the keying pulses applied to the AGC generating circuit.

In accordance with a further aspect of the present invention, means are coupled to the AGC transistor, under control of the switch means, for supplying additional currents thereto to prevent AGC lockout upon the occurrence of sudden increases in received signal level and to speed the response of the AGC system under non-synchronized, strong signal conditions.

The present invention and its various objects will be better understood by reading the following specification and looking at the attached drawing in which:

Figure 1 illustrates, partially in block diagram and partially in schematic diagram form, a portion of a television receiver constructed in accordance with the present invention; and

Figure 2 illustrates in pictorial form, a portion of an IF amplifier stage arrangement constructed as an integrated circuit in accordance with certain aspects of the present invention.

Referring to Figure 1, the dashed line rectangle 10 schematically represents a monolithic semiconductor integrated-circuit chip. The chip 10 has a plurality of contact areas or terminals (T_1—T_{11}) about its outer edge. Connections from the internal circuitry of chip 10 to external elements are made via these terminals. Chip 10 includes a first IF amplifier indicated generally by the reference numeral 12, second and third IF amplifiers 14, a video detector 16, a first video amplifier 18, keyed AGC circuitry to develop AGC potential indicated generally by the reference numeral 20, and a source of delayed AGC voltages to control the RF amplifier stage, and which source of delayed AGC voltages is indicated generally by the reference numeral 22.

In a television receiver employing the chip 10, modulated carrier wave television signals are received by an antenna 24 and are coupled to a television tuner 26. Tuner 26, typically includes an RF amplifier stage and a frequency converter. The tuner 26 performs the conventional functions of (1) selectively amplifying a desired one of various received RF television signals and (2) converting the selected RF signal to an intermediate frequency (IF) signal. The RF amplifier of tuner 26 is arranged for gain control in a conventional manner compatible with the AGC system to be described below.

Amplified intermediate-frequency signals are coupled by means of a first frequency-selective network 28 and an IF input terminal T_1 of chip 10 to first IF amplifier stage 12. A second frequency-selective network 30, located externally to chip 10 is coupled between the output of amplifier 12 and the input of second and third IF amplifier stages 14 via chip terminals T_2 and T_4.

The amplified intermediate-frequency output signal of second and third IF amplifier stages 14 is coupled to video detector 16. The video detector 16 operates to recover image-representative and synchronizing signal components from the intermediate-frequency signals. The output of video detector 16 is amplified in a first video amplifier 18. The video output signal of the video amplifier 18 has negative-going synchronization pulses. This video output signal is coupled via chip terminal T_5 to additional conventional television signal processing apparatus external to chip 10.

Video amplifier 18 also supplies signals to AGC source 20, which is of the type described in our Patent Application No. 9873 of 1970 (Serial No. 1,290,091). Additional aspects of AGC potential source 20 are also described in concurrently filed Application No. 14771/71 (Serial No. 1,343,466). AGC source 20 operates as a keyed AGC system. A keyed AGC system in a television receiver comprises a detector which is sensitive to the amplitude of the detected video signal during short periodically recurring intervals. These intervals of detector sensitivity are arranged to coincide with the intervals when synchronizing pulses are present in the video signal. The gains of the video IF amplifiers and RF amplifiers are controlled to maintain the amplitude of the synchronizing pulses substantially constant despite the variation of RF input signal level. With this mode of operation the AGC system will be unaffected by impulse noise occurring at times between the intervals when the detector is made sensitive to detected video signal.

The keyed AGC system is supplied via chip terminal T_6 with keying pulses from a keying pulse source 32 such as a horizontal deflection output transformer (not shown) of the television receiver. AGC source 20 is coupled via chip terminal T_3 to an external AGC filter network 34. The AGC filter network 34 comprises the parallel combination of a resistor 36 and a capacitor 38. A source of voltage (B^+) is also coupled

via the series combination of resistor 40 and resistor 42 to filter network 34. Negative feedback is provided from the output of IF amplifier 12 via frequency-selective network 30 to the input of amplifier 12 (i.e. via the junction of resistors 40, 42). The feeback from network 30 and the AGC voltage produced across filter network 34 is coupled via a resistor 44 to IF amplifier input terminal T_1 for gain control of first IF amplifier 12 as will be explained below. Appropriate AGC voltage is also coupled, as will be explained below, via delay network 22 and chip terminal T_{10} to the RF amplifier of tuner 26. An external AGC delay control comprising a variable resistor 46 coupled across a suitable voltage source (e.g., B^+) is coupled via a resistor 48 and chip terminal T_{11} to delay network 22.

Ground terminals T_7 and T_9 are provided, respectively, for the high and low signal level portions of chip 10.

Operating voltage (B^+) is supplied to various portions of the circuitry included within chip 10 via terminal T_2. Operating voltage is typically 11 volts. First IF amplifier 12 is supplied with relatively noise-free operating voltage by means of a dynamic noise filter 50 coupled to terminal T_2. Noise filter 50 is described in Application No. 9874 of 1970 (Serial No. 1,290,092) supplies substantially identical but de-coupled voltages at circuit terminals 52 and 54.

In chip 10 the intermediate-frequency signals supplied by frequency-selective network 28 and the AGC voltage supplied by filter network 34 at terminal T_1 are directly applied to the base electrode of an input transistor 56. The collector electrode of transistor 56 is connected to an operating voltage supplied at point 54. The emitter electrode of transistor 56 connects to the base electrode of a subsequent emitter-follower transistor 58. The capacitance associated with the base-emitter semiconductor of transistor 56 is shown in dotted lines and is designated by the reference numeral 56d. As will be explained below, for large input signals, capacitor 56d is varied as a function of AGC voltage and serves as an attenuator in conjunction with the resistance which appears between the emitter electrode of transistor 56 and ground. A load resistor 60 is connected between the emitter electrode of emitter-follower transistor 58 and ground.

Signals appearing across load resistor 60 are coupled to the base electrode of a grounded-emitter transistor 62. The collector electrode of transistor 62 is connected to one of the emitter electrodes of a dual-emitter transistor 64. Operating potential (B^+) is supplied to the collector electrode of transistor 64 via a direct-current path through the second frequency-selection network 30. A high-gain cascode amplifier stage is formed by transistors 62 and 64 for supplying amplified IF signals to subsequent stages via the second frequency selective network 30. Transistor 62 has a relatively high maximum transconductance (g_m) which can be varied as a function of AGC biasing voltage applied from terminal T_1. In the illustrated circuit, reverse AGC is utilized. That is, the gain of transistor 62 is reduced by decreasing the positive bias voltage supplied to its base electrode from terminal T_1 via transistors 56 and 58.

The emitter electrode of input transistor 56 is also directly coupled to the base electrode of a transistor 66. The collector electrode of transistor 66 is coupled to the second emitter electrode of transistor 64. A bias voltage divider comprising resistors 68 and 70 is coupled between the base electrode of transistor 66 and ground. The junction of resistors 68 and 70 is connected to the emitter of transistor 66. The biasing resistors 68 and 70 are selected so that transistor 66 is biased for conduction whenever transistor 62 conducts. Furthermore, the resistors are selected so that transistor 66 remains biased for conduction when transistor 62 is cut off. Transistor 66 is a relatively small area device as compared to transistor 62. Transistors 66 and 64 form a low gain (e.g., unity gain) cascode amplifier stage which acts in parallel with the high gain cascode stage 62, 64 for coupling high-level IF input signals from transistor 56 to subsequent stages. The operation of transistor 66 will be explained in greater detail below.

Control of the gain of the cascode-connected first IF amplifier stage (transistors 62, 64, 66) for relatively low-level input signal conditions has been described. For higher-level input signals additional gain control of the overall RF and IF amplifier system is obtained by (1) varying the gain of the RF amplifier of tuner 26, (2) varying the transconductance of transistor 56 and (3) providing for attenuator operation of transistor 56. The manner in which these three functions are obtained will now be described.

The emitter electrode of input transistor 56 is coupled to AGC delay network 22. Specifically, the base electrode of a transistor 72 is coupled to AGC delay network 22. Specifically, the base electrode of a transistor 72 is coupled via a resistor 74 to the emitter electrode of transistor 56. The input (base-emitter path) of transistor 72 is substantially in parallel with the input of transistor 66 and is biased by means of a voltage divider comprising resistors 76 and 78. Operating voltage is supplied to the collector electrode of transistor 72 by means of the external AGC delay control comprising resistors 46, 48 and the B^+ supply. Bias and operating

voltage parameters associated with transistor 72 are selected such that, during no signal or relatively weak signal conditions transistor 72 is maintained in full, saturated conduction.

A transistor 80 is connected as an emitter-follower coupling the collector electrode of transistor 72 to the base electrode of a dual-emitter transistor 82. The collector electrodes of transistors 80 and 82 are shown connected to point 54, which supplies them operating potential. When transistor 72 is maintained full conductive during no-signal or weak-signal conditions, transistor 82 will be held non-conductive.

One emitter electrode of transistor 82 is coupled via resistor 84 to the base electrodes of transistors 58 and 66. The other emitter electrode of transistor 82 is coupled to a voltage divider comprising resistors 86 and 88. Resistor 84, as will appear below, in combination with capacitor 56d, provides attenuator operation for strong-signal conditions. Resistor 84 also serves, for medium-signal and strong-signal conditions, to close a negative feedback loop to the base electrode of transistor 72. Under medium-signal and strong-signal conditions, the applied AGC voltage reduces the conduction of transistor 72, causing it to come out of saturation. The collector voltage of transistor 72 then rises, causing transistors 80 and 82 to conduct. The voltage divider 86, 88 is selected such that when a predetermined level of AGC voltage (corresponding to a certain IF signal level) is reached, a further transistor 90 conducts and supplies suitable AGC voltage to tuner 26. A base resistor 92, an emitter resistor 94 and an external collector voltage level translating network 96 coupled to terminal T_{10} are associated with transistor 90.

The keyed AGC circuit 20 shown in Figure 1 is arranged so that the collector current of transistor 98 will discharge AGC filter capacitor 38 when the video output level of video amplifier 18 exceeds a predetermined level. The reduction of AGC voltage causes the gain of appropriate ones of the IF and RF amplifier elements to be reduced. If the video output level decreases below the desired level (such as might happen during a fade in input signal), capacitor 38 is charged up to an increasingly positive voltage. The charging current flows from the B^+ supply via resistors 40 and 42. As a result of the increased AGC voltage the signal gain of the appropriate amplifying elements will be increased.

Now the way the desired AGC characteristics are provided will be described. This will be done by considering the operation of the circuitry as received signal level is progressively increased from no-signal to a maximum-signal input level.

When there is no received signal, tuner 26 and IF amplifier 12 are operated at maximum gain. That is: (1) AGC capacitor 38 charges to a relatively high positive voltage; (2) transistors 56, 58, 62, 64 and 66 are all biased for maximum gain and (3) transistor 72 is biased into saturation. Transistors 80, 82 and 90 are cut off (i.e., non-conducting). As received signal strength increases, the signals are amplified by the active elements preceding detector 16 and their level is sensed at AGC source 20. When a predetermined, acceptable video signal level is reached, AGC source 20 begins to operate to decrease the AGC voltage supplied to terminal T_1. The gain of transistor 62 is thereafter decreased so as to maintain the video signal output at terminal T_5 at its predetermined desired level. During low-level input signals, transistor 66 is conducting. However, it provides only substantially unitary voltage gain. Therefore, its contribution to the signal supplied to grounded-base transistor 64 is insignificant compared to that supplied by the high gain (e.g. $g_m = .05$ mho) transistor 62. Furthermore, since transistor 72 is saturated, tuner 26 is operated at maximum gain.

As the received signal level increases and the AGC voltage supplied to terminal T_1 becomes less positive, the gain of transistor 62 is decreased. This decrease will proceed, for example, at a rate of 6db for each 20 millivolts of AGC voltage change. When the AGC voltage decreases to a sufficiently low positive level, transistor 72 comes out of saturation, causing transistors 80 and 82 to conduct. Transistors 72, 80 and 82 then provide a negative feedback function which tends to stabilize the input to transistors 66 and 58 (and therefore to transistor 62). The biasing resistors 68, 70, 76 and 78 are selected to provide the desired transition between operating modes before transistor 62 is removed from conduction.

Any further increase in signal level and its resulting decrease in AGC voltage level produces very little change in gain of the cascode amplifier 62, 64, 66. The AGC transistor 98 therefore conducts heavily to reduce the AGC voltage across capacitor 38 at a more rapid rate. Since transistors 80 and 82 are conducting, AGC voltage is transferred, after division by resistors 86, 88 and translation by network 96 to the RF amplifier of tuner 26. Transistor 62 passes through a low-gain, distortion-producing condition as it is removed from conduction. However, the transition occurs rapidly and transistor 64 provides a substantially distortion-free main output current component to overcome any adverse effect of such distortion. The cascode amplifier 64, 66 operates in a relatively fixed, substantially unity

signal voltage gain condition for any further increases in signal.

A signal level increases further the AGC voltage across capacitor 38 continues to decrease. The gain of the tuner 26 is thereby decreased until the RF amplifier is reduced to its minimum gain condition. At that time the direct AGC voltage supplied to terminal T_1 is low enough to affect the transconductance of input transistor 56, the emitter electrode of which is clamped by the feedback circuit 72, 80, 82. For further increases in signal level, the gain of tuner 26 remains at a minimum while the transconductance of input transistor 56 is reduced until transistor 56 is no longer conductive.

At this time, the base-emitter capacitance 56d of transistor 56 serves to provide, in conjunction primarily with resistor 84, a voltage divider or signal attenuator operation. The reverse-biased junction capacitance 56d acts as a varactor, the capacitance of which decreases as the applied AGC voltage becomes less positive. At the signal frequencies in question (i.e., approximately 50 MHz), this capacitive change is sufficient to provide a desired attenuation characteristic for very high input signal levels. The overall signal voltage gain of the first IF amplifier stage between input terminal T_1 and terminal T_4 (the input to second IF amplifier 14) is reduced under these conditions to less than unity. It should also be noted that the signal voltage gain of tuner 26 is substantially unity. Therefore, the signal-to-noise ratio of detected signals is affected by any noise source up to and including IF amplifier 12. AGC systems of television receivers customarily are arranged so that the peak-to-peak amplitude of low frequency synchronizing signals is maintained at a predetermined level at the output of the video detector. Normally, the synchronizing pulse tip level is in a fixed ratio with the maximum chrominance signal level. Then, the AGC system operates to provide satisfactory signal to noise ratio of both luminance and chrominance components. However, there are conditions where this relationship will unfortunately not be maintained.

For instance, in mass production of color television receivers, the frequency selectivity (i.e. bandpass characteristics) of the RF and IF amplifier stages may depart from the desired nominal response. The relative amplitudes of the low frequency (sync and luminance) and high frequency (chrominance) signal components in the detected video signal will consequently not be correct. Furthermore, such signal components are so widely spaced apart from each other in frequency that different transmission and reception conditions can cause their relative amplitudes to be incorrect. Multipath reflections, different cable impedances on wired systems, antenna impedance variations, etc., can cause this problem. Thus, for example, the chrominance signal component of the received signal may be processed with too low gain since it is too small with respect to the lower frequency components to which the AGC system responds. Suppose the received signal is relatively strong, but that the chrominance component is reduced relative to luminance. The AGC system of the receiver will then operate so as to reduce the gain of the amplifier stages to such an extent that, while the luminance signal-to-noise ratio is adequate, the chrominance signal-to-noise ratio may be unacceptably poor. In many modern television receivers the chrominance amplifiers are provided with their own AGC, which is popularly called "automatic color control" or "ACC". These chrominance amplifiers with ACC cause the chrominance signal to be maintained at full amplitude, even when its amplitude is reduced in the video detector output signal. If the signal-to-noise ratio of the chrominance signals supplied to these chrominance amplifiers is unacceptably poor, unwanted colored "snow" caused by the noise will appear on the kinescope during reception of color program material.

To avoid the problems associated with the above-described conditions and also to provide a relatively wide signal level handling range in a receiver, employing automatic gain control, any sources of noise energy within the signal amplifier chain beyond the input stage must have their effect upon the amplified signal minimized. These problems must be given particularly careful consideration in an AGC system intended for use with an IF amplifier constructed in integrated circuit form, since the gain range and signal level handling capabilities of individual stages are restricted.

The manner in which a portion of integrated circuit chip 10 is constructed to avoid noise problems will now be explained in connection with Figure 2 which shows a pictorial view of chip 10 including several transistors, 56, 62, 64 and 66; terminals T_1, T_3 and T_6 and conductive interconnections associated with such components. The manner in which the illustrated structure is fabricated is well known and will not be described in detail. For purposes of the present invention, it is sufficient to state that the chip 10 is made of semiconductor material, preferably silicon, having a layer of N type conductivity. The N type material is formed, for example, as an epitaxial layer on a P type substrate. "Boats" of N type material to serve as transistor collector regions can then be formed by diffusing P^+ regions through the N type material to the P type substrate.

Each of the illustrated transistors 56, 62, 64 and 66 is formed in a separate boat of N type material forming the collector of the transistor by diffusion of the aforementioned P^+ isolation around the periphery of each of the collector regions 56c, 62c, 64c, 66c. Base diffusions 56b, 62b, 64b, and 66b of P type material (shown lightly stippled or shaded) are formed in each of the respective collector regions and, subsequently, corresponding emitter regions of N type material 56e, 62e, 64e, $64e_2$, and 66e are formed by diffusion. The transistors are interconnected in accordance with the schematic diagram of Figure 1 by a metallization pattern (segments of which are designated M) which is applied in a conventional manner over an oxide layer (not shown) having openings at the appropriate contact areas of the transistors and other components.

Transistor 62 is constructed, as noted in connection with Figure 1, as a device having a controllable, relatively high maximum transconductance at the operating intermediate frequencies (of the order of 45 MHz). As such, the area of collector region 62c is relatively large. Furthermore, the base region 62b is provided with two metallization contacts M, one adjacent each side of emitter region 62e to provide the desired high gain characteristics as is well known.

Transistor 66, on the other hand, is a relatively small geometry device having a collector region 66c (one edge of which is hidden by metallization M but is in line with the corresponding edge of collector 62c), which is of smaller area than collector region 62c. A relatively small base area 66b having a single contact and a correspondingly small emitter area 66e are also provided. The area of each of the transistors 62 and 66 determines a capacitance between the N type collector region of the transistor and the adjacent P type substrate. The devices are drawn to scale to illustrate the difference in size, the scale being such that the terminal T_1, in the actual chip, is 0.1 mm by 0.1 mm. Terminal T_9 is formed by means of a P^+ diffusion connected to the P type substrate. The metallization M connected to terminal T_9 is also connected externally of the chip to ground as shown in Figure 1. Each of transistors 62 and 66 therefore exhibits a predetermined capacitance between collector and ground. The capacitance of the larger area device 6 is approximately twice the capacitance of the smaller area device 66. This characteristic of the transistors 62, 66 is of particular significance in connection with their operation in the large-signal, low IF amplifier gain portion of the circuit characteristics described above.

That is, as stated above in connection with Figure 1, as the received signal level increases, the AGC voltage supplied from filter network 34 via terminal T_1 becomes less positive. The gain of transistor 62 is reduced. Eventually, such gain approaches the unity gain level associated with transistor 66. As this reduction of the gain is transistor 62 takes place, the emitter impedance of each of transistors 62 and 64 increases in a similar manner (e.g., from approximately 10 ohms to 1000 ohms). This similar increase is because transistors 62 and 64 are coupled in series relation. The collector-to-substrate capacitance of transistor 62 is such that the impedance which it presents at the operating frequency (e.g., approximately 45Mhz) is also approximately 1000 ohms. The emitter impedance of transistor 64 and the impedance of the collector-to-substrate capacitance of transistor 62 are of the same order of magnitude. Therefore, a substantial portion (approximately one-half) of the signal current supplied by transistor 62 flows through its collector-to-substrate capacitance rather than through transistor 64. At the same time, that capacitance also acts as an emitter load impedance for internal noise generated by transistor 64. The combined effect of (1) the reduction of signal supplied to transistor 64 and (2) the undiminished noise contribution of transistor 64 serves to degrade the signal-to-noise ratio of the IF amplifier 12 (which is, at this time, operating at approximately 0dB gain). To eliminate this additional noise source, the second input transistor 66 is provided. As the gain of transistor 62 is reduced to the above-described low level and becomes nearly non-conductive, the rate at which the gain of IF amplifier 12 changes (i.e. dB gain change per millivolt of AGC potential change) decreases substantially. The AGC system operates, as signal level increases, to drive transistor 62 rapidly out of conduction. The emitter electrode of transistor 64, to which the collector electrode of transistor 62 is coupled, therefore is no longer provided with direct current. The base-emitter semiconductor junction of transistor 64 which to the collector-to-substrate capacitance of transistor 62 is effectively disconnected from the operating circuit. The smaller collector-to-substrate-capacitance of transistor 66 does not cause the pronounced degradation of signal-to-noise ratio encountered with the larger collector-to-substrate capacitance of transistor 62. Signal-to-noise performance of the receiver is therefore improved.

As noted above when explaining Figure 1, transistor 56 operates to provide a base-to-emitter capacitance which, under reverse-bias conditions, varies inversely with the applied reverse bias. The geometry of transistor 56 which provides this desired characteristic is illustrated in Figure 2. The capa-

citance variation is of the order of several picofarads. This capacitance variation operating in combination with the resistance including resistor 84 attenuates high-level input signal to prevent overload of IF amplifier 12.

While the use of parallel amplifiers in a gain-controlled amplifier has been described in terms of a preferred embodiment, various modifications may be made within the scope of the invention. For example, while transistor 64 has been illustrated as a single transistor device having a dual-emitter construction, it can be replaced by two separate transistors each connected in a common base configuration. Such separate transistors would have their base electrodes connected together, their collector electrodes connected together and their respective emitter electrodes connected to the collectors of transistors 62 and 66. The dual-emitter transistor, however, occupies less space upon the integrated circuit chip than two separate single-emitter transistors. This is because less area is required to make ohmic contacts (connections) between the metalization and base and collector semiconductor regions with the dual-emitter transistor than would be the case with two separate single-emitter transistors. Also, the area on the chip needed to isolate two separate transistors is saved.

When the operating frequencies of the gain-controlled IM amplifier are not in the 45 MHz region, but are appreciably lower, the common-emitter amplifier transistors 62 and 66 may not need to be in cascode connection. The cascode connection minimizes the effects of collector-to-base, collector-to-emitter and collector-to-substrate capacitances upon the bandwidths of the common-emitter amplifiers. At lower frequencies the effect of these capacitances upon the bandwidths of the amplifiers may be unimportant. In that case, these amplifier transistors 62 and 66 might be directly connected to a common load (e.g., the primary winding of a double-tuned coupling transformer). The parallel combination of the common-emitter transistors 62 and 66 would still provide the overall characteristics of a gain-controlled device with remote cut-off characteristic which is not found in conventional gain-controlled transistor amplifiers.

In the illustrative embodiment of the present invention shown in Figure 1 gain-control signals are applied to transistor 66 as well as to transistor 62. The effect of the gain-control signals upon transistor 66 is less pronounced than their effect upon the grounded-emitter transistor 62 because of the negative feedback provided by transistor 66 by its emitter degeneration resistor 70. In circuits where a wide gain control is less necessary but where it is still desired to improve signal-to-noise ratio during the reception of high-level input signals, one may use a fixed-gain amplifier in conjunction with a gain-controlled amplifier.

WHAT WE CLAIM IS:—

1. A gain-controlled amplifier circuit having a first transistor connected as a gain-controlled first common-emitter amplifier stage, and, a second transistor connected as a second common-emitter amplifier stage, said stages being arranged for connection in parallel with each other and said gain-controlled first common-emitter amplifier stage having greater maximum gain and less minimum gain than said second common-emitter amplifier stage.

2. A gain controlled amplifier as claimed in claim 1 wherein the second common-emitter amplifier stage has degenerative feedback.

3. A gain-controlled amplifier circuit as claimed in claim 1 or claim 2, in which the emitter electrode of said second transistor is coupled through a first resistor to a reference potential point, the emitter electrode of said first transistor is arranged to be directly connected to the same reference potential, the base electrode of said second transistor is adapted to receive a signal to be amplified superimposed upon an AGC potential, and, a first common-collector amplifier stage couples the base electrode of said second transistor to the base electrode of said first transistor.

4. A gain-controlled amplifier circuit as claimed in claim 3 further including an auxiliary transistor connected in a second common-collector amplifier stage with the base electrode of said second transistor adapted to receive said superimposed signal via said second common-collector amplifier stage, and a (second) resistor connecting the emitter electrode of said auxiliary transistor to a source of delayed AGC potential.

5. A gain controlled amplifier circuit as claimed in claim 4 wherein said auxiliary transistor is arranged to operate, when reverse biased, as a variable capacitor providing attenuation of said superimposed signal in conjunction with said (second) resistor.

6. A gain-controlled amplifier circuit as claimed in any of the previous claims, wherein there is a first common-base transistor amplifier stage for connecting the collector electrode of said first transistor to a common load for said common emitter stages, and a second common-base amplifier stage for connecting the collector electrode of said second transistor to said output load, the said second transistor having smaller effective by-pass capacitance associated with its collector than said first transistor.

7. A gain controlled amplifier circuit as

citance variation is of the order of several picofarads. This capacitance variation operating in combination with the resistance including resistor 84 attenuates high-level input signal to prevent overload of IF amplifier 12.

While the use of parallel amplifiers in a gain-controlled amplifier has been described in terms of a preferred embodiment, various modifications may be made within the scope of the invention. For example, while transistor 64 has been illustrated as a single transistor device having a dual-emitter construction, it can be replaced by two separate transistors each connected in a common base configuration. Such separate transistors would have their base electrodes connected together, their collector electrodes connected together and their respective emitter electrodes connected to the collectors of transistors 62 and 66. The dual-emitter transistor, however, occupies less space upon the integrated circuit chip than two separate single-emitter transistors. This is because less area is required to make ohmic contacts (connections) between the metalization and base and collector semiconductor regions with the dual-emitter transistor than would be the case with two separate single-emitter transistors. Also, the area on the chip needed to isolate two separate transistors is saved.

When the operating frequencies of the gain-controlled IM amplifier are not in the 45 MHz region, but are appreciably lower, the common-emitter amplifier transistors 62 and 66 may not need to be in cascode connection. The cascode connection minimizes the effects of collector-to-base, collector-to-emitter and collector-to-substrate capacitances upon the bandwidths of the common-emitter amplifiers. At lower frequencies the effect of these capacitances upon the bandwidths of the amplifiers may be unimportant. In that case, these amplifier transistors 62 and 66 might be directly connected to a common load (e.g., the primary winding of a double-tuned coupling transformer). The parallel combination of the common-emitter transistors 62 and 66 would still provide the overall characteristics of a gain-controlled device with remote cut-off characteristic which is not found in conventional gain-controlled transistor amplifiers.

In the illustrative embodiment of the present invention shown in Figure 1 gain-control signals are applied to transistor 66 as well as to transistor 62. The effect of the gain-control signals upon transistor 66 is less pronounced than their effect upon the grounded-emitter transistor 62 because of the negative feedback provided by transistor 66 by its emitter degeneration resistor 70. In circuits where a wide gain control is less necessary but where it is still desired to improve signal-to-noise ratio during the reception of high-level input signals, one may use a fixed-gain amplifier in conjunction with a gain-controlled amplifier.

WHAT WE CLAIM IS:—

1. A gain-controlled amplifier circuit having a first transistor connected as a gain-controlled first common-emitter amplifier stage, and, a second transistor connected as a second common-emitter amplifier stage, said stages being arranged for connection in parallel with each other and said gain-controlled first common-emitter amplifier stage having greater maximum gain and less minimum gain than said second common-emitter amplifier stage.

2. A gain controlled amplifier as claimed in claim 1 wherein the second common-emitter amplifier stage has degenerative feedback.

3. A gain-controlled amplifier circuit as claimed in claim 1 or claim 2, in which the emitter electrode of said second transistor is coupled through a first resistor to a reference potential point, the emitter electrode of said first transistor is arranged to be directly connected to the same reference potential, the base electrode of said second transistor is adapted to receive a signal to be amplified superimposed upon an AGC potential, and, a first common-collector amplifier stage couples the base electrode of said second transistor to the base electrode of said first transistor.

4. A gain-controlled amplifier circuit as claimed in claim 3 further including an auxiliary transistor connected in a second common-collector amplifier stage with the base electrode of said second transistor adapted to receive said superimposed signal via said second common-collector amplifier stage, and a (second) resistor connecting the emitter electrode of said auxiliary transistor to a source of delayed AGC potential.

5. A gain controlled amplifier circuit as claimed in claim 4 wherein said auxiliary transistor is arranged to operate, when reverse biased, as a variable capacitor providing attenuation of said superimposed signal in conjunction with said (second) resistor.

6. A gain-controlled amplifier circuit as claimed in any of the previous claims, wherein there is a first common-base transistor amplifier stage for connecting the collector electrode of said first transistor to a common load for said common emitter stages, and a second common-base amplifier stage for connecting the collector electrode of said second transistor to said output load, the said second transistor having smaller effective by-pass capacitance associated with its collector than said first transistor.

7. A gain controlled amplifier circuit as

* C L M S *

claimed in Claim 6, wherein said first and said second common-base transistor amplifier stages jointly employ a dual-emitter transistor.

8. A gain controlled amplifier circuit substantially as hereinbefore described with reference to amplifier 12 in Fig. 1 of the accompanying drawings.

9. A gain controlled amplifier circuit according to any preceding claim in combination with a delayed AGC circuit substantially as hereinbefore described with reference to portion 22 in Fig. 1 of the accompanying drawings.

10. A gain controlled amplifier circuit as claimed in any of claims 1—8 having keyed and delayed AGC provided substantially as hereinbefore described with reference to Fig. 1 of the accompanying drawings.

11. A gain controlled amplifier circuit as claimed in any preceding claim wherein said first (62) and second (66) transistors of said parallel stages are provided in an integrated circuit with relative characteristics substantially as hereinbefore described with reference to portions 62 and 66 of Fig. 2 of the accompanying drawings.

12. An integrated circuit gain controlled amplifier circuit substantially as hereinbefore described with reference to Figs. 1 and 2 together of the accompanying drawings.

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