STRESS OPTIMIZATION IN DUAL EMBEDDED EPITAXIALLY GROWN SEMICONDUCTOR PROCESSING

Abstract of the Disclosure

A method of manufacturing dual embedded semiconductor transistors is provided, the method including, depositing a first elongated nitride spacer over first and second transistors, depositing a first photoresist block on the nitride spacer above the first transistor, etching the first nitride spacer above the second transistor, etching a first recess, forming a first epitaxially grown semiconductor material in the first recess, depositing an elongated blocking oxide over the first and second transistors and first extension, depositing a second photoresist block above the second transistor and first extension, etching the blocking oxide and first nitride spacer above the first transistor, etching a second recess, forming a second epitaxially grown semiconductor material in the second recess, etching nitride caps from the first and second transistors, depositing a second elongated nitride, etching the second nitride spacer, and implanting deep sources and drains in the first and second transistors.

Fig. 23