METHOD TO PREVENT DIE ATTACH ADHESIVE CONTAMINATION IN STACKED CHIPS

TECHNICAL FIELD

This invention relates generally to integrated circuit semiconductor device assemblies. More particularly, the present invention relates to stacked arrangements for semiconductor dice in semiconductor device assemblies.

BACKGROUND

Semiconductor devices are increasingly used in portable electronic applications, necessitating the development of smaller, higher performance components. In conventional semiconductor manufacturing processes, a multitude of integrated circuit (IC) dice or semiconductor dice are typically fabricated at one time onto a wafer comprising a semiconducting substrate (e.g., silicon or gallium arsenide) through methods well known in the art. These semiconductor dice are then incorporated, in turn, into a system by mounting them on a carrier substrate, for example a printed circuit board, to interconnect with the rest of the elements of the system, many of which are also other semiconductor dice.

In recent years, semiconductor manufacturing technology has steadily progressed, resulting in ever increasing numbers of circuit elements placed on a single semiconductor die. Semiconductor wafers are now subjected to thinning processes, resulting in the removal of nearly all excess silicon from individual semiconductor die. To further decrease the size of the overall packaged system, printed circuit boards and other component supporting substrates are made as small as practicable. For still further increases in electronics density, recent innovations have turned to new ways to package semiconductor dice. One such innovation involves vertically stacking a plurality of horizontally disposed semiconductor dice to form a dense electronic package. By using such stacking arrangements, multiple semiconductor die can be attached to the system using the footprint area of a single semiconductor die. The resulting increases in density allow for faster signal propagation while providing lower overall device weight. Additionally, these "chip-on-chip or die-on-die" arrangements

can often be fabricated faster and more cheaply than by designing new integrated circuitry for substrates.

The lack of available "real estate" on smaller circuit boards makes the stacking of semiconductor dice particularly desirable. One type of stacking arrangement, wherein several bare semiconductor dice used for the same or different functions are mounted in a common package, is known as a multi-chip module (MCM). MCMs generally contain a plurality of semiconductor dice in a dense arrangement where they are packaged together in a supporting substrate that can be hermetically sealed. Although prior art MCMs typically have a number of individual semiconductor die mounted within the package in a laterally adjacent manner, the vertical stacking of semiconductor dice is increasingly gaining acceptance.

Many types of semiconductor dice can be used to form MCM chip-on-chip or die-on-die stacks, including dynamic random access memory (DRAM), static random access memory (SRAM) and FLASH memory chips, as well as semiconductor dice having other types of functions such as analog to digital convertor (ADC) semiconductor dice, microprocessors, and field programmable gate arrays (FPGAs). Typically, the stacked semiconductor dice have electrical contacts which are coupled in common or in parallel to contacts on the substrate board.

In early MCM stacking arrangements, single stacks of semiconductor dice were generally made using semiconductor dice having substantially equal dimensions. For example, in United States Patent 5,323,060, assigned to the assignee of the present application, a plurality of identical, vertically-stacked semiconductor dice are disclosed with a relatively thick adhesive layer interposed therebetween. The active circuitry of the horizontally disposed semiconductor dice are shown facing upward, with wirebonds from each semiconductor die extending downwardly from the active surface to contact pads onto a multi-chip module substrate.

In the case of memory semiconductor dice, vertical stacking proves particularly advantageous since a plurality of semiconductor dice could be used to multiply the amount of memory available. Illustrative of the prior state of the art in this regard is "*Laminated Memory: A new 3-Dimensional Packaging Technology for MCM*", *Proceedings of* 1994 *IEEE Multi-Chip Module Conference*, pp. 58-63.

More recently, single stacks have been made comprised of semiconductor dice of different sizes and/or functions directly attached to one another. Generally, one or more semiconductor die are bonded on top of a larger semiconductor die, although larger semiconductor die have been placed on smaller semiconductor die using various ball grid array connections and various interposers as shown in United States Patents 5,977,640 and 5,790,384, respectively.

Numerous packaging alternatives for stacked dice are found in the art. In United States Patent 5,777,345, an integrated circuit package is disclosed wherein a first semiconductor die (a microprocessor) is attached to a die paddle of a lead frame, and a second smaller semiconductor die (a memory chip) is directly attached to the upwardly facing active surface of the first semiconductor die. The bonding pads of the semiconductor dice are shown to be connected to each other, and to the lead frame, by a wire bonding process.

United States Patent 5,998,864 discloses horizontally disposed bare semiconductor dice stacked atop one another in offset fashion such that an edge portion of each semiconductor die is exposed. On the edge portions of each semiconductor die are terminals (bond pads) for interconnection of the semiconductor dice to an interconnection substrate.

United States Patent 6,005,778 shows semiconductor die stacking arrangements wherein a planar silicon spacer with a conductive surface and upwardly facing bond pads is mounted between two semiconductor die on a substrate carrier. The planar conductive spacer is shown with two configurations. In a first configuration, the intermediately disposed spacer has a two-tiered portion at its lateral edges, with bond pads exposed on the lower of the two tiers. The spacer is further provided with lesser horizontal dimensions than the first semiconductor die, such that the two lateral edges of the first semiconductor die, containing bond pads for wire bonding to the substrate, remain exposed after the spacer is adhesively affixed to the first semiconductor die. In a second embodiment, the planar spacer has a larger footprint than the horizontally disposed semiconductor dice used in the assembly. The spacer is placed intermediate to the two smaller semiconductor dice such that lateral edge upper surface areas of the spacer, containing bond pads and wire bonds, extend beyond the footprints of both semiconductor dice. The second semiconductor die, also containing wire bonds on its

upper surface lateral edges, is bonded to the spacer by an adhesive layer, leaving the bonding pads and wire bonds of the spacer exposed.

In these types of stacked semiconductor die arrangements, the semiconductor dice are typically bonded to each other, or to intermediately disposed spacers/interposers, by means of an adhesive layer. Typically, bare semiconductor die are attached to such substrates using organic-based adhesives. The adhesive layer is typically dispensed by automatically by screen printing, a stamping device, or by a needle or syringe, in a non-cured state (soft phase), and is deposited between in a predetermined area designated for the mounting of the semiconductor die (i.e., the die attach area). Meanwhile, the semiconductor die to be mounted is then typically picked up and held by an automated vacuum mechanism, or other apparatus, of a die bonding machine. The semiconductor die is then positioned over the center of the die attach area, and is pressed into the previously deposited adhesive, ideally forming a uniform layer of adhesive under the semiconductor die. Usually, the adhesive layer is thereafter brought to its cured phase through exposure to elevated temperatures for a specified time period.

In many adhesive compositions, the carrier material, which provides the adhesion and mechanical strength in the bond line, is a polyimide or an epoxy resin. The carrier can be filled with metal particles in the event electrical and thermal conductivity is required. Alternatively, the carrier can be filled with non-metallic particles, such as alumina, if the final bond is to act an insulator.

One problem associated with the application of die attach adhesives is that an amount of a particular adhesive must be satisfactorily dispensed in a particular thickness and over a particular area which will provide sufficient bond integrity for the application, while simultaneously being free from voids. Voids are a problem for several reasons. First, if a void appears directly under an active part of a power circuit, the junction temperature may rise significantly since there is no material available to pull away the heat. Second, and more obviously, voids can affect the quality and mechanical strength of the die attach itself. Thus, the distribution of voids across the adhesive bonding layer is important in determining the effects which they will have. Small, random voids have only a modest effect on the thermal performance and mechanical integrity of the attach. Large, contiguous voids, however, can be

catastrophic to both thermal and mechanical performance. Voids can also serve as sites for moisture to collect during storage. This is especially problematic in plastic packages since this moisture can spread to critical interfaces and cause delaminations and package cracking. Care must be taken therefore, to ensure a sufficient amount of a properly viscous adhesive is applied to the die attach site so that void formation is minimized.

A related problem is that the adhesive, when dispensed, may overflow the site for semiconductor die or spacer/interposer attachment, or the adhesive may be squeezed out too far when the semiconductor die or spacer/interposer to be mounted is pressed into it. In the situation of vertically stacked semiconductor dice, this overflow or excess of adhesive can lead to the contamination of nearby bond pads, consequently interfering with subsequent wire bond operations, or even resulting in the loss of the function of the semiconductor die.

An associated phenomenon pertains to the use of conductive silver filled epoxies for the bonding of silicon semiconductor dice, a well-established procedure in the microelectronics industry. One of the problems that has plagued the industry in the past is the separation or "bleeding out" of the resin vehicle from the epoxy. In some cases, this resin bleed is severe enough to interfere with subsequent wire bonding and lid sealing operations by disadvantageously coating the surfaces with a thin film of the resin material.

The rheology (also referred to as viscosity) of adhesives is therefore a property which is critical to proper die attach processes. Viscosity can be a difficult property to control, and may be affected by even small changes in the ambient temperature. Different application methods for adhesive also have different viscosity ranges. For example, viscosity ranges typical for dispensing are from about 20,000 to about 60,000 centipois (cps), from about 8,000 to about 20,000 cps for stamping, and from about 30,000 to about 100,000 cps for screen printing.

Therefore, when attaching vertically stacked semiconductor dice, it would be advantageous to develop a method and assembly for preventing adhesive overflow which can potentially lead to bond pad contamination. Such a method and assembly should ideally be simple, inexpensive, and compatible with widely-practiced means of fabricating stacked semiconductor dice package assemblies. Additionally advantageous

would be a method which allows for relaxed requirements for die attach materials and process controls.

DISCLOSURE OF INVENTION

The present invention relates to a method and assembly for preventing adhesive overflow contamination of bond pads during the attachment of stacked semiconductor dice. The method and assembly comprise building or placing an adhesive flow control dam positioned between an adhesive application area and electrical contacts on an upper surface of a first semiconductor die. A second semiconductor die or other substrate is mounted (i.e., stacked) onto the adhesive application area of the first semiconductor die. In accordance with the invention, the adhesive flow control dam is rendered of a sufficient height and shape to block applied adhesive from flowing over the electrical contacts of the first semiconductor die when the second substrate is mounted onto the upper surface of the first semiconductor die. The mounting surface of the semiconductor die stack may be supplied with a thermally and/or electrically conductive adhesive, which holds the stack together in addition to allowing for heat dissipation and providing the necessary electrical interconnection between mounted chips, respectively. The semiconductor die stack may also be mounted on carrier substrate.

In another embodiment, two stacked semiconductor dice may be separated by a semiconducting interposer or other substrate. The interposer is adhesively attached to the upper surface of the first semiconductor die, while a second semiconductor die is attached to the upper surface of the interposer. An adhesive flow control dam positioned in the region between the perimeter of the interposer and the electrical contacts or bond pads of the first semiconductor die prevents adhesive from flowing over the electrical contacts.

In another embodiment, the method of the present invention may be used when the two semiconductor dice are of the same or substantially similar size. The semiconductor dice can be mounted in an offset fashion relative to one another, leaving the edge portions of the semiconductor dice containing electrical contacts exposed. An adhesive flow control dam is located on a first semiconductor die between the electrical contacts and the die attach site. In addition, the dice may be mounted directly

one above the other, wherein an adhesive flow control dam located on the terminal area portions of each semiconductor die is configured to deform when the mounting semiconductor die is pressed into it.

In another embodiment, the adhesive flow control dam can serve as a decoupling capacitor or a decoupling capacitor coupon. The decoupling capacitor coupon is electrically connected to the surface of the first semiconductor die to lower noise and to improve inductive impedance.

In a further embodiment, the dam of the present invention can be used to accumulate thermally conductive adhesive on a constrained region of the semiconductor die in addition to preventing overflow of adhesive onto the electrical bond pads. The thermally conductive adhesive provides increased thermal dissipation of heat from the semiconductor die.

Other features and advantages of the present invention will become apparent to those of skill in the art through a consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings, which illustrate what is currently considered to be the best mode for carrying out the invention:

FIG. 1 illustrates an example of a prior art stacked semiconductor die assembly;

FIG. 2*a* shows a stacked semiconductor die assembly with less than a sufficient amount of adhesive under the mounting semiconductor die, thus resulting in the undesirable formation of voids;

FIG. 2*b* illustrates a stacked semiconductor die assembly with the correct amount of adhesive applied under the mounting semiconductor die;

FIG. 2*c* illustrates a stacked die assembly wherein an excess of adhesive has been applied under a mounting semiconductor die;

FIG. 3 shows a side view of a stacked semiconductor die assembly which makes use of an adhesive flow control dam to prevent the flow of semiconductor die attach adhesive onto electrical contacts of a first semiconductor die;

FIG. 4 shows a side view of an embodiment of a stacked semiconductor die assembly wherein a semiconducting interposer is intermediately disposed between two semiconductor die;

FIG. 5*a* illustrates an embodiment of the present invention wherein an adhesive flow control dam may be used when semiconductor dice are stacked in an offset fashion relative to one another;

FIG. 5*b* illustrates an embodiment wherein a mounted semiconductor die is placed in contact with an adhesive flow control dam of the present invention;

FIG. 6 illustrates an adhesive flow control dam of the present invention used to prevent solder flow from wire bonding operations from contacting a mounted semiconductor device; and

FIG.7 illustrates an embodiment in which a thermally conductive adhesive is disposed adjacent an adhesive flow control dam for added heat dissipation.

BEST MODES FOR CARRYING OUT THE INVENTION

Illustrated in drawing FIG. 1 is an example of a vertically stacked integrated circuit semiconductor die package 10 contemplated for use in the method and assembly of the present invention. Package 10 comprises a first large semiconductor die 12 and a smaller semiconductor die 14 which are horizontally disposed upon a carrier substrate 20, the bare semiconductor dice mounted in a face-to back configuration relative to one another. Large semiconductor die 12 and smaller semiconductor die 14 are provided with wire bonding bond pads 16 exposed on two edges of an active surface 19 of both dice (only one edge is shown), and with wire bonds 18 extending to bond pads 22 on the carrier substrate 20. Bond pads 16 may also be configured as any of a variety of contact pads typically used for the electrical interconnection of substrates. Under the die attach area of smaller semiconductor die 14, an adhesive layer 13 is provided which serves to bond semiconductor die 12 and semiconductor die 14 together. The adhesive layer may be formed of any type die attach material known in the art, including polymers such as polyimides, polyamides, epoxies, cyanate esters, silicones and acrylics (including UV curable), as well as gels, pastes, solders, various other electrically or thermally conductive adhesives, and the like. Semifluid adhesives may be used, as well as fluid-like adhesives with relatively little resistance to

flow. Use of thermally and electrically conductive adhesives are preferable in some applications; a thermally conductive adhesive allows large semiconductor die 12 and smaller semiconductor die 14 to operate at substantially the same temperatures, while an electrically conductive adhesive allows the stacked dice to have the same ground potentials. Adhesive layer 13 can be deposited by any means known in the art, including, but not limited to, screen printing, stenciling, stamping device, rolled on, sprayed on, or by a needle or syringe. Preferably, adhesive layer 13 has a relatively high coefficient of thermal expansion and/or electrical conductivity to improve the thermal and/or electrical efficiency of package 10, depending on the particular application.

In the embodiment shown in drawing FIG. 1, the first semiconductor die 12 is a SRAM die while the second semiconductor die 14 is a FLASH memory die. The first semiconductor die 12, however, may be of any variety of semiconductor die known in the art, including, but not limited to: microprocessors, DRAM, SRAM, FLASH, ADC, FGPA, active pixel sensor (APS) operational amplifier (op AMP), etc.. The second semiconductor die 14 may also be of any variety known in the art, including a semiconductor die that serves the same or a similar function to that of semiconductor die 12, the only qualification of this embodiment being that second semiconductor die 14 is smaller than semiconductor die 12.

Illustrated in drawing FIGs. 2*a*, 2*b*, and 2*c* are a top views of smaller semiconductor die 14 mounted atop a larger semiconductor die 12 by means of a previously dispensed layer of adhesive 13. Larger semiconductor die 12 is configured with bond (or electrical contact) pads 16 on lateral edges. In drawing FIG. 2*a*, semiconductor die 14 is shown with less than a sufficient amount of adhesive thereunder, resulting in the undesirable formation of voids 19. Illustrated in drawing FIG. 2*b* is the correct amount of adhesive dispensed, while drawing FIG. 2*c* illustrates the application of too much adhesive. Above each figure is a top view of adhesive layer 13 shown as it would appear prior to the attachment of semiconductor die 14, the adhesive deposited in this case by a stamping tool. Illustrated in drawing FIG. 2*c*, is the deposit of adhesive where the deposit of adhesive is the same size as the semiconductor die, the mounting of a semiconductor die or substrate may cause adhesive material to be squeezed out sufficiently such that the adhesive 13 is forced outside the perimeter of the

semiconductor die and onto bond pads 16*a*, 16*b* of larger semiconductor die 12, the contamination potentially rending the bond pads unusable. As shown in drawing FIGs. 2*b* and 2*c*, adhesive 13 may also be forced from the perimeter edges of semiconductor die 14 and in the vicinity or onto bond pads 16, dependent upon the viscosity of the adhesive 13.

As shown in drawing FIG. 3, dam or barrier 30 (herein after referred to as dam 30) is provided or formed on an upper surface of semiconductor die 12. Dam 30, which is an adhesive flow control dam, is formed in situ or is manufactured and then pre-placed and adhered on large semiconductor die 12 prior to die attach. Dam 30 is positioned in a region on the upper die surface 19 between the area for die attach adhesive application and bond pads 16*a*. Dam 30 may be a polyimide, epoxy, polyamide or other type strip, as well as a cured liquid, or other type of physical barrier. When formed in situ, dam 30 may be formed on a wafer or a semiconductor die through any of a variety or combination of deposition techniques well known in the art, including sputtering, CVD, PVD, and photoimaging techniques. Dam 30 may also be pre-formed or formed in place by casting techniques. Dam 30 is configured with lateral dimensions and a predetermined height, shape, and viscosity so as to prevent the flow of adhesive material 13 onto bond pad 16*a* when semiconductor die 14 is mounted onto die 12. By preventing the flow of adhesive material 13 onto bond pads 16, the bond pads 16 are protected from "contamination" by the adhesive material, which could potentially render the bond pads unusable. It is understood that use of the term "contamination" refers to any contact of adhesive 13 to bondpads 16. It is contemplated that dam 30 may be placed in any location on semiconductor die 12 wherein the potential exists for adhesive overflow onto bond pads or other electrical structures of semiconductor die 12.

Illustrated in drawing FIG. 3 is an overflow 15 of adhesive material 13 of the kind the invention was designed to protect, resulting, for example, from the dispensing of a low viscosity adhesive, the inaccurate placement of adhesive, or from an excess of adhesive squeezed out from the die edges during the mounting of small semiconductor die 14 onto the die attach area of large semiconductor die 12. Once die attach has been accomplished using dam 30, stacked semiconductor dice assembly 10 may be encapsulated by means known in the art to protect assembly 10, as well as its related

interconnections, from moisture, contamination, etc. Dam 30 may remain in place during encapsulation. Alternatively, dam 30 can be removed prior the encapsulation process. Typically, encapsulant 50 is an electrically insulating material which prevents electrical shorting of bond pads 16 and wire bonds 18. In a preferred embodiment, dam 30 is made of a material which is the same, or substantially similar to, the material which forms encapsulant 50.

Illustrated in drawing FIG. 4 is an alternate embodiment of an assembly 10 wherein a semiconducting interposer 40 is intermediately disposed between two semiconductor die 12*a* and 12*b*. Interposer 40 is mounted onto an upper surface of first semiconductor die 12*a,* the upper surface of semiconductor die 12*a* containing bond pads at its lateral edges. A second semiconductor die12*b* having bond pads 16*b*, which is shown as smaller in size as semiconductor die 12*a,* is adhesively mounted on a top surface of interposer 40 by adhesive layer 13. Interposer 40, which preferably comprises a conductive substrate, is formed of dimensions less than the footprint of semiconductor die 12*a* such that bond pads 16 of semiconductor die 12*a* remain exposed. Interposer 40 is adhesively attached on top of semiconductor die 12*a* by a layer of adhesive 13 as described above. Dams 30 are shown positioned in the region between a perimeter edge of interposer 40 and bond pads 16 of semiconductor die 12*a* and bond pads 16*b* of semiconductor die 12*b* so as to block an overflow of adhesive 13 onto bond pads 16 and 16*b*.

It is also contemplated that dam 30 may be used when interposer 40 is formed as a semiconductor substrate with bond pads 32 disposed thereon. In this alternate embodiment, interposer 40 is intermediate to two stacked and horizontally disposed dice. As seen in drawing FIG. 4, interposer 40 is configured with a footprint larger than that of top die 14. A dam 30 is positioned in the region between a perimeter edge of semiconductor die 14 and bond pads 32 of interposer 40 such that die attach adhesive 13 does not overflow onto bond pads 32 during die attach processes.

Dam 30 can also be used when stacked dice are of the same or approximately the same size. As shown in drawing FIG. 5*a*, semiconductor dice 12*a* and *12b* are mounted in an offset fashion similar to or the same as that disclosed in United States Patent 5,998,884. In this configuration, bare semiconductor dice are stacked atop one another in offset fashion such that an edge portion of each semiconductor die,

containing bond pads 16, is exposed. A dam 30 can be formed between each of the semiconductor die attach sites and bond pads 16 to prevent contamination resulting from adhesive overflow.

In drawing FIG. 5*b*, semiconductor dice 12*a,* and 12*b,* of the same or similar size, are shown in a stacked arrangement, mounted directly above one another, with a relatively thick layer of adhesive placed therebetween. Such a stacked arrangement is described in United States Patent 5,323,060, assigned to the assignee of the present application. Dams 30, formed of a height, length, and other dimensions so as to effectively block the flow of the thick layer of adhesive 13, may be placed in the terminal area portions on lateral edges of each semiconductor die to prevent contamination of wire bonding pads 16. In a preferred embodiment of this arrangement, dams 30 are pre-formed on an upper surface of semiconductor dice 12*a* in a peaked shape. When semiconductor dice 12 are pressed together to form a vertically stacked package 10, peaked dams 30 are of a height and material so as to deform, thus providing support for the "overhang" regions of stacked dice arrangement to protect the dice against structural damage. As an additional advantage, peaked dams 30, when deformed by the mounting of semiconductor dice12, form a complete barrier to the passage of excess adhesive 13, consequently providing increased protective capacity and insulation for bond pads 16. As is apparent to one of ordinary skill in the art, the peaked dam structure of this embodiment has further application in other types of mounting arrangements, such as the interposer/die stack arrangement shown in drawing FIG. 4.

In another embodiment, dam 30 can be formed to serve an additional function as a decoupling capacitor or a decoupling capacitor coupon. A decoupling capacitor coupon dam 30*a*, as used herein, is defined as a relatively thin capacitive structure which is sufficiently thin so as to minimize any associated height increase to the semiconductor die to which it is mounted. Such a decoupling capacitor is the subject of United States Patent 5,982,018, assigned to the assignee of the present invention. Illustrated in drawing FIG. 6 is an example of a capacitor coupon 30*a* placed near a proximate edge region of larger semiconductor die 12 such that it also functions as a dam 30, preventing die attach adhesive 13, used for the attachment of smaller semiconductor die 14, from contaminating bond pads 16 on larger semiconductor die

12. Decoupling capacitor 30*a* is electrically connected to the active surface of semiconductor die 12 (or other substrates) by conventional methods known in the art. The coupon 30*a* comprises at least two electrode plates 30*b* with a dielectric film 30*c* disposed therebetween. Such coupons are useful in lowering noise by providing a path to ground for high frequency signals, and when positioned in close proximity to a chip, demonstrate an improved inductive impedance. Capacitor coupons 30*a* may be preformed of layers of conductive foil and dielectric, such as a polyimide tape, and dispensed from a stack or a reel for placement on a carrier substrate, in which case the coupon may be provided with a pre-placed adhesive (conductive or non-conductive, as required) for affixation of each coupon to a semiconducting substrate or die in accordance with the uses specified by the present invention. Alternatively, capacitor coupons 30*a* may be formed adjacent future die bond pad regions during fabrication of semiconductor dice on a wafer or other semiconductor substrates by deposition or application of the electrode and dielectric layers to the wafer prior to singulation of the dice therefrom. Preferably, the capacitor coupon dam 30*a* is used in combination with an insulating die attach adhesive 13. To prevent electrically shorting capacitor coupon dam 30*a*, die attach adhesive 13 should not be electrically conductive.

In addition to preventing bond pad contamination from die attach adhesive, use of dam 30 has several other distinct advantages. First, the protective aspect of dam 30 allows relaxed requirements for die attach materials and process controls. For example, lower viscosity adhesives can be used in the various dispensing operations. Additionally, the dispensing process controls need not be as precise, allowing for less expensive and higher throughput die attach procedures. Furthermore, in applications where tight tolerances between stacked chips are required, dam 30 may secondarily prevent the overflow of solder from bond pads 16 (during wire bonding or other operations) onto a surface or conductive extension of stacked semiconductor die 14, thus preventing electrical shorts. Illustrated in drawing FIG. 6 is this secondary preventive function of dam 30. In drawing FIG. 6, an excess of solder 60 is controlled from reaching surface areas or conductive extensions of semiconductor die 14 by the flow control properties of dam 30. Preferably, this embodiment entails rendering semiconductor die 30 from a material or composition of materials which have dielectric characteristics.

An additional advantage is realized when die attach adhesive 13 is thermally conductive. During their operation, chips dissipate electrical power as heat. Fluctuations in heat caused by the powering on and off of semiconductor dice are known to cause considerable mechanical stresses on semiconductor die interconnecting arrangements and mountings. Furthermore, where semiconductor dice are stacked one atop the other, it is difficult to dissipate the heat generated by the semiconductor dice in the middle of the stack. Thus, a design challenge for stacked semiconductor dice assemblies is to withstand thermal expansion during operation, and the substantial contraction that occurs when operation ceases. Moreover, there has been a need for semiconductor dice assemblies which provide enhanced heat dissipation, particularly from semiconductor dice in the middle of a stack. Dam 30, when used in conjunction with a thermally conductive die attach adhesive, helps solve this problem.

As shown in drawing FIG. 7, thermally conductive adhesive 13*a* is suitably viscous and/or is placed onto and around the die attach area in such a manner so as to be in contact with, or to flow outwardly towards, dam 30, where it is restrained from contaminating the bond pads 16. The surface area provided by the overflow of thermally conductive adhesive 13*a* provides increased thermal dissipation of heat from semiconductor dice 12 and 14. In this embodiment, dam 30 may protect contamination of bond pads 16 or alternatively, may be used on the upper surface of a stacked semiconductor die wherein the upper surface does not contain bond pads, such as in stacked die arrangements with one or more BGA die, to allow for an accumulation of thermally conductive adhesive 13*a*. Preferably, thermally conductive adhesive 13*a* is comprised of an Ag-filled polymer. Other adhesive polymers are also contemplated for use, including non-electrically conductive polymers, such as alumina-filled polymers, in applications where bond pads 16 or other electrically conductive parts of vertically stacked assembly 10 are in danger of electrically shorting due to close proximity of thermally conductive adhesive 13*a*. In carrying out this embodiment, dam 30 may be formed of a predetermined height which is relatively taller than other dam embodiments disclosed by the present invention, the height configured to provide sufficient protection for bond pads 16 due to increased risk of contamination by an intentionally applied excess amount of thermally conductive adhesive 13*a*. In an alternative embodiment, a thermal gel is used as the thermally conductive adhesive 13*a*.

It will be appreciated by those skilled in the art that the embodiments herein described, while illustrating certain embodiments, are not intended to so limit the invention or the scope of the appended claims. For example, this invention, while being described with reference to a dam or barrier for the protection of adhesive contamination of bond pads during die attach, has applicability for the protection of other electrical components which may be attached to a semiconductor die, including traces, contact pads, solder balls, mounting recesses, electrical plugs, etc.. Those skilled in the art will also understand that various combinations or modifications of the preferred embodiments could be made without departing from the scope of the invention.

CLAIMS

What is claimed is:

1. A method for preventing adhesive contamination of at least one electrical contact during manufacturing of a stacked semiconductor die assembly, comprising:

providing a first semiconductor die, said first semiconductor die having an upper surface, said upper surface comprising at least one electrical contact and at least one region for mounting a second semiconductor die;

providing at least one adhesive flow control dam positioned between said at least one region for mounting a second semiconductor die and said at least one electrical contact;

applying an adhesive to at least a portion of said at least one region for mounting a second semiconductor die; and

mounting a second semiconductor die onto said at least one region for mounting a second semiconductor die of said first semiconductor die, said adhesive prevented from contacting said at least one electrical contact by said at least one adhesive flow control dam.

2. The method of claim 1, wherein said applying an adhesive comprises applying a thermally conductive adhesive.

3. The method of claim 2, wherein said applying an adhesive comprises applying an Ag-filled polymer.

4. The method of claim 1, wherein said applying an adhesive comprises applying an electrically conductive adhesive.

5. The method of claim 4, wherein said electrically conductive adhesive comprises alumina-filled polymers.

6. The method of claim 1, wherein said applying an adhesive comprises applying an adhesive having a coefficient of thermal expansion approximating a

coefficient of thermal expansion of one of a coefficient of thermal expansion of said first semiconductor die, a coefficient of thermal expansion of said second semiconductor die, and an average of the coefficients of thermal expansion of said first semiconductor die and said second semiconductor die.

7. The method of claim 1, wherein said applying an adhesive comprises applying an adhesive by one of screen printing, stenciling, stamping device, rolling on, spraying on, needle dispensed, and syringe dispensed.

8. The method of claim 1, wherein said applying an adhesive comprises applying an adhesive of one of polyimides adhesives, polyamides adhesives, epoxy adhesives, cyanate ester adhesives, silicone adhesives and acrylic adhesives.

9. The method of claim 1, wherein said applying an adhesive comprises applying an adhesive of one of gels, pastes, and solders.

10. The method of claim 1, wherein said providing at least one adhesive flow control dam comprises forming at least one adhesive flow control dam in situ on said first semiconductor die.

11. The method of claim 10, wherein said forming said at least one adhesive flow control dam in situ comprises forming at least one adhesive flow control dam by a method selected from the group consisting of sputtering, CVD, PVD and photoimaging techniques, or any combination of these techniques.

12. The method of claim 1, wherein said providing at least one adhesive flow control dam comprises forming at least one adhesive flow control dam by a casting technique and attaching said at least one adhesive flow control dam to said first semiconductor die.

13. The method of claim 1, wherein said providing at least one adhesive flow control dam comprises forming at least one adhesive flow control dam of a material of one of polyimides, polyamides, and epoxies.

14. The method of claim 1, wherein said providing at least one adhesive flow control dam comprises providing at least one adhesive flow control dam comprising a decoupling capacitor coupon.

15. The method of claim 1, wherein said providing a first semiconductor die comprises providing a first semiconductor die having a larger size than the size of said second semiconductor die.

16. The method of claim 1, wherein said providing a first semiconductor die comprises providing an integrated circuit semiconductor die.

17. The method of claim 1, wherein said mounting of said second semiconductor device comprises placing at least a portion of said second semiconductor die in contact with said at least one adhesive flow control dam.

18. The method of claim 17, wherein said placing at least a portion of said second semiconductor die in contact with said at least one adhesive flow control dam comprising pressing said at least a portion of said second semiconductor die against said at least one adhesive flow control dam, said at least one dam being deformable.

19. A method of manufacturing a stacked semiconductor die assembly comprising:

providing a first semiconductor die, said first semiconductor die having an upper surface, said upper surface comprising at least one electrical contact and at least one region for mounting a second semiconductor die;

providing at least one adhesive flow control dam positioned between said at least one region for mounting a second semiconductor die and said at least one electrical contact;

applying an adhesive to at least a portion of said at least one region for mounting a second semiconductor die; and

mounting a second semiconductor die onto said at least one region for mounting a second semiconductor die of said first semiconductor die, said adhesive prevented from contacting said at least one electrical contact by said at least one adhesive flow control dam.

20. The method of claim 19, wherein said applying an adhesive comprises applying a thermally conductive adhesive.

21. The method of claim 20, wherein said applying a thermally conductive adhesive comprises applying an Ag-filled polymer.

22. The method of claim 19, wherein said applying an adhesive comprises applying an electrically conductive adhesive.

23. The method of claim 22, wherein said electrically conductive adhesive comprises alumina-filled polymers.

24. The method of claim 19, wherein said applying an adhesive comprises applying an adhesive having a coefficient of thermal expansion approximating a coefficient of thermal expansion of one of a coefficient of thermal expansion of said first semiconductor die, a coefficient of thermal expansion of said second semiconductor die, and an average of the coefficients of thermal expansion of said first semiconductor die and said second semiconductor die.

25. The method of claim 19, wherein said applying an adhesive comprises applying an adhesive by a method of one of screen printing, stenciling, stamping device, rolling on, spraying on, needle dispensed, and syringe dispensed.

26. The method of claim 19, wherein said applying an adhesive comprises applying an adhesive of one of polyimide adhesives, epoxy adhesives, cyanate ester adhesives, silicone adhesives, and acrylic adhesives.

27. The method of claim 19, wherein said applying an adhesive comprises applying an adhesive of one of gels, pastes, and solders.

28. The method of claim 19, wherein said providing at least one adhesive flow control dam comprises forming at least one adhesive flow control dam in situ on said first semiconductor die.

29. The method of claim 28, wherein said forming said at least one adhesive flow control dam in situ comprises forming at least one adhesive flow control dam by a method selected from the group consisting of sputtering, CVD, PVD and photoimaging techniques, or any combination of these techniques.

30. The method of claim 19, wherein said providing at least one adhesive flow control dam comprises forming at least one adhesive flow control dam by a casting technique and attaching said at least one adhesive flow control dam to said first semiconductor die.

31. The method of claim 19, wherein said providing at least one adhesive flow control dam comprises forming at least one adhesive control dam of a material of one of polyimides, polyamides, and epoxies.

32. The method of claim 19, wherein said providing at least one adhesive flow control dam comprises providing at least one adhesive flow control dam comprising a decoupling capacitor coupon.

33. The method of claim 19, wherein said providing a first semiconductor device comprises providing a first semiconductor die having a larger size than the size of said second semiconductor die.

34. The method of claim 19, wherein said providing a first semiconductor die comprises providing an integrated circuit semiconductor die.

35. The method of claim 19, further comprising encapsulating at least a portion of a surface area of said first semiconductor die and said second semiconductor die.

36. The method of claim 35, wherein said encapuslating at least a portion of a surface area of said first semiconductor die and said second semiconductor die further comprises encapsulating said at adhesive flow control dam.

37. The method of claim 36, wherein said providing at least one adhesive flow control dam comprises forming said at least one adhesive flow control dam from a composition of materials substantially similar to the materials used for said encapsulating at least a portion of a surface area of said first semiconductor die and said second semiconductor die

38. The method of claim 35, further comprising removing said at least one adhesive flow control dam prior to said encapsulating.

39. The method of claim 19, wherein said applying an adhesive comprises applying said adhesive such that at least a portion of said adhesive is disposed adjacent said at least one adhesive flow control dam and outside said at least one region for mounting a second semiconductor die.

40. The method of claim 39, wherein said applying an adhesive comprises applying a thermally conductive adhesive.

41. The method of claim 19, wherein said mounting of said second semiconductor die comprises placing at least a portion of said second semiconductor die in contact with said at least one adhesive flow control dam.

42. The method of claim 41, wherein said placing at least a portion of said second semiconductor die in contact with said at least one adhesive flow control dam comprises pressing said at least a portion of said second semiconductor die against said at least one adhesive flow control dam, and wherein said providing at least one adhesive flow control dam comprises providing said at least one adhesive flow control dam which is deformable.

43. The method of claim 19, further comprising wire bonding said at least one electrical contact, and wherein said providing at least one adhesive flow control dam comprises configuring said at least one adhesive flow control dam for preventing solder flow onto at least a portion of said second semiconductor die or an extension thereof during said wire bonding.

44. A stacked semiconductor die assembly comprising:

a first semiconductor die, said first semiconductor die having an upper surface, said upper surface comprising at least one electrical contract and at least one region for mounting a second semiconductor die;

at least one adhesive flow control dam for preventing flow of an adhesive onto said at least one electrical contact during mounting of a second semiconductor die, said at least one adhesive flow control dam positioned on the upper surface of said first semiconductor die; and

a second semiconductor die, said second semiconductor die adhesively mounted onto said at least one region for mounting a second semiconductor die of said first semiconductor die.

45. The stacked semiconductor die assembly of claim 44, further comprising an encapsulant surrounding at least a portion of a surface area of said first semiconductor die and said second semiconductor die.

46. The stacked semiconductor die assembly of claim 44, further comprising a carrier substrate, said first semiconductor die being disposed on said carrier substrate.

47. The stacked semiconductor die assembly of 44, further comprising a mounting adhesive disposed on at least a portion of a region of said upper surface of said first semiconductor die, at least a portion of said mounting adhesive disposed between said at least one adhesive flow control dam and said second semiconductor die.

48. The stacked semiconductor die assembly of claim 47, wherein said mounting adhesive is configured to be thermally conductive having an exposed surface area being heat dissipative.

49. The stacked semiconductor die assembly of claim 48, wherein said mounting adhesive comprises an Ag-filled polymer.

50. The stacked semiconductor die assembly of claim 47, wherein said mounting adhesive is configured to have a coefficient of thermal expansion selected from the group consisting of a coefficient of thermal expansion of said first semiconductor die, a coefficient of thermal expansion of said second semiconductor die, and an average of the coefficients of thermal expansion of said first semiconductor die and said second semiconductor die.

51. The stacked semiconductor die assembly of claim 44, wherein said at least one adhesive flow control dam comprises at least one decoupling capacitor coupon.

52. The stacked semiconductor die assembly of claim 51, wherein an adhesive used to mount said second semiconducting includes an electrically insulating adhesive.

53. The stacked semiconductor die assembly of claim 44, wherein said at least one adhesive flow control dam comprises a material selected from the group consisting of polyimides, polyamides, and epoxies.

54. The stacked semiconductor die assembly of claim 44, wherein said first semiconductor die is larger than said second semiconductor die.

55. The stacked semiconductor die assembly of claim 44, wherein said first semiconductor die is substantially the same size as said second semiconductor die.

56. The stacked semiconductor die assembly of claim 44, wherein said first semiconductor die comprises an integrated circuit semiconductor die.

57. The stacked semiconductor die assembly of claim 44, wherein said second semiconductor die comprises an integrated circuit semiconductor die.

58. The stacked semiconductor die assembly of claim 56, wherein said integrated circuit semiconductor die is selected from the group consisting of microprocessors, DRAM, SRAM, FLASH, ADC, FGPA, active pixel sensor, and operation amplifier.

59. The stacked semiconductor die assembly of claim 57, wherein said integrated circuit semiconductor die is selected from the group consisting of microprocessors, DRAM, SRAM, FLASH, ADC, FGPA, active pixel sensor, and operation amplifier.

60. The stacked semiconductor die assembly of claim 44, wherein said second semiconductor die is mounted in an offset fashion relative to said first semiconductor die in one of a horizontal offset and a vertical offset.

61. The stacked semiconductor die assembly of claim 44, wherein said at least a portion of said second semiconductor die is in contact with said at least one adhesive flow control dam.

62. The stacked semiconductor die assembly of claim 61, wherein said at least one adhesive flow control dam is configured to deform upon said contact with said second semiconductor die.

63. The stacked semiconductor die assembly of claim 44, wherein said at least one adhesive flow control dam extends substantially across an entire width of said first semiconductor die.

64. The stacked semiconductor die assembly of claim 44, further comprising at least one wire bond extending from said at least one electrical contact.

65. The stacked semiconductor die assembly of claim 64, wherein said at least one adhesive flow control dam is further configured to prevent solder flow onto at least a portion of said second semiconductor die or an extension thereof during wire bonding of said at least one electrical contact.

66. A semiconductor die structure for use in a stacked semiconductor die assembly comprising:

a first semiconductor die, said first semiconductor die having an upper surface, said upper surface comprising at least one electrical contact and at least one region for mounting a second semiconductor die; and

at least one adhesive flow control dam positioned between said at least one region for mounting a second semiconductor die and said at least one electrical contact, wherein said at least one adhesive flow control dam is configured to prevent adhesive from contacting said at least one electrical contact during mounting of a second semiconductor die onto said at least one region for mounting a second semiconductor die.

67. The semiconductor die structure of claim 66, wherein said at least one adhesive flow control dam comprises a decoupling capacitor coupon.

68. The semiconductor die structure of claim 66, wherein said at least one adhesive flow control dam comprises a material selected from the group consisting of polyimides, polyamides, and epoxies.

69. The semiconductor die structure of claim 66, wherein said first semiconductor die comprises an integrated circuit semiconductor die.

70. The semiconductor die structure of claim 66, wherein said first semiconductor die and said second semiconductor die are each selected from the group consisting of microprocessors, DRAM, SRAM, FLASH, ADC, FGPA, active pixel sensor, and operation amplifier.

71. The semiconductor die structure of claim 66, wherein said at least one adhesive flow control dam extends substantially across an entire width of said first semiconductor die.

72. The semiconductor die structure of claim 66, wherein said at least one adhesive flow control dam is configured to deform upon contact by a second semiconductor die.