Fig. 1

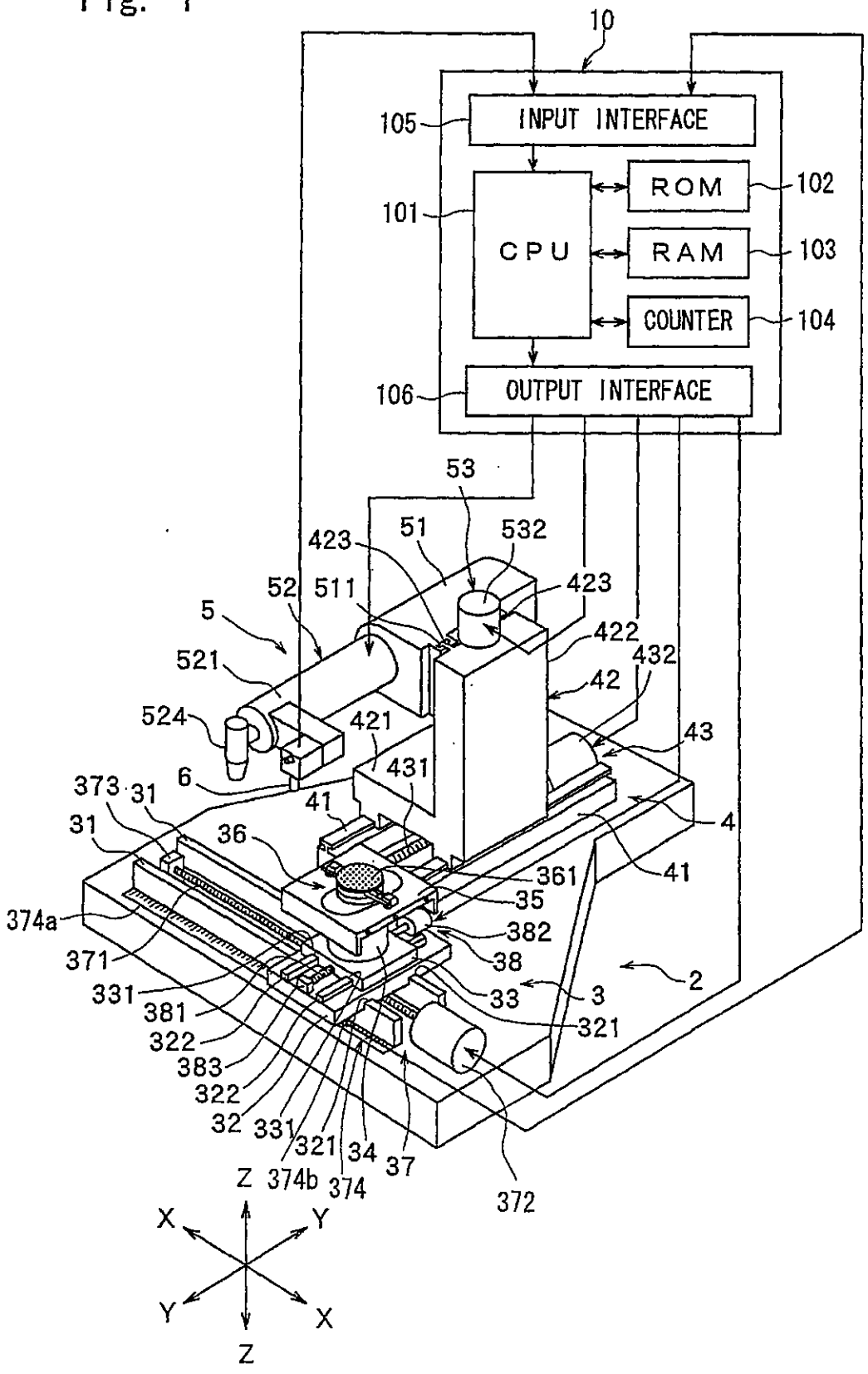

10
105
INPUT INTERFACE
101
CPU
ROM
102
RAM
103
COUNTER
104
106
OUTPUT INTERFACE
53
423
51
532
52
511
423
5
422
521
432
42
524
421
43
6
431
373
31
41
4
31
36
361
41
35
374a
382
371
38
2
331
33
3
381
321
322
383
322
32
331
321
34
37
Z
374b
374
372
X
Y
Y
X
Z

Fig. 2

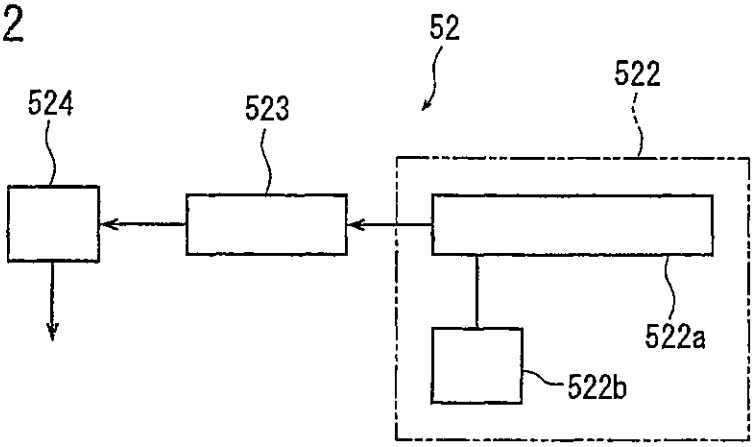


Fig. 3

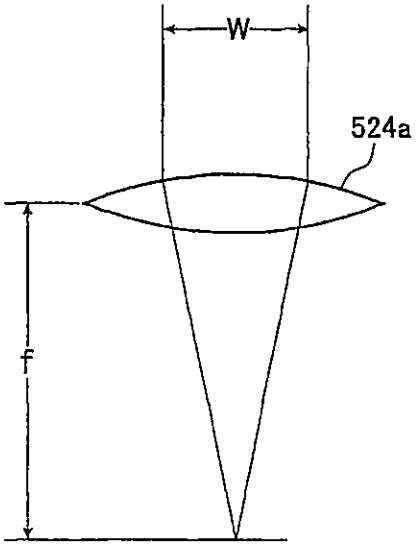


Fig. 4

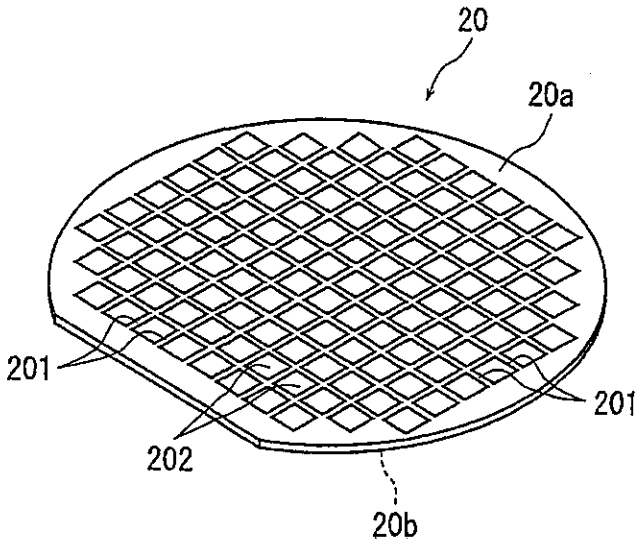


Fig. 5

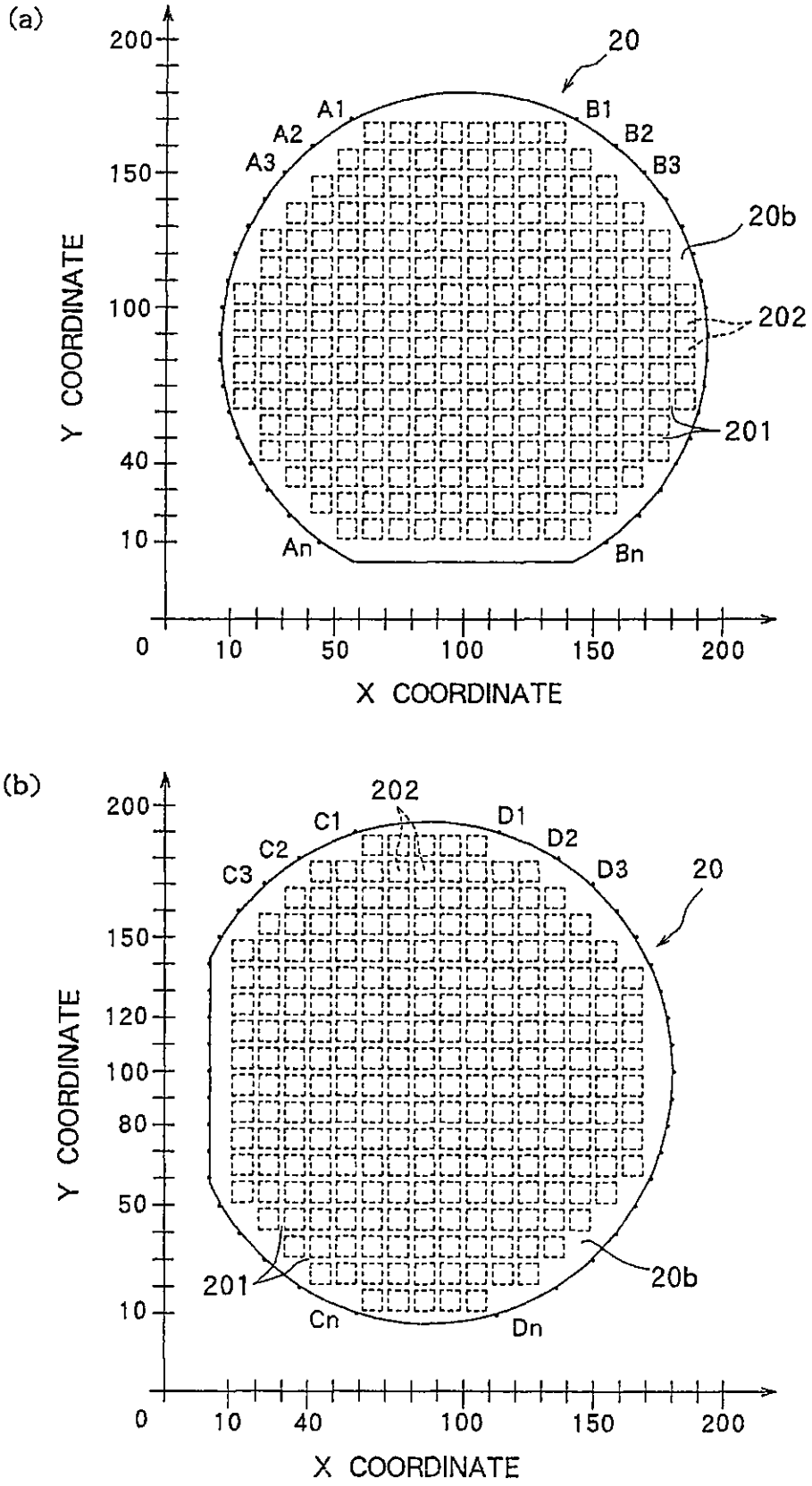

(a)
200
150
100
40
10
0
10
50
100
150
200
Y COORDINATE
X COORDINATE
20
A1
A2
A3
B1
B2
B3
20b
202
201
An
Bn
(b)
200
150
120
100
80
50
10
0
10
40
100
150
200
Y COORDINATE
X COORDINATE
202
C1
C2
C3
D1
D2
D3
20
201
20b
Cn
Dn

Fig. 6

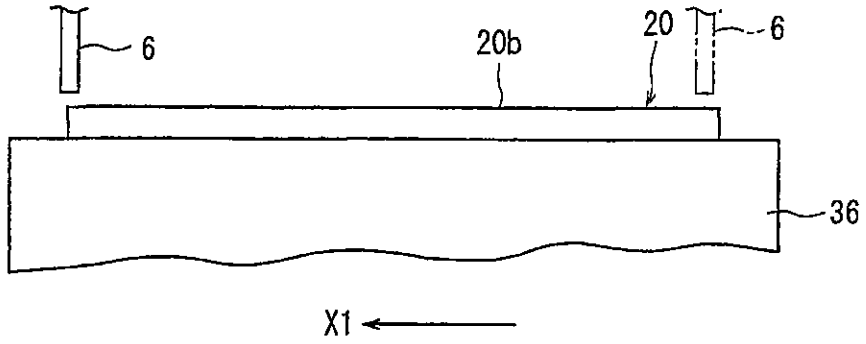
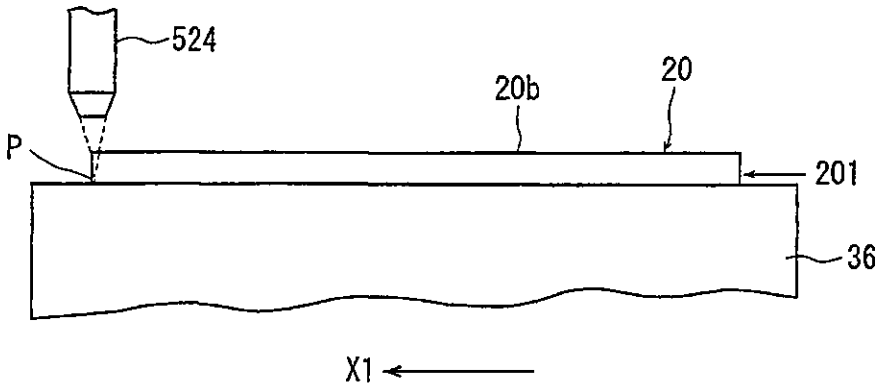


Fig. 7

(a)



(b)

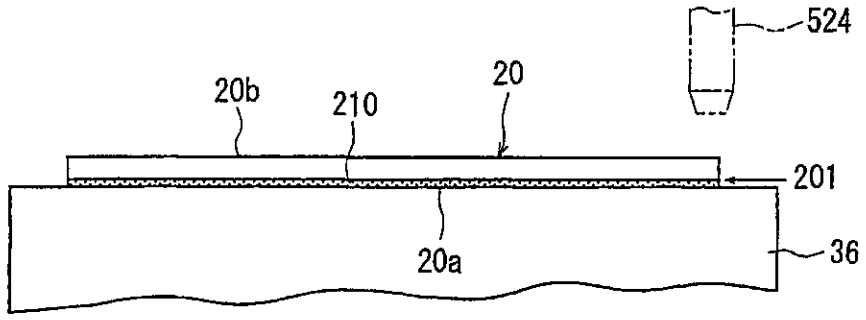


Fig. 8

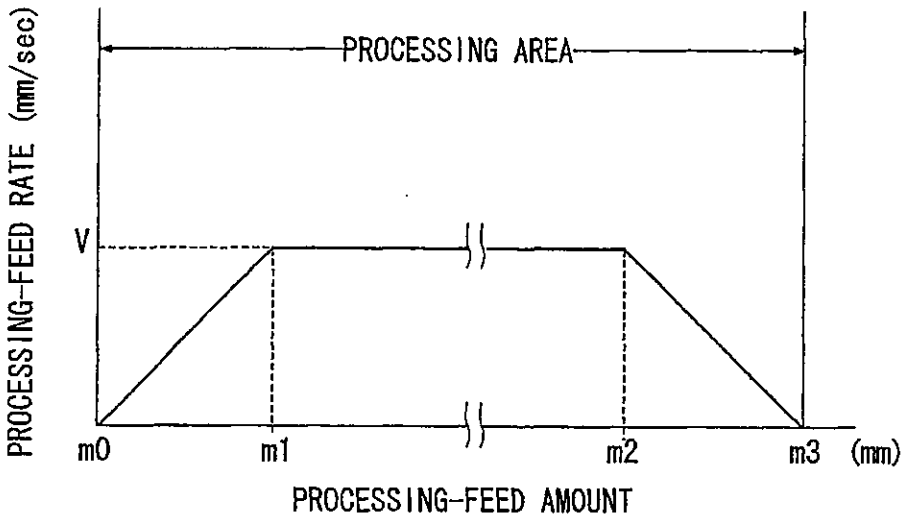

PROCESSING AREA
PROCESSING-FEED RATE (mm/sec)
V
m0
m1
m2
m3
(mm)
PROCESSING-FEED AMOUNT

Fig. 9

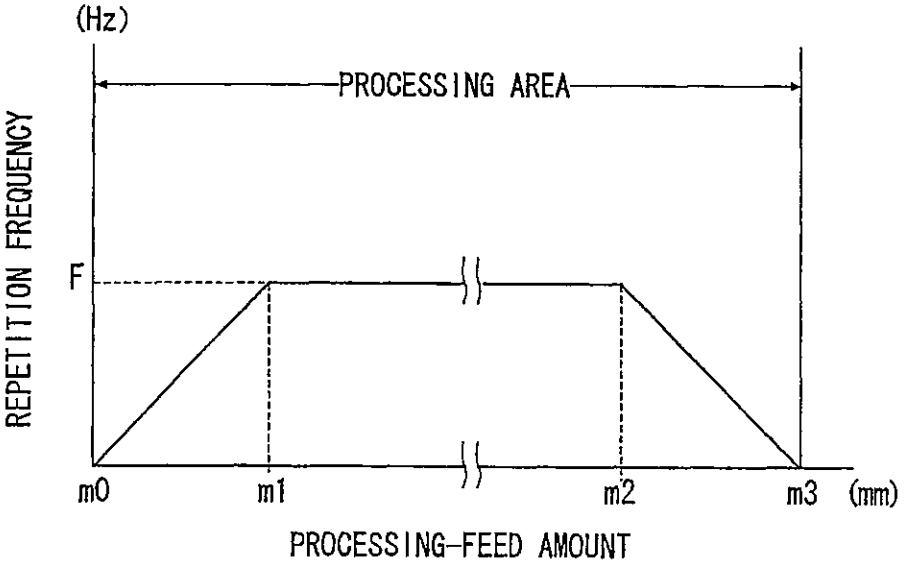

(Hz)
PROCESSING AREA
REPETITION FREQUENCY
F
m0
m1
m2
m3
(mm)
PROCESSING-FEED AMOUNT

Fig. 10

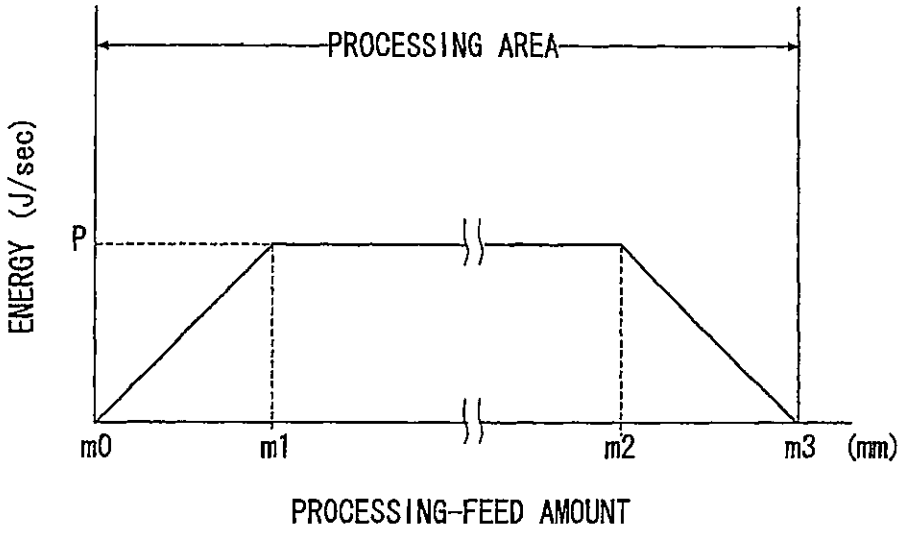
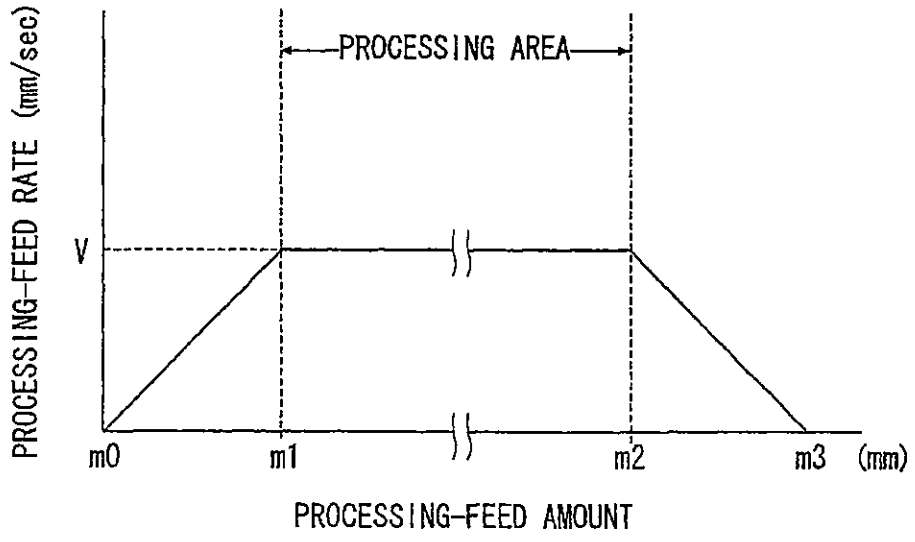

PROCESSING AREA
ENERGY (J/sec)
P
m0
m1
m2
m3
(mm)
PROCESSING-FEED AMOUNT

Fig. 11


PROCESSING AREA
PROCESSING-FEED RATE (mm/sec)
V
m0
m1
m2
m3
(mm)
PROCESSING-FEED AMOUNT