Integration for Buried Epitaxial Stressor

Abstract

Structures and methods of fabricating isolation regions for a semiconductor device. An example method comprises the following. We form one or more buried doped regions in a substrate. We form a stressor layer over the substrate. We form a strained layer over the stressor layer. We form STI trenches down through the strained layer and the stressor layer to as least partially expose the buried doped regions. We etch the buried doped regions to form at least a buried cavity in communication with the STI trenches. In the first and second embodiments, we fill only the STI trenches with insulation material to form isolation regions and form voids in the cavities. In the third and fourth embodiments, we fill both the STI trenches and the cavities with insulation material.

Figure 6A