

PATENT SPECIFICATION

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(54) AN IMPROVED CIRCUIT ARRANGEMENT FOR SUPPLYING CLOCK PULSES TO A PROJECTILE FUSE

(71) We, WERKZEUGMASCHINENFABRIK OERLIKON-BUHRLE AG a company organised and existing under the laws of Switzerland of Birchstrasse 155, CH-8050 Zurich, Switzerland, do hereby declare the invention for which we pray that a Patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

The present invention relates to a new and improved construction of circuit arrangement for supplying or delivering clock or timing pulses to a projectile fuse.

There are already known to the art such type devices which, however, do not afford the requisite accuracy with respect to maintaining a predetermined time-delay.

It is an object of the present invention to provide an improved circuit arrangement for delivering clock pulses to a projectile fuse in a manner not associated with the aforementioned drawbacks and limitations of the prior art proposals.

The present invention comprises a circuit arrangement for delivering clock pulses for a projectile fuse comprising circuitry containing an astable multivibrator and a supply capacitor for the voltage supply of the astable multivibrator, a resistor connected in circuit between the astable multivibrator and the supply capacitor, and a trimmer capacitor for stabilising the frequency of the clock pulses connected in parallel with said resistor.

Reference is now made to the accompanying drawings in which:

Figure 1 is a schematic circuit diagram of the entire apparatus of the invention for the supply of clock or timing pulses;

Figure 2 is a schematic circuit diagram of a multivibrator;

Figure 3 is a diagram showing the course of the periodic time as a function of supply voltage;

Figure 4 is a circuit diagram of a second exemplary embodiment of multivibrator; and

Figure 5 is a diagram showing curves of the voltage at different locations of the multivibrator.

Describing now the drawings, according to the circuit diagram of Figure 1 a multivibrator 10 having an output A₁ for the delivery of clock or timing pulses is connected via a parallel connected RC-element, i.e. a resistor 13 and a capacitor 22, with a supply capacitor 20. The supply capacitor 20 can be charged by a current generator 9 upon firing the projectile. The significance of the RC-element will be explained more fully herein-after. Current generator 9 may be a conventional component in this art and may comprise, for instance, an inductance coil, a permanent magnet and a soft iron core. During the firing acceleration of the projectile there occurs a relative displacement or shifting of these components for producing an induced current in the induction coil. Due to this induced current the supply capacitor 20 is charged.

Continuing, and turning to the circuit diagram of multivibrator as shown in Figure 2 it will be recognised that the same comprises four field-effect transistors 51, 52, 53 and 54. Each two respective ones of the field-effect transistors are connected in series, such as the field-effect transistors 51 and 52 and the field-effect transistors 53 and 54. The field-effect transistors (FET) 51, 52, 53 and 54 are connected with the current supply i.e. via the RC-element 13, 22 with the supply capacitor 20 and also with ground. The gates of the FET's 51, 52, 53, 54 are connected via the diodes 41, 43 with the current supply and via the diodes 42, 44 with ground. Both of the

FET's 51, 52 form a first inverter A and both of the FET's 53, 54 form a second inverter B. The output 4 of the inverter A, which at the same time constitutes the input of the inverter B, is connected via a resistor 11 and the junction point 2 with one terminal or side of a capacitor 21. The output 1 of the inverter B is connected with the other terminal or side of the capacitor 21. The input 3 of the inverter A is connected via a resistor 12 and the junction point 2 with the first terminal or side of the capacitor 21.

The FET's 51 and 53 are p-channel IGFET's or MOSFET's and the transistors 52 and 54 are n-channel transistors or MOSFET's. Consequently, upon application of a positive voltage to the inputs 3, 4 of both inverters A and B the p-channel transistors 51 and 53 are rendered non-conductive i.e. block, whereas the n-channel transistors 52 and 54 are conductive. On the other hand, if the voltage at the inputs 3, 4 of both of the inverters A and B drops to a predetermined value, then the operating state reverses, i.e. the p-channel transistors 51 and 53 become conductive and the n-channel transistors 52 and 54 become non-conductive i.e. block.

The voltage curve at the outputs 1 and 4 of both inverters B and A as well as at the input 3 of the inverter A will be apparent by referring to Figure 5.

The mode of operation of the above-described circuitry is as follows:

In the event that current flows through the FET's 52 and 53 and no current flows through the FET's 51 and 54, then there appears at the output 1 of the inverter B and at the input 3 of the inverter A the supply voltage U_{vers} , and at the input 4 there appears the ground voltage U_0 , as is apparent from the graphs of Figure 5 at the start of the oscillation time t_1 . The output 1 is connected in circuit via the FET 53 with the current supply and the input 4 is connected via the FET 52 with ground. Since the supply voltage U_{vers} appears at the output 1, the said one side of the capacitor 21 can be positively charged from the supply voltage U_{vers} . From the said other side of the capacitor 21 the charging current can flow via the resistor 11 and the FET 52, causing the voltage at the input 3 to drop according to an exponential curve, the time to switch being governed by the following equation:

EQUATION (1)

$$U_{UN} = (U_{VERS} + U_{UN}) e^{-t_1/RC}$$

In the above Equation (1) U_{un} represents the switching voltage for the inverters A, B the symbol R represents the resistances of the resistors 11 and 12, the symbol C the capacitance of the capacitor 21, and the symbol t_1 the time between two successive switching operations.

As soon as the voltage at the input 3 has dropped to the switching voltage, then both of the inverters A and B are switched. Current can now flow through the FET's 51 and 54, whereas current no longer flows through the FET's 52 and 53. The voltage at the output 1 thus drops to the voltage U_0 (ground). Via said one side or terminal the capacitor 21 can charge oppositely through the FET 54, current flowing to the said other side of the capacitor 21 via the FET 51 and the resistor 11. The voltage immediately reaches the value U_{vers} at the input 4. At the input 3 the voltage rises on an exponential curve, the time t_2 to switch being governed by the following equation:

EQUATION (2)

$$(U_{VERS} - U_{UN}) = (2U_{VERS} - U_{UN}) e^{-t_2/RC}$$

Since the oscillation period $T = t_1 + t_2$, there can be derived from the Equations (1) and (2) the following:

EQUATION (3)

$$T = t_1 + t_2 = -RC \left(\ln \frac{U_{UN}}{U_{VERS} + U_{UN}} + \ln \frac{U_{VERS} - U_{UN}}{2U_{VERS} - U_{UN}} \right)$$

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From this Equation it will be apparent that the oscillation period T is dependent upon the supply voltage U_{verr} . If there is provided a capacitor for the supply voltage U_{verr} , then it cannot be avoided that due to the removal of energy the voltage U_{verr} of the capacitor will drop, and consequently there will be a change in the oscillation period T .

The objective which should be realized with the present invention resides in the provision of a circuit arrangement wherein at least the mean or average oscillation period T_m should be constant during a predetermined time, for instance the time from the moment of firing a projectile until its detonation, amounting to for instance approximately 5 to 10 seconds. There should be taken into account that the supply capacitor 20 of the current supply is not always charged to the same output voltage. A numerical example should render this problem clearer. Assuming that the voltage U_{verr} to which the supply capacitor 20 has been charged can fluctuate by 10%, then it is required that the time until detonation of the projectile, for instance amounting to 5.3 seconds, is exactly maintained within 1% to 2%.

Now in order to solve this objective, according to Figure 1, an ohmic resistance 13 is connected between the multivibrator 10 and the supply capacitor 20, and further, there is connected in parallel with such ohmic resistance or resistor 13 a trimmer or balancing capacitor 22. The operation of such circuit configuration will be apparent from Figure 3. The supply voltage U_{verr} drops under the influence of the resistor 13. The course of such voltage brings about a change of the oscillation time according to curve a . The trimmer or balancing capacitor 22 brings about a correction according to the curve b ; from both of these curves a and b there results the curve c which represents the frequency and therefore the oscillation time T of the multivibrator 10.

The trimmer or balancing capacitor 22 is matched to the internal capacitance of the multivibrator 10, represented by broken lines in Figure 1 as the equivalent capacitance 23.

In order to further understand the invention reference will be made to individual characteristics of the multivibrator 10. The oscillation period T is dependent upon the performance of the FET's 51, 52, 53, 54. Upon reaching the switching threshold the FET's 51, 52, 53, 54 are rendered conductive, and specifically for such length of time until there is attained the required switching current I_D . This switching current I_D can be represented by the following Equation:

EQUATION (4)

$$I_D = \mu C_{ox} \frac{Z}{L} \left[(U_g - U_t) U_D - \frac{1}{2} U_D^2 \right]$$

In this Equation the following symbols have the following meaning:

U_g = gate voltage

U_t = threshold voltage

U_D = FET source-drain voltage

Z and L = dimensions of the FET (general width and general length)

C_{ox} = transistor capacitance.

From this Equation of the switching current a differential equation may be derived from which there will be apparent the dependency of the oscillation period T upon the supply voltage. Depending upon the size of the trimmer or balancing capacitor 22 and the internal capacitance 23 the oscillation period T can exponentially increase or decrease with increasing supply voltage U_{verr} .

After switching of the FET's there occurs the exponential discharge of the capacitor 21. This discharge time is shorter, when with higher supply voltage the switching voltage becomes smaller and the capacitor 21 is less intensely charged, than with lower supply voltage and relatively great switching voltage the capacitor 21 is more intensely charged.

By suitably tuning or matching the capacitances 21 and 22 there is possible a variation of the frequency as a function of the supply voltage in such a manner that apart from the properties of the employed complementary metal-oxide-semiconductor circuit (C-MOS) it is also possible to adjust the circuit construction in such a manner that over a certain range of the fundamental oscillations with a known size of the supply capacitor 20 there can be obtained a slow variation of frequency.

According to a modified exemplary embodiment as illustrated in the circuit arrangement of Figure 4 a respective ohmic resistance or resistor 60 is additionally arranged between both of the FET's 51, 52 and also between the FET's 53, 54, the function of which resistors 60 is analogous to the resistor 13. With these two resistors 60 it is possible, however, not only to choose their size i.e. resistance value, but also the tapping-off of the outputs 1 and 4 respectively.

WHAT WE CLAIM IS:—

1. A circuit arrangement for delivering clock pulses for a projectile fuse, comprising circuitry containing an astable multivibrator and a supply capacitor for the voltage supply of the astable multivibrator, a resistor connected in circuit between the astable multivibrator and the supply capacitor, and a trimmer capacitor for stabilising the frequency of the clock pulses connected in parallel with said resistor.

2. A circuit according to claim 1 in which the astable multivibrator is provided with field-effect transistors.

3. A circuit arrangement according to claim 2 where said field-effect transistors total at least four in number and additionally to said resistor connected in circuit between the astable multivibrator and the supply capacitor said multivibrator comprises two inverters containing said field-effect transistors, each inverter incorporating two field-effect transistors, and a respective resistor connected in circuit between the two field-effect transistors of each inverter.

4. A circuit arrangement for supplying clock pulses for a projectile fuse substantially as described herein with reference to the accompanying drawings.

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