BACKSIDE SEALING OF A SEMICONDUCTOR SUBSTRATE

INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0002] In semiconductor processing, auto-doping is a severe problem that occurs in epitaxial deposition processes. During this process, doped heteroatoms may diffuse out from the back of the substrate and migrate around the edge of the substrate, resulting in unintentional over-doping on the edge and frontside of the substrate. Current solutions for mitigating auto-doping include an extensive procedure that goes through various temperatures, processes, and substrate positions, involving a complicated procedure requiring repositioning (including flipping), resulting in high cost and low efficiency. A new solution using a tool for mitigating auto-doping that obviates much of the complication and even improves other aspects of using the tool would be desirable.

[0003] The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor implicitly admitted as prior art against the present disclosure.

SUMMARY

[0004] In one aspect of the present disclosure, an apparatus configured for backside sealing of a semiconductor substrate is disclosed. In some embodiments, the apparatus may include: one or more process chambers; a showerhead configured to deliver one or more process gases to a backside of the semiconductor substrate in at least one of the one or more process chambers; and a controller coupled to the showerhead and the one or more process chambers, and configured to: cause delivery of a first set of one or more process

gases to a first process chamber having the semiconductor substrate; apply a first process temperature of 200-400 °C in presence of plasma to form a layer of silicon oxide (SiO_2) on the backside of the semiconductor substrate; cause delivery of a second set of one or more process gases to the first process chamber; and apply the first process temperature of 200-400 °C in the presence of plasma to form a layer of amorphous silicon on the layer of SiO2 on the backside of the semiconductor substrate to collectively form a stack of materials that seals the backside of the semiconductor substrate and mitigates diffusion of dopants from the semiconductor substrate. In some implementations, the controller may be further configured to, subsequent to the formation of the layer of amorphous silicon, apply a second process temperature that is at least 700 °C to cause an annealing process to occur, the annealing process comprising causing crystallization of the layer of amorphous silicon to form a layer of polycrystalline silicon to collectively form a stack of materials that seals the backside of the semiconductor substrate.

[0005] In another aspect of the present disclosure, an apparatus is disclosed. In some embodiments, the apparatus may include: a first process chamber configured to receive a semiconductor substrate; a showerhead configured to deliver one or more process gases to a backside of the semiconductor substrate in the first process chamber; and a controller coupled to at least the showerhead and the first process chamber, and configured to: cause delivery of a first set of one or more process gases to the first process chamber having the semiconductor substrate; apply a first process temperature of 200-400 °C in presence of plasma to form a layer of amorphous silicon on the backside of the semiconductor substrate; cause delivery of a second set of one or more process gases to the first process chamber; and apply the first process temperature of 200-400 °C in the presence of plasma to form a layer of silicon oxide (SiO2) on the layer of amorphous silicon on the backside of the semiconductor substrate to collectively form a stack of materials that seals the backside of the semiconductor substrate and mitigates diffusion of dopants from the semiconductor substrate. In some implementations, the controller may be further configured to, subsequent to the formation of the layer of SiO2, apply a second process temperature that is at least 700 °C to cause an annealing process to occur, the annealing process comprising causing crystallization of the layer of amorphous silicon to form a layer of polycrystalline silicon to collectively form a stack of materials that seals the backside of the semiconductor substrate.

[0006] In another aspect of the present disclosure, a method for backside sealing of a

semiconductor substrate is disclosed. In some embodiments, the method may include: causing delivery of a first set of one or more process gases to a first process chamber of a deposition apparatus, the first process chamber having a semiconductor substrate disposed therein; applying a first process temperature in presence of plasma to form a first layer of material on the backside of the semiconductor substrate; causing delivery of a second set of one or more process gases to the first process chamber; and applying the first process temperature in the presence of plasma to form a second layer of material on the first layer of material on the backside of the semiconductor substrate to collectively form a stack of materials that seals the backside of the semiconductor substrate and mitigates diffusion of dopants from the semiconductor substrate. In some implementations, method may further include, subsequent to the formation of the second layer of material, applying a second process temperature to cause an annealing process to occur, the annealing process comprising causing crystallization of the first layer of material or the second layer of material to collectively form a stack of materials that seals the backside of the semiconductor substrate.

[0007] These and other features of the disclosed embodiments will be described in detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0008] FIGS. 1A and 1B illustrate example doping profiles in which an epitaxial process is being applied to a semiconductor substrate to cause epitaxial growth of a film.

[0009] FIG. 2 shows an example process flow of a conventional approach to depositing a backside sealing layer, without backside deposition.

[0010] FIG. 3 shows an example process flow of an approach to depositing a backside sealing layer, using backside deposition, according to some embodiments.

[0011] FIG. 4 depicts an example of an enhanced backside sealing layer formed over a surface of a semiconductor substrate, according to some embodiments.

[0012] FIG. 5 shows another example process flow of an approach to depositing a backside sealing layer, using backside deposition, according to some embodiments.

[0013] FIG. 6 is a flow diagram of an example of a method of backside sealing of a semiconductor substrate, according to some embodiments.

[0014] FIGS. 7 and 8 show block diagrams of example substrate processing systems, according to some embodiments herein.

[0015] FIG. 9A shows an example cross section of an edge of a shower-pedestal.

[0016] FIG. 9B shows a top view of an example carrier ring.

[0017] FIG. 10 is a diagram of a cross-sectional view of a processing system for depositing film on a backside of a semiconductor substrate, according to some embodiments herein.

[0018] FIG. 11 shows a schematic of an example process system that may be used to perform the methods described herein.

DETAILED DESCRIPTION

[0018] The following terms are used throughout the instant specification:

[0019] The terms "semiconductor wafer," "wafer," "substrate," "wafer substrate" and "partially fabricated integrated circuit" may be used interchangeably. Those of ordinary skill in the art understand that the term "partially fabricated integrated circuit" can refer to a semiconductor wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, 300 mm, or 450 mm. Examples of wafer materials include silicon (Si), gallium arsenide (GaAs), and silicon germanium (SiGe). Besides semiconductor wafers, other workpieces that may take advantage of the disclosed embodiments include various articles such as printed circuit boards, magnetic recording media, magnetic recording sensors, mirrors, optical elements, display devices or components such as backplanes for pixelated display devices, flat panel displays, micro-mechanical devices and the like. The workpiece may be of various shapes, sizes, and materials.

[0020] A "semiconductor device fabrication operation" as used herein is an operation performed during fabrication of semiconductor devices. Typically, the overall fabrication process includes multiple semiconductor device fabrication operations, each performed in its own semiconductor fabrication tool such as a plasma reactor, an electroplating cell, a chemical mechanical planarization tool, a wet etch tool, and the like. Categories of semiconductor device fabrication operations include subtractive processes, such as etch processes and planarization processes, and material additive processes, such as deposition

processes (e.g., physical vapor deposition, chemical vapor deposition, atomic layer deposition, electrochemical deposition, electroless deposition). In the context of etch processes, a substrate etch process includes processes that etch a mask layer or, more generally, processes that etch any layer of material previously deposited on and/or otherwise residing on a substrate surface. Such an etch process may etch a stack of layers in the substrate.

[0021] In the context of the present disclosure, "epitaxy" or "epitaxial" may refer to an approach to fabrication to create a crystalline layer on which to build a semiconductor device. An "epitaxial process," "epitaxial deposition process," or "epitaxial growth process" may refer to a process that includes forming layers (e.g., films) of material under a high temperature, and may be one example of the aforementioned semiconductor device fabrication operation.

[0022] "Manufacturing equipment" refers to equipment in which a manufacturing process takes place. Manufacturing equipment often has a process chamber in which the workpiece resides during processing. Typically, when in use, manufacturing equipment performs one or more semiconductor device fabrication operations. Examples of manufacturing equipment for semiconductor device fabrication include deposition reactors such as electroplating cells, physical vapor deposition reactors, chemical vapor deposition reactors, and atomic layer deposition reactors, and subtractive process reactors such as dry etch reactors (e.g., chemical and/or physical etch reactors), wet etch reactors, and ashers.

[0023] "Silicon oxide" is referred to herein as including any and all stoichiometric possibilities for Si_xO_y, including integer values of x and y and non-integer values of x and y. For example, "silicon oxide" includes compounds having the formula SiO_n, where $1 \leq n \leq 2$, where n can be an integer or non-integer values. "Silicon oxide" can include sub-stoichiometric compounds such as $SiO_{1.8}$. "Silicon oxide" also includes silicon dioxide (SiO_2) and silicon monoxide (SiO). "Silicon oxide" also includes both natural and synthetic variations and also includes any and all crystalline and molecular structures, including tetrahedral coordination of oxygen atoms surrounding a central silicon atom. "Silicon oxide" also includes amorphous silicon oxide and silicates.

[0024] In various approaches, materials in the stacks of layers (e.g., thin films) may be deposited through chemical vapor deposition (CVD) techniques such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD),

atmospheric pressure chemical vapor deposition (APCVD), metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), plasma enhanced atomic layer deposition (PEALD), or through direct metal deposition (DMD), etc. These examples are not intended to be limiting. Different deposition techniques may be used for different ends. For example, deposition may be useful whenever wafer stress and/or bowing are induced due to material present on the frontside of the wafer. Notably, different deposition techniques may be associated with or subject to different temperatures, pressures, precursors, or other deposition processes, conditions, or recipes. For instance, certain deposition techniques may overlap in temperatures ranges that can be used, which may advantageously be used to strategically deposit multiple layers at once or certain layers only.

[0025] A semiconductor substrate may be doped with elements (e.g., phosphorous atoms) to improve conductivity of the substrate. More specifically, conductivity of the silicon in a silicon-based wafer can be increased using such dopants. Many downstream applications or uses of the wafer can involve high temperatures, such as forming an epitaxial growth layer on the surface of the wafer. However, high temperatures can cause dopants to diffuse out of the wafer. This is a problem that the semiconductor industry is well aware of, known as "auto-doping."

[0026] One way to prevent dopants from being released is to deposit a backside sealing layer on the backside of the wafer. Commonly, a silicon-based film such as a silicon oxide (SiO_2), silicon nitride (SiN), or polysilicon film can be deposited to seal the backside of the wafer. However, the conventional process to achieve the deposition of a backside sealing layer is expensive, complex, lengthy, and inefficient. Particularly, multiple deposition techniques requiring different temperatures and orientations of the wafer (wafer backside facing down and up through the processes) increase the complexities and inefficiencies.

[0027] To solve this problem in conventional approaches, methods and apparatus for depositing an enhanced backside sealing layer directly on the backside of a wafer are herein described. These approaches do not require flipping of the wafer between different deposition techniques. In fact, the wafer may remain stationary in the processing environment (e.g., process chamber or station of a deposition apparatus). In some implementations, the enhanced backside sealing layer can include a stack of SiO_2 and amorphous silicon (a-Si), which can be formed in a single process using a deposition

apparatus configured for backside deposition, e.g., using PECVD at the same process temperature, as will be described in greater detail herein. This simplified approach advantageously reduces the cost and time involved, and increases the efficiency of providing a backside sealing layer to the wafer.

Wafer Backside Sealing

[0028] FIG. 1A illustrates an example doping profile 100 in which an epitaxial process is being applied to a semiconductor substrate 102 to cause epitaxial growth of a film 104. In some examples, the semiconductor substrate 102 may be a doped silicon-based wafer, and a film 104 may be formed or in the process of being formed on the frontside of the semiconductor substrate 102 as a result of an epitaxial deposition process. However, during this epitaxial deposition process, dopants 106 such as doped heteroatoms may diffuse out from the backside of the semiconductor substrate 102, from the surface opposite to the frontside. This diffusion may migrate along and affect the edge and bevel of the semiconductor substrate 102, resulting in unintentional over-doping 108 on the wafer edge and frontside, also known as auto-doping. Example doping profile 100 is thus a detrimental doping profile that requires backside sealing to mitigate the auto-doping, which is commonly performed before the epitaxial process.

[0029] To this end, in some approaches, a silicon-based film may be deposited on the backside of the semiconductor substrate 102. Examples of the silicon-based film may include silicon oxide (e.g., SiO_2), low temperature oxide (LTO, which SiO_2 can also refer to), silicon nitride (e.g., SiN), or polycrystalline silicon (also referred to as poly-Si, polysilicon, or semi-crystalline silicon). In addition, the deposited material can be a combination of different films, resulting in a stack of layers or materials. An example stack may be a stack of SiO_2 and poly-Si. The deposited film or stack can seal the dopants 106 in the semiconductor substrate 102 and prevent excessive diffusion and migration of the dopants 106.

[0030] FIG. 1B illustrates another example doping profile 120 in which an epitaxial process is being applied to a semiconductor substrate 102 to cause epitaxial growth of a film 104. In this example, a backside sealing layer 124 is deposited onto the backside of the semiconductor substrate 102. A stack of SiO_2 and poly-Si films deposited on the backside of semiconductor substrate 102 may be an example of the backside sealing layer

124. This mitigates the auto-doping problem by preventing diffusion and migration of the dopants 106.

[0031] However, current technology for depositing the backside sealing layer 124 is complex, costly, and inefficient. In one example of such current technology, shown in FIG. 2, a five-step process flow is required to deposit the backside sealing layer 124 to the backside.

[0032] FIG. 2 shows an example process flow 200 of a conventional approach to depositing a backside sealing layer, without backside deposition. At step 202, a semiconductor substrate 201 may be provided with its frontside facing upward. At step 204, the semiconductor substrate 201 may be flipped such that the frontside is facing downward. At step 206, a deposition process may be applied to the semiconductor substrate 201 to deposit a silicon oxide layer on the backside of the semiconductor substrate 201 from above (since the frontside is facing downward).

[0033] Returning to FIG. 2, an example of a deposition process that may be used at step 206 is APCVD and a silicon oxide precursor introduced at a uniform rate into an atmospheric pressure processing environment (e.g., process chamber), and application of a first process temperature (e.g., 250-400 °C) to the environment may result in deposition of a first layer. Another example of a deposition process that can be used at step 206 is PECVD with introduction of the silicon oxide precursor. The first layer may be a layer of silicon oxide (SiO_2) deposited on the backside of the semiconductor substrate 201, as illustrated in FIG. 2.

[0034] At step 208, another deposition process may occur to deposit a layer on both sides of the semiconductor substrate 201. For example, LPCVD may be used with a second process temperature (e.g., 600-700 °C) with a silicon-based precursor to deposit a layer of polysilicon (poly-Si) on the frontside and the backside.

[0035] At step 210, the semiconductor substrate 201 may be flipped again such that the frontside is back to facing upward again. At step 212, the frontside of the semiconductor substrate 201 may be polished to remove the layer of poly-Si from the frontside. Thus, the example process flow 200 can result in a wafer having a backside sealing layer, where the backside sealing layer includes a layer of silicon oxide and a layer of poly-Si. Having these two layers can improve the sealing capability of the backside sealing layer, as opposed to having one of the layers, although having one of the layers can also be acceptable under

some circumstances (e.g., when the epitaxial layer is not thick and fewer dopants diffuse out from the backside).

[0036] However, there are drawbacks to the above conventional approach. Such complicated procedures involving flipping and several steps require high cost and time and lead to low efficiency. Part of the complexity of the conventional approach is that depositing the two silicon oxide and poly-Si layers requires different process temperatures (e.g., 250-400 °C and 600-700 °C). Also, two different deposition tools are needed to deposit the two layers, which increases the complexity of the process flow, and its cost and process time. Moreover, the layer of poly-Si deposited via LPCVD can undergo excessive crystallization in any subsequent epitaxial steps at high process temperature (e.g., above 1000 °C), resulting in large grain size and a rough surface.

[0037] While the resulting backside sealing layer can mitigate auto-doping, it is clear that significant improvements can be made to reduce the complexity, reduce the costs, reduce the process time, and thereby increase efficiency. The techniques and apparatus described below can improve each of these issues. Moreover, different types of layers can be deposited (beyond SiO_2 and poly-Si) in different configurations to prevent some of the problems mentioned above.

[0038] FIG. 3 shows an example process flow 300 of an approach to depositing a backside sealing layer, using backside deposition, according to some embodiments. At step 302, a semiconductor substrate 301 may be provided with its frontside facing upward.

[0039] At step 304, a deposition process may be applied to the semiconductor substrate 301 without flipping the semiconductor substrate 301. In some embodiments, the deposition process may include PECVD using a backside deposition apparatus (described below). This obviates the need to flip or otherwise move the semiconductor substrate 301, as it allows deposition of one or more layers directly to the backside of the semiconductor substrate 301.

[0040] In some approaches, the deposition process may include two consecutive deposition steps. In a first deposition step, a first layer 312 may be deposited on the backside of the semiconductor substrate 301 in an environment suited for PECVD (e.g., a process chamber of the backside deposition apparatus). In some examples, the first layer 312 may include a silicon oxide (SiO_2) film. This deposition step may involve a lower process temperature (e.g., 200-400 °C) compared to that used in LPCVD, applied to a set

of first process gases (reactant gases, e.g., silane gas (SiH_4) and nitrous oxide gas (N_2O)) and plasma introduced to the environment to form a SiO_2 film.

[0041] In a second deposition step, subsequent to the deposition of the first layer 312 and while the frontside is still facing upward, a second layer 314 may be deposited on the backside of the semiconductor substrate 301, directly over the first layer 312. The second deposition step may occur immediately or substantially immediately after the first deposition step (e.g., within 5 seconds). This deposition step may involve the same process temperature as that of the first deposition step (e.g., 200-400 °C), and a carrier gas and plasma introduced to the environment. In some examples, the second layer 314 may include a high-quality amorphous silicon (a-Si) film. The SiO_2 film and the a-Si film may each have a prescribed thickness. For instance, the SiO_2 film may have a thickness of 3000-5000 angstroms (Å), and the a-Si film may have a thickness of up to 12000 Å. In some implementations, either or both of the SiO_2 film and the a-Si film may have a thickness of up to 20000 Å. For the formation of a-Si, the chemical reaction involves decomposition of SiH_4, so only the carrier gas may be introduced, with no other process gases or reactant gases. The carrier gas used in the second deposition step may be an inert gas, e.g., argon (Ar), nitrogen (N_2), or helium (He).

[0042] In some embodiments, deposition of the second layer 314 may result in an enhanced backside sealing layer 320 on the backside of the semiconductor substrate 301 without any movement of the semiconductor substrate 301 during the formation of the enhanced backside sealing layer 320. The enhanced backside sealing layer 320 may thus include a SiO_2 + a-Si stack.

[0043] While the above is described in terms of first and second deposition steps for reference, it will be understood that these steps are part of a single process to produce two layers or films. That is, the process temperature may be kept constant (at, e.g., 200-400 °C), and the substrate may be kept immobile, with the only change in the process conditions being the switch in reactant gases to form the two layers on the backside of the substrate. As will be described below with respect to FIG. 5, reactant gases can be changed to modify the order of layers formed on the backside of the substrate.

[0044] Herein lies one salient advantage of the present disclosure. The two deposition steps for producing the bilayer of silicon oxide (SiO_2) and a-Si may be performed in the same environment or process chamber and at the same process temperature without

breaking the vacuum, or transferring out or otherwise moving the semiconductor substrate 301. Only a change in process gases between deposition steps is needed. No flipping is required as with the conventional approach, such as the example process flow 200 of FIG. 2, since the depositions are performed directly on the backside of the wafer, without any frontside deposition occurring nor any removal or polish of the frontside being needed or performed. In addition, there is good adhesion between the silicon oxide and a-Si layers, which can prevent peeling or flaking of the a-Si film, which may be relatively thicker than the silicon oxide film in some cases.

[0045] Additional advantages and use applications include, for example, cases in which a-Si may be used as a conductive layer to improve wafer chucking, e.g., electrostatic chucking. In some cases, the bilayer may serve as an opaque and conductive backside layer, e.g., for glass wafer processing for devices and products, including user devices and wearable devices, such as those implementing displays for extended reality (XR) (e.g., augmented reality (AR), virtual reality (VR), mixed reality (MR)). Hence, deposition of a-Si on the semiconductor substrate 301 can be useful for enabling transparent glass wafer processing on wafer processing equipment (including that configured to perform CVD deposition, physical vapor deposition (PVD), or etching), and further stabilizing or immobilizing it within the environment, e.g., on a pedestal of the process chamber.

[0046] In some optional approaches, an annealing process may be performed at step 306. The annealing process may be optional because the second layer 314 (e.g., a-Si film) alone can provide the desired results, e.g., backside sealing and mitigation of auto-doping. In some embodiments involving an annealing process, the annealing may occur at a different temperature than that used for deposition steps, e.g., above 700 °C (e.g., 700-1100 °C). That is, the semiconductor substrate 301 having the first layer 312 and the second layer 314 may be exposed to the high temperature (e.g., 700-1100 °C) and allowed to cool over time. Annealing may be performed in a different environment or process chamber. By this annealing process, the second layer 314 (e.g., a-Si film) may undergo crystallization and transition to a different material. In some examples, a resulting crystallized layer 316 (e.g., a poly-Si film) may be formed over the SiO_2 film, forming an enhanced backside sealing layer 320' on the backside of the semiconductor substrate 301 without any movement of the semiconductor substrate 301 during the formation of the enhanced backside sealing layer 320'. The enhanced backside sealing layer 320' may thus include a SiO_2 + poly-Si stack. The poly-Si film may have a smaller grain size and a smoother surface than in the

conventional approach, such as the example process flow 200 of FIG. 2, which is another advantage of the present disclosure. It is generally desirable in wafer processing that the surface has a smooth surface rather than a rough surface, as otherwise, wafer chucking on other tools and downstream processes (including lithography and etch processes) may be impacted.

[0047] Thus, the bilayer structure of the enhanced backside sealing layer 320 or 320' on the semiconductor substrate 301 may include either: (i) the first layer 312 (e.g., SiO_2 film) and the second layer 314 (e.g., a-Si film) without any further annealing or epitaxial processes, or (ii) the first layer 312 (e.g., SiO_2 film) and a crystallized layer 316 produced by annealing (e.g., poly-Si film).

[0048] Referring briefly to FIG. 4, an example of an enhanced backside sealing layer 400 formed over a surface of a semiconductor substrate 401 is depicted according to some embodiments. According to the single-process deposition approach described above with respect to step 304, a first layer of material (e.g., SiO_2 film 404) may be deposited onto the surface of the semiconductor substrate 401, and a second layer of material (e.g., a-Si film 406) may be deposited onto the first layer of material. The SiO_2 film 404 may have a thickness T_1 (e.g., 4500 Å in this example, which is within aforementioned parameters) that is less than a thickness T_2 of the a-Si (e.g., 10000 Å in this example, which is within aforementioned parameters). However, among the functions of the SiO_2 film 404 includes promotion of adhesion of a-Si to the semiconductor substrate 401. Hence, the thicker T_2 does not create an issue of peeling or flaking of the a-Si film 406. The SiO_2 film 404 may further block dopants from escaping or diffusing from the semiconductor substrate 401, and increase the stability of the a-Si film 406 during high temperature processes by absorbing released hydrogen from the a-Si. Moreover, the outer surface 408 of the a-Si film 406 produced according to disclosed embodiments after annealing is smoother (due to a smaller grain size) compared to poly-Si produced using LPCVD in the conventional approach.

[0049] Further optionally, subsequent to the annealing process of step 306, other processes may be performed, such as (i) removing the semiconductor substrate 301 having the enhanced backside sealing layer 320, (ii) downstream processes relating to the environment (e.g., process chamber), such as process diagnostics, process control, chamber clean, hazard purge, gas purge (e.g., of N_2, from the process chamber), or (iii) collection of data relating to the semiconductor substrate 301 and/or the environment via

one or more sensors such as a spatial sensor (e.g., camera), a spectral sensor (e.g., optical emission spectrometry (OES) sensor), and/or a temporal sensor (e.g., photodiode).

[0050] Moreover, the above process can be performed concurrently on multiple semiconductor substrates in a single process chamber or multiple process chambers of a multi-chamber deposition apparatus, which is further described below.

[0051] In some embodiments, however, the first layer 312 may include a-Si, and the second layer 314 may include SiO_2. That is to say, the material of the first layer 312 and the second layer 314 may be flipped instead of what is shown in FIG. 3.

[0052] FIG. 5 shows another example process flow 500 of an approach to depositing a backside sealing layer, using backside deposition, according to some embodiments. Here, the process begins with step 502, in which a semiconductor substrate 501 is provided with its frontside facing upward, similar to step 302.

[0053] At step 504, a deposition process may be applied to the semiconductor substrate 501 without flipping the semiconductor substrate 501. In some embodiments, the deposition process may include PECVD using a backside deposition apparatus (described below). This obviates the need to flip or otherwise move the semiconductor substrate 501, as it allows deposition of one or more layers directly to the backside of the semiconductor substrate 501.

[0054] In some approaches, the deposition process may include two consecutive deposition step. In a first deposition step, a first layer 512 may be deposited on the backside of the semiconductor substrate 501 in an environment suited for PECVD (e.g., a process chamber of the backside deposition apparatus). In some examples, the first layer 512 may include an a-Si film. This deposition step may involve a lower process temperature (e.g., 200-400 °C) compared to that used in LPCVD, applied to a set of first process gases (e.g., reactant gas SiH_4) and plasma introduced to the environment to form the a-Si film.

[0055] In a second deposition step, subsequent to the deposition of the first layer 512 and while the frontside is still facing upward, a second layer 514 may be deposited on the backside of the semiconductor substrate 501, directly over the first layer 512. The second deposition step may occur immediately or substantially immediately after the first deposition step (e.g., within 5 seconds). This deposition step may involve the same process temperature as that of the first deposition step (e.g., 200-400 °C), and a second set of process gases (e.g., reactant gases SiH_4 and N_2O) and plasma introduced to the

environment. In some examples, the second layer 514 may include a SiO_2 film. The SiO_2 film and the a-Si film may each have a prescribed thickness, e.g., up to 12000 Å for a-Si and up to 5000 Å for SiO_2.

[0056] In some embodiments, deposition of the second layer 514 may result in an enhanced backside sealing layer 520 on the backside of the semiconductor substrate 501 without any movement of the semiconductor substrate 501 during the formation of the enhanced backside sealing layer 520. The enhanced backside sealing layer 5320 may thus include an a-Si + SiO_2 stack.

[0057] Again, advantageously, the two deposition steps for producing the bilayer of a-Si and SiO_2 may be performed in the same environment or process chamber and at the same process temperature without breaking the vacuum, or transferring out or otherwise moving the semiconductor substrate 501. Only a change in process gases between deposition steps is needed. No flipping is required as with the conventional approach, such as the example process flow 200 of FIG. 2, since the depositions are performed directly on the backside of the wafer, without any frontside deposition occurring nor any removal or polish of the frontside being needed or performed.

[0058] In some optional approaches, an annealing process may be performed at step 506, similar to that of step 306 (which may also be optional). Similar to the bilayer produced according to step 304, the annealing process at step 506 may be optional because the first layer 512 (e.g., a-Si film) alone can provide the desired results, e.g., backside sealing and mitigation of auto-doping. In some embodiments, the annealing may occur at a different temperature than that used for deposition steps, e.g., 700-1100 °C, within the same environment or process chamber, and allowed to cool over time. By this annealing process, the first layer 512 (e.g., a-Si film) may undergo crystallization and transition to a different material. In some examples, a resulting crystallized layer 516 (e.g., a poly-Si film) may be formed under the SiO_2 film, forming an enhanced backside sealing layer 520' on the backside of the semiconductor substrate 501 without any movement of the semiconductor substrate 301 during the formation of the enhanced backside sealing layer 520'. The enhanced backside sealing layer 520' may thus include a poly-Si + SiO_2 stack. In example process flow 500, the surface smoothness of the enhanced backside sealing layer 520' depends on that of the outer layer, which is second layer 514 (e.g., SiO_2 film).

[0059] Thus, the bilayer structure of the enhanced backside sealing layer 520 or 520' on the semiconductor substrate 501 may include either: (i) the first layer 512 (e.g., a-Si film) and the second layer 514 (e.g., SiO_2 film) without any further annealing or epitaxial processes, or (ii) a crystallized layer 516 produced by annealing (e.g., poly-Si film) and the second layer 514 (e.g., SiO_2 film).

[0060] Optionally, subsequent to the annealing process of step 506, other downstream processes may be performed, such as those described.

[0061] Moreover, the above process can be performed concurrently on multiple semiconductor substrates in a single process chamber or multiple process chambers of a multi-chamber deposition apparatus, which is further described below.

Methods

[0062] FIG. 6 is a flow diagram of an example of a method 600 of backside sealing of a semiconductor substrate, according to some embodiments. One or more of the functions of the method 600 may be performed by or caused by a computerized apparatus or system. Structure for performing the functionality illustrated in one or more of the blocks shown in FIG. 6 may be performed by hardware and/or software components of such computerized apparatus or system, such as, for example, a controller apparatus, a computerized system, or a computer-readable apparatus including a storage medium storing computer-readable and/or computer-executable instructions that are configured to, when executed by a processor apparatus, cause the at least one processor apparatus or a computerized apparatus to perform the operations. A controller may be one example of the computerized apparatus or system. A process chamber may be another example of the computerized apparatus or system. Example components of above apparatus are illustrated in FIGS. 7 – 11, and described in more detail elsewhere herein.

[0063] It should also be noted that the operations of FIG. 6 may be performed in any suitable order, not necessarily the order depicted in FIG. 6. Further, the process shown in FIG. 6 may include additional or fewer operations than those depicted in FIG. 6.

[0064] At block 610, the method 600 may include causing delivery of a first set of one or more process gases to a first process chamber of a deposition apparatus, the first process chamber having a semiconductor substrate disposed therein. In some embodiments, the first process chamber may be one of multiple process chambers or stations of a deposition apparatus, described further below.

[0065] At block 620, the method 600 may include applying a first process temperature in presence of plasma to form a first layer of material on the backside of the semiconductor substrate.

[0066] In some embodiments, the first layer of material may include silicon oxide (SiO_2).

[0067] In some embodiments, the first layer of material may include amorphous silicon.

[0068] In some embodiments, the first process temperature may include a temperature of 200-400 °C.

[0069] At block 630, the method 600 may include causing delivery of a second set of one or more process gases to the first process chamber.

[0070] In some embodiments, the first set of one or more process gases may include silane (SiH4) and nitrous oxide (N_2O), and the second set of one or more process gas may include a carrier gas. For example, these sets of gases may be used with the example process flow 300.

[0071] In some embodiments, the first set of one or more process gases may include silane (SiH_4), and the second set of one or more process gas may include SiH_4 and nitrous oxide (N_2O). For example, these sets of gases may be used with the example process flow 500.

[0072] At block 640, the method 600 may include applying the first process temperature in the presence of plasma to form a second layer of material on the first layer of material on the backside of the semiconductor substrate. The first process temperature may be the same first process temperature (e.g., 200-400 °C) from block 620.

[0073] In some embodiments, the second layer of material may include amorphous silicon. In some embodiments, the second layer of material may include silicon oxide (SiO_2).

[0074] Optionally, at block 650, the method 600 may include, subsequent to the formation of the second layer of material, applying a second process temperature to cause an annealing process to occur, the annealing process comprising causing crystallization of the first layer of material or the second layer of material to collectively form a stack of materials that seals the backside of the semiconductor substrate.

[0075] In some embodiments, the first layer of material may include a layer or film of

silicon oxide (SiO_2); the second layer of material may include a layer or film of amorphous silicon formed on the film of SiO_2; the crystallization of the first layer of material or the second layer of material may include crystallization of the film of amorphous silicon to a layer or film of polycrystalline silicon; and the film of polycrystalline silicon and the film of SiO_2 may collectively form the stack of materials that seals the backside of the semiconductor substrate, and thereby mitigate diffusion of dopants from the semiconductor substrate.

[0076] In some embodiments, the first layer of material may include a layer or film of amorphous silicon; the second layer of material may include a layer or film of silicon oxide (SiO_2) formed on the film of amorphous silicon; the crystallization of the first layer of material or the second layer of material may include crystallization of the film of amorphous silicon to a layer or film of polycrystalline silicon; and the film of polycrystalline silicon and the film of SiO_2 may collectively form the stack of materials that seals the backside of the semiconductor substrate, and thereby mitigate diffusion of dopants from the semiconductor substrate.

[0077] In some implementations, the layer of silicon oxide (SiO_2) may have a thickness up to 5000 angstroms, and the layer of amorphous silicon may have a thickness of up to 12000 angstroms.

[0078] In some embodiments, the semiconductor substrate may be disposed in at least one of one or more process chambers (e.g., the first process chamber) such that the backside of the semiconductor substrate is facing downward and a frontside of the semiconductor substrate is facing upward during the formation of the first layer material on the backside of the semiconductor substrate and the formation of the second layer of material on the backside of the semiconductor substrate.

[0079] In some embodiments, movement of the semiconductor substrate does not occur between the application of the first process temperature and the application of the second process temperature. In some embodiments, during the application of the first process temperature, the first layer of material and the second layer of material may form only on the backside of the semiconductor substrate and may not form on a frontside of the semiconductor substrate.

[0080] In some embodiments, the method 600 may further include causing an epitaxial process to be performed subsequent to the formation of the second layer of material. In

some implementations, the stack of materials may mitigate diffusion of dopants from the semiconductor substrate during the epitaxial process.

Apparatus

[0081] In some embodiments, FIG. 7 is a block diagram that illustrates a substrate processing system 700 used to perform processing on a semiconductor substrate 702 (also referred to herein as a wafer), according to some embodiments. As shown, the substrate processing system 700 may include a chamber 734. A center column may be configured to support a pedestal for when a top surface of the semiconductor substrate 702 is being processed, e.g., a film is being formed on the top surface of the semiconductor substrate 702, or on the backside of the semiconductor substrate 702. The pedestal, in accordance with some embodiments disclosed herein, may be referred to as a showerhead-pedestal ("ShoPed") 706. A showerhead 736 may be disposed over the ShoPed 706.

[0082] In some embodiments, the showerhead 736 may be electrically coupled to power supply 738 via a match network 740. The power supply 738 may be controlled by a control module 742, e.g., a controller. In some embodiments, power may be provided to the ShoPed 706 instead of the showerhead 736. The control module 742 may be configured to operate the substrate processing system 700 by executing process input and control for specific process recipes. Depending on whether the top surface of the semiconductor substrate 702 is receiving a deposited layer or layer stack or the bottom surface of the semiconductor substrate 702 is receiving a deposited layer or layer stack, the controller module 742 may set various operational inputs for a process recipe, such as power levels, timing parameters, process gasses, mechanical movement of a semiconductor substrate 702, and/or the height of the semiconductor substrate 702 relative to the ShoPed 706.

[0083] In some embodiments, the center column may also include lift pins, which are controlled by a lift pin control. Such lift pins may be used to raise the semiconductor substrate 702 from the ShoPed 706 to allow an end effector (not shown) to pick the wafer and to lower the semiconductor substrate 702 after being placed by the end effector. The end effector may also place the semiconductor substrate 702 over spacers 744. As will be described below, the spacers 744 may be sized to provide a controlled separation of the semiconductor substrate 702 between a top surface of the showerhead 736 (facing the wafer) and a top surface of the ShoPed 706 (facing the wafer).

[0084] In some embodiments, the substrate processing system 732 may further include a first gas manifold 746 that is connected to first gas sources 748, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a top surface of the semiconductor substrate 702, the control module 742 may controls the delivery of first gas sources 748 via the first gas manifold 746. The chosen gases may then be flown into the showerhead 736 and distributed in a space volume defined between a face of the showerhead 736 that faces that semiconductor substrate 702 when the wafer is resting over the pedestal.

[0085] In some embodiments, the substrate processing system 732 may further include a second gas manifold 750 that is connected to second gas sources 752, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a bottom surface of the semiconductor substrate 702, the control module 742 may control the delivery of second gas sources 752 via the second gas manifold 750. The chosen gases may then be flown into the showerhead 736 and distributed in a space volume defined between a face of the ShoPed 706 that faces an under surface or under side (e.g., backside) of the semiconductor substrate 702 when the wafer is resting over the spacers 744. The spacers 744 may provide for a separation that optimizes deposition to the under surface of the semiconductor substrate 702, while reducing deposition over the top surface of the semiconductor substrate 702. In some embodiments, while deposition is targeted for the under surface of the semiconductor substrate 702, an inert gas may be flown over the top surface of the semiconductor substrate 702 via the showerhead 736, which may push reactant gases away from the top surface and enable reactant gases provided from the ShoPed 706 to be directed to the under surface of the semiconductor substrate 702.

[0086] In some embodiments, either showerhead 736 or ShoPed 706 may have a zonal deposition design. For example, second gas manifold 750 may be fluidically linked to control the delivery of gases to different zones of a wafer. By controlling the flow of gases to different zones, different films may be deposited on the wafer as desired.

[0087] Further, the gases may be premixed or not. Appropriate valving and mass flow control mechanisms may be employed to ensure that the correct gases are delivered during the deposition and plasma treatment phases of the process. Process gases may exit the chamber 734 via an outlet. A vacuum pump (e.g., a one or two stage mechanical dry pump and/or a turbomolecular pump) may draw process gases out and maintains a suitably low

pressure within the reactor by a close loop-controlled flow restriction device, such as a throttle valve or a pendulum valve.

[0088] In some embodiments, a carrier ring 754 may encircle an outer region of the ShoPed 706. When the top surface of the semiconductor substrate 702 is being processed, e.g., a material is being deposited thereon, the carrier ring 754 may be configured to sit over a carrier ring support region that is a step down from a wafer support region in the center of the ShoPed 706. The top surface of the carrier ring 754 is generally coplanar with the top surface of the semiconductor substrate 702. The carrier ring 754 may include an outer edge side of its disk structure, e.g., outer radius, and a wafer edge side of its disk structure, e.g., inner radius, that is closest to where the semiconductor substrate 702 sits. The carrier ring 754 may be associated with an inner diameter (ID). The inner diameter may extend to an inner perimeter of the carrier ring and generally surround a substrate (e.g., semiconductor substrate 702) in a processing chamber. The wafer edge side of the carrier ring 754 may also include a plurality of contact support structures or "tabs" which may be configured to lift the semiconductor substrate 702 when the carrier ring 754 is held by the spacers 744. The carrier ring 754 may include a plurality of tabs with a quantity selected from a range to support the semiconductor substrate 702 during processing. Additional details regarding embodiments of the tabs will follow.

[0089] FIG. 8 is a block diagram that illustrates another substrate processing system 800 used to perform processing on a semiconductor substrate 802 (also referred to herein as a wafer), according to some embodiments. In some embodiments, spider forks 856 may be used to lift and maintain the carrier ring 854 in its process height, e.g., to allow depositing in the under surface (backside) of the semiconductor substrate 802. The carrier ring 854 may therefore be lifted along with the semiconductor substrate 802. In some implementations, the carrier ring 854 may be rotated to another station, e.g., in a multi-station system.

[0090] Broadly speaking, the embodiments disclosed herein are for a system to deposit PECVD films on the selective side of the wafer (front and/or back) with dynamic control. Some embodiments may include a dual gas-flowing electrode for defining a capacitively-coupled PECVD system. The system may include a gas-flowing showerhead (e.g., showerhead 836) and a ShoPed 806. In some embodiments, the gas-flowing pedestal (i.e., ShoPed) is a combination showerhead and pedestal, which enables deposition on a back-side of the wafer. The electrode geometry combines features of a showerhead, e.g., a gas

mixing plenum, holes, hole-pattern, gas jet preventing baffle, and features of a pedestal. Examples of features of a pedestal include an embedded controlled heater, wafer-lift mechanisms, ability to hold plasma suppression rings, and movability. This enables the transfer of wafers and the processing of gasses with or without RF power from the pedestal.

[0091] In some embodiments, the system may have a wafer lift mechanism that tightly controls parallelism of the substrates against the electrodes. In one example, this may be achieved by setting up the lift mechanism parallel to the two electrodes and controlling manufacturing tolerances, e.g., spindle or lift pins mechanisms. In another example, the lift may be achieved by raising the wafer lift parts. This option may not allow dynamic control of the side that gets deposited.

[0092] In some configurations, the lift mechanism may allow dynamically controlling the substrate position during processing (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. The system may further allow selective enabling/disabling of the side where reactants are flown. One side can flow the reactant and the other side can flow inert gases to suppress the deposition and plasma.

[0093] In some embodiments, the gap between the side of the wafer that does not need plasma/dep may be tightly controlled. This distance may be controlled to suppress plasma. By not controlling the distance, the wafer may be susceptible to plasma damage. For example, the system may allow a minimal gap from about 2 mm to about 0.5 mm, and in another embodiment from about 1 mm to about .05 (limited by the wafer bow), and such gap can be controlled. The gap maybe controlled depending on process conditions.

[0094] In some embodiments, the gas-flowing pedestal (i.e., ShoPed) may enable, without limitation: (a) thermal stabilization of the wafer to processing temperature prior to processing; (b) selective design of hole patterns on the ShoPed to selectively deposition film in different areas of the back-side of the wafer; (c) swappable rings can be attached to achieve appropriate plasma confinement and hole pattern; (d) stable wafer transfer mechanisms within chamber and for transferring wafer outside to another chamber or cassette – such as lift pins, RF-coupling features, minimum-contact arrays; (e) implement gas mixing features, e.g., such as inner plenum, baffle and manifold lines openings; and (f) add compartments in the gas-flowing pedestal (i.e., ShoPed) to enable selective gas

flow to different regions of the back side of the wafer and control flow rates via flow controllers and/or multiple plenums.

[0095] In another embodiment, dynamic gap control using wafer lift mechanism enables: (a) control of the distance from deposition or reactant flowing electrode to the side of the wafer that needs deposition or in the middle so that both sides can be deposited; and (b) the lift mechanism to control the distance dynamically during the process (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. In another embodiment, for a deposition mode used to deposit on the backside of the wafer, film edge exclusion control is highly desirable to avoid lithography-related overlay problems. The lift mechanism used in this system is done via a carrier ring 854 that has a design feature to shadow the deposition on the edge. This specifies the edge exclusion control via the design and shape of the carrier ring.

[0096] FIG. 9A shows a cross-sectional view of an edge region of the ShoPed 906 (e.g., 706, 806). This view provides a cross-sectional representation of a carrier ring 954 (e.g., 754, 854), which has a carrier ring inner radius 954a and a carrier ring outer radius 954b. In some embodiments, the carrier ring 954 includes support extensions 954c, which extend below the substantial flat surface of the carrier ring 954.

[0097] The support extensions 954c are configured to mate and sit within support surfaces defined into a top surface of the spacers 944. The support surfaces provide a complementary mating surface for the support extensions 954c, such that the carrier ring 954 is prevented from sliding or moving when supported by the spacers 944. Although three spacers are shown as spacers 944 are shown in FIG. 9, it is envisioned that any number of spacers may be provided, so long as the carrier ring can be supported substantially parallel to the surface of the ShoPed 906, and spacing is defined for supporting semiconductor substrate 902 at a spaced apart relationship from a top surface of the ShoPed 906.

[0098] Further shown is that a top surface of the ShoPed 906 will include a hole pattern 906a that is distributed throughout the surface to provide even distribution and output of gases during operation. In one embodiment, the hole pattern 906a is distributed in a plurality of concentric rings that start at the center of the top surface of the ShoPed 906 and extend to an outer periphery of the ShoPed 906. At least one hole pattern 906a is provided at an edge hole region 907 of the hole pattern, and orifices defined in the edge

hole region 907 are preferably angled to provide gases non-perpendicular to the surface of the ShoPed 906.

[0099] In one example, the angle or tilt at which the orifices in the edge hole region 907 is defined to tilt or angle away from the center of the ShoPed 906. In one embodiment, the angle is approximately 45° from horizontal. In other embodiments, the angle can vary between 20° from horizontal to about 80° from horizontal. In one embodiment, by providing the angled orifices in the edge hole region 907, additional distribution of process gases can be provided during backside deposition of the semiconductor substrate 902. In one embodiment, the remainder orifices 906d of the hole pattern 906a are oriented substantially perpendicular to the surface of the ShoPed 906 and directed toward the underside of the semiconductor substrate 902.

[0100] FIG. 9B illustrates that when the semiconductor substrate 902 is held by the carrier ring 954, the semiconductor substrate 902 edge will sit on an edge region closer to the carrier ring inner radius 954a of the carrier ring 954. The surface of the showerhead 936 facing the top surface of the semiconductor substrate 902, when positioned using spacers 944, may be substantially close to prevent deposition during a mode where deposition is being carried out to the backside of the semiconductor substrate 902.

[0101] By way of example, the distance between the top of the semiconductor substrate 902 and the surface of the showerhead 936 is preferably between about 2 mm to about.5 mm, and in some embodiments about 1 mm to about .5 mm, depending on the wafer bow. That is, if the wafer is bowed substantially, the separation will be about .5 mm or larger. If the wafer is not yet bowed substantially, the separation can be less than about .5 mm. In one embodiment, it is preferable that the separation be minimized to prevent deposition on the top side of the substrate when the backside of the substrate is being deposited with a layer of material. In some embodiments, the showerhead 936 is configured to supply an inert gas flow over the top side of the semiconductor substrate 902 during when the backside of the substrate is being deposited and deposition gases are being supplied by the ShoPed 906.

[0102] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems.

[0103] FIG. 10 is a diagram of a cross-sectional view of a processing system 1000 for depositing film on a backside of a semiconductor substrate, according to some embodiments herein. In some embodiments, the processing system 1000 may include a showerhead 1002, a shower-pedestal (ShoPed) 1004, one or more support structures 1006 (e.g., a carrier ring 754, 854, 954 and/or tabs of a carrier ring, or spider forks 856). The one or more support structures 1006 may be configured to support a semiconductor substrate 1020. In some implementations, the one or more support structures 1006 may be coupled to the ShoPed 1004 and/or other structures associated with the processing system 1000, e.g., processing chamber wall(s). In some implementations, electrostatic chucking (e.g., bipolar chucking or monopolar chucking) may be used to further secure the semiconductor substrate 1020 (electrostatic chuck not depicted). In some implementations, as described above, deposition of SiO_2 on the semiconductor substrate 1020 may improve chucking of the semiconductor substrate 1020.

[0104] In some embodiments, the showerhead 1002 may include an electrode 1010 operable by providing RF power to a plurality of zones. For example, there may be two distinct zones configured to receive different amounts of RF power at different or substantially concurrent times. In another example, there may be three distinct zones. In other examples, there may be four or more. The RF power provided to two or more (or in some cases all) of the zones may be the same amount.

[0105] In some implementations, the electrode 1010 may be integrated or embedded into the showerhead 1002. The electrode 1010 may have a specific configuration of zones according to wafer bow and/or other requirements. Examples of zones are discussed above. In certain implementations, however, the electrode 1010 may be a distinct component that may be replaced and installed into the showerhead 1002 without breaking the showerhead 1002. Such interchangeable electrodes may be useful for performing different customized backside film deposition of the type discussed in the present disclosure. For instance, an electrode having three zones may be swapped for one having two zones to correct different types of wafer bow.

[0106] In some embodiments, the ShoPed 1004 may have one or more gas inlets 1005 configured to transport and emit process gas 1007. Examples of process gas 1007 may include silane (SiH_4), nitrous oxide (N_2O), and/or ammonia (NH_3). Inert carrier gases (e.g., argon, nitrogen, neon, or helium) may also be transported through and out of the ShoPed 1004. In some cases, a mixture of process gas and carrier gas may be routed through the

showerhead 1002 and emitted therefrom. Different types of film material may be deposited on the semiconductor substrate 1020 based on the type of process gas. The showerhead 1002 may have one or more gas inlets 1003 configured to receive and disperse purge gas 1008, such as nitrogen. Purge gas 1008 flowing along the top or front side of the semiconductor substrate 1020 may be used to prevent the process gas 1007 from the ShoPed 1004 or impurities from reaching the top or front side of the semiconductor substrate 1020.

[0107] In some embodiments, the semiconductor substrate 1020 may be placed and supported at a position that is closer to the showerhead 1002 than to the ShoPed 1004. In example implementation, the distance of the gap 1012 between the showerhead 1002 and the semiconductor substrate 1020 may be about 1 mm, while the distance of the gap 1014 between the ShoPed 1004 and the semiconductor substrate 1020 may be about 12 mm. Various distances may be used. However, it is notable and useful that the gap 1012 is small (e.g., small enough to not allow a plasma to form) and could be much smaller than the gap 1014. This is to prevent plasma 1015 from developing between the showerhead 1002 and the semiconductor substrate 1020 where the front side of the semiconductor substrate 1020 is. That is, the plasma 1015 is encouraged to form at the backside 1025 of the semiconductor substrate 1020, where the backside faces away from the showerhead 1002 and the electrode 1010, and faces toward the ShoPed 1004 and/or support structures 1006. The front side may have sensitive and expensive features (transistors, memory cells, wiring lines, etc.). In some implementations, a flowing purge gas out of holes in the showerhead 1002 may push away any process gas or precursor that might have been left or transported to the front side.

[0108] As already discussed herein, by specifying the amount of RF power provided to different zones of the electrode 1010, and at different times in some implementations, film material having properties varying spatially across the semiconductor substrate 1020 may be formed. Some examples of film properties include internal stress (e.g., tensile stress or a compressive stress) and film thickness.

[0109] FIG. 11 is a schematic of a process system suitable for conducting deposition processes, such as frontside deposition processes, in accordance with embodiments. The system 1100 includes a transfer module 1103. The transfer module 1103 provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 1103

is a multi-station reactor 1109 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-station reactor 1109 may include multiple stations 1111, 1113, 1115, and 1117 that may sequentially perform operations in accordance with disclosed embodiments. Stations may include a heated pedestal or substrate support, one or more gas inlets or showerhead or dispersion plate.

[0110] Mounted on the transfer module 1103 may be one or more single or multi-station modules 1107 capable of performing plasma or chemical (non-plasma) pre-cleans, other deposition operations, or etch operations. The module may also be used for various treatments to, for example, prepare a substrate for a deposition process. The system 1100 also includes one or more wafer source modules 1101, where wafers are stored before and after processing. An atmospheric robot (not shown) in the atmospheric transfer chamber 1119 may first remove wafers from the wafer source modules 1101 to loadlocks 1121. A wafer transfer device (generally a robot arm unit) in the transfer module 1103 moves the wafers from loadlocks 1121 to and among the modules mounted on the transfer module 1103.

[0111] In various embodiments, a system controller 1142 is employed to control process conditions during deposition. The system controller 1142 will typically include one or more memory devices and one or more processors. A processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0112] The system controller 1142 may control all the activities of the deposition apparatus. The system controller 1142 executes system control software, including sets of instructions for controlling the timing, mixture of gases, chamber pressure, chamber temperature, wafer temperature, radio frequency (RF) power levels, wafer chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the system controller 1142 may be employed in some embodiments.

[0113] The depicted embodiment includes a user interface associated with the system controller 1142. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0114] System control logic may be configured in any suitable way. In general, the logic can be designed or configured in hardware and/or software. The instructions for controlling the drive circuitry may be hard coded or provided as software. The instructions may be provided by "programming." Such programming is understood to include logic of any form, including hard coded logic in digital signal processors, application-specific integrated circuits, and other devices which have specific algorithms implemented as hardware. Programming is also understood to include software or firmware instructions that may be executed on a general-purpose processor. System control software may be coded in any suitable computer readable programming language.

[0115] The computer program code for controlling the processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran, or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program. Also as indicated, the program code may be hard coded.

[0116] The controller parameters relate to process conditions, such as, for example, process gas composition and flow rates, temperature, pressure, cooling gas pressure, substrate temperature, and chamber wall temperature. These parameters are provided to the user in the form of a recipe and may be entered utilizing the user interface.

[0117] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller 1142. The signals for controlling the process are output on the analog and digital output connections of the system 1100.

[0118] The system software may be designed or configured in different ways. For example, various chamber component subroutines or control objects may be written to control operation of the chamber components necessary to carry out the deposition processes in accordance with the disclosed embodiments. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code.

[0119] In some implementations, a system controller 1142 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for

controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the "controller," which may control various components or subparts of the system or systems. The system controller 1142, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings in some systems, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

System Controllers

[0120] Broadly speaking, a controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. Such controller may be used in or with any of the apparatus described herein. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0121] A system controller may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, a system controller may be in the "cloud" or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new

process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0122] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a CVD chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0123] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0124] A system controller may include various programs. A substrate positioning program may include program code for controlling chamber components that are used to load the substrate onto a pedestal or chuck and to control the spacing between the substrate and other parts of the chamber such as a gas inlet and/or target. A process gas control

program may include code for controlling gas composition, flow rates, pulse times, and optionally for flowing gas into the chamber prior to deposition in order to stabilize the pressure in the chamber. A pressure control program may include code for controlling the pressure in the chamber by regulating, e.g., a throttle valve in the exhaust system of the chamber. A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas such as helium to the wafer chuck.

[0125] Examples of chamber sensors that may be monitored during deposition include mass flow controllers, pressure sensors such as manometers, and thermocouples located in the pedestal or chuck. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain desired process conditions.

[0126] The foregoing describes implementation of disclosed embodiments in a single or multi-chamber semiconductor processing tool. The apparatus and process described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels, and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically includes some or all of the following steps, each step provided with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

Conclusion

[0127] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Embodiments disclosed herein may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. Further, while the disclosed

embodiments will be described in conjunction with specific embodiments, it will be understood that the specific embodiments are not intended to limit the disclosed embodiments. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

CLAIMS

What is claimed is:

1. An apparatus configured for backside sealing of a semiconductor substrate, the apparatus comprising:

one or more process chambers;

a showerhead configured to deliver one or more process gases to a backside of the semiconductor substrate in at least one of the one or more process chambers; and

a controller coupled to the showerhead and the one or more process chambers, and configured to:

cause delivery of a first set of one or more process gases to a first process chamber having the semiconductor substrate;

apply a first process temperature of 200-400 °C in presence of plasma to form a layer of silicon oxide (SiO_2) on the backside of the semiconductor substrate;

cause delivery of a second set of one or more process gases to the first process chamber; and

apply the first process temperature of 200-400 °C in the presence of plasma to form a layer of amorphous silicon on the layer of SiO_2 on the backside of the semiconductor substrate to collectively form a stack of materials that seals the backside of the semiconductor substrate and mitigates diffusion of dopants from the semiconductor substrate.

2. The apparatus of claim 1, wherein the semiconductor substrate is disposed in the at least one of the one or more process chambers such that the backside of the semiconductor substrate is facing downward and a frontside of the semiconductor substrate is facing upward during the formation of the layer of SiO_2 on the backside of the semiconductor substrate and the formation of the layer of amorphous silicon on the backside of the semiconductor substrate.

3. The apparatus of claim 1, wherein the first set of one or more process gases comprises silane (SiH_4) and nitrous oxide (N_2O), and the second set of one or more process gas comprises a carrier gas.

4. The apparatus of claim 1, wherein the layer of silicon oxide (SiO_2) comprises a thickness up to 5000 angstroms, and the layer of amorphous silicon comprises a thickness of up to 12000 angstroms.

5. The apparatus of claim 1, wherein the controller is further configured to, subsequent to the formation of the layer of amorphous silicon, apply a second process temperature that is at least 700 °C to cause an annealing process to occur, the annealing process comprising causing crystallization of the layer of amorphous silicon to form a layer of polycrystalline silicon to collectively form the stack of materials that seals the backside of the semiconductor substrate.

6. The apparatus of claim 5, wherein:

the controller is further configured to perform an epitaxial process subsequent to the formation of the layer of amorphous silicon; and

the stack of materials mitigates diffusion of dopants from the semiconductor substrate during the epitaxial process.

7. The apparatus of claim 5, wherein movement of the semiconductor substrate does not occur between the application of the first process temperature and the application of the second process temperature.

8. The apparatus of claim 5, wherein, during the application of the first process temperature, the amorphous silicon and the polycrystalline silicon form only on the backside of the semiconductor substrate and do not form on a frontside of the semiconductor substrate.

9. An apparatus comprising:

a first process chamber configured to receive a semiconductor substrate;

a showerhead configured to deliver one or more process gases to a backside of the semiconductor substrate in the first process chamber; and

a controller coupled to at least the showerhead and the first process chamber, and configured to:

cause delivery of a first set of one or more process gases to the first process chamber having the semiconductor substrate;

apply a first process temperature of 200-400 °C in presence of plasma to form a layer of amorphous silicon on the backside of the semiconductor substrate;

cause delivery of a second set of one or more process gases to the first process chamber; and

apply the first process temperature of 200-400 °C in the presence of plasma to form a layer of silicon oxide (SiO_2) on the layer of amorphous silicon on the backside of the semiconductor substrate to collectively form a stack of materials that seals the backside of the semiconductor substrate and mitigates diffusion of dopants from the semiconductor substrate.

10. The apparatus of claim 9, wherein the first set of one or more process gases comprises silane (SiH_4), and the second set of one or more process gas comprises SiH_4 and nitrous oxide (N_2O).

11. The apparatus of claim 9, wherein the controller is further configured to, subsequent to the formation of the layer of SiO_2, apply a second process temperature that is at least 700 °C to cause an annealing process to occur, the annealing process comprising causing crystallization of the layer of amorphous silicon to form a layer of polycrystalline silicon to collectively form the stack of materials that seals the backside of the semiconductor substrate.

12. A method for backside sealing of a semiconductor substrate, the method comprising:

causing delivery of a first set of one or more process gases to a first process chamber of a deposition apparatus, the first process chamber having a semiconductor substrate disposed therein;

applying a first process temperature in presence of plasma to form a first layer of material on the backside of the semiconductor substrate;

causing delivery of a second set of one or more process gases to the first process chamber;

applying the first process temperature in the presence of plasma to form a second layer of material on the first layer of material on the backside of the semiconductor substrate to collectively form a stack of materials that seals the backside of the

semiconductor substrate and mitigates diffusion of dopants from the semiconductor substrate.

13. The method of claim 12, wherein the first layer of material comprises silicon oxide (SiO_2).

14. The method of claim 12, wherein the first layer of material comprises amorphous silicon.

15. The method of claim 12, wherein the second layer of material comprises amorphous silicon.

16. The method of claim 12, wherein the second layer of material comprises silicon oxide (SiO_2).

17. The method of claim 12, wherein the first process temperature comprises a temperature of 200-400 °C.

18. The method of claim 12, wherein the first set of one or more process gases comprises silane (SiH_4) and nitrous oxide (N_2O), and the second set of one or more process gas comprises a carrier gas.

19. The method of claim 12, wherein the first set of one or more process gases comprises silane (SiH_4), and the second set of one or more process gas comprises SiH_4 and nitrous oxide (N_2O).

20. The method of claim 12, further comprising, subsequent to the formation of the second layer of material, applying a second process temperature to cause an annealing process to occur, the annealing process comprising causing crystallization of the first layer of material or the second layer of material to collectively form the stack of materials that seals the backside of the semiconductor substrate.

21. The method of claim 20, wherein:
the first layer of material comprises a film of silicon oxide (SiO_2);

the second layer of material comprises a film of amorphous silicon formed on the film of SiO_2;

the crystallization of the first layer of material or the second layer of material comprises crystallization of the film of amorphous silicon to a film of polycrystalline silicon; and

the film of polycrystalline silicon and the film of SiO_2 collectively form the stack of materials that seals the backside of the semiconductor substrate, and thereby mitigates diffusion of dopants from the semiconductor substrate.

22. The method of claim 20, wherein:

the first layer of material comprises a film of amorphous silicon;

the second layer of material comprises a film of silicon oxide (SiO_2) formed on the film of amorphous silicon;

the crystallization of the first layer of material or the second layer of material comprises crystallization of the film of amorphous silicon to a film of polycrystalline silicon; and

the film of polycrystalline silicon and the film of SiO_2 collectively form the stack of materials that seals the backside of the semiconductor substrate, and thereby mitigates diffusion of dopants from the semiconductor substrate.

23. The method of claim 12, further comprising causing an epitaxial process to be performed subsequent to the formation of the second layer of material;

wherein the stack of materials mitigates diffusion of dopants from the semiconductor substrate during the epitaxial process.

24. The method of claim 12, wherein movement of the semiconductor substrate does not occur between the application of the first process temperature and the application of the second process temperature.

25. The method of claim 12, wherein, during the application of the first process temperature, the first layer of material and the second layer of material form only on the backside of the semiconductor substrate and do not form on a frontside of the semiconductor substrate.