WHAT IS CLAIMED IS:

1. An electronic device, comprising:

a semiconductor memory device configured to store process information and to output the process information to outside of the semiconductor memory device; and

a host configured to read the process information from the semiconductor memory device, and to:

select one of a plurality of operation modes depending on the process information, and set to an operation mode of the plurality of operation modes of the semiconductor memory device, the setting of the operation mode of the semiconductor memory device including writing to a mode register of the semiconductor memory device,

wherein;

the process information is information indicating whether a process used to manufacture the semiconductor memory device is an enhanced process or a legacy process,

the plurality of operation modes define a plurality of respectively different latencies, by which data are output from the semiconductor memory device in response to a read command, and include:

a first operation mode, in which the semiconductor memory device is set by the host to operate at a first latency and a first voltage,

a second operation mode, in which the semiconductor memory device is set by the host to operate at the first latency and a second voltage, the second voltage being less than the first voltage, and

a third operation mode, in which the semiconductor memory device is set by the host to operate at a second latency and the first voltage, the second latency being less than the first latency,

the process information is programmed in the semiconductor memory device as part of a process of manufacturing the semiconductor memory device;

when the process information programmed in the semiconductor memory device as part of manufacturing the semiconductor memory device indicates the enhanced process, the process used to manufacture peripheral circuits of the semiconductor memory device is a high-K metal gate process, and the host sets the semiconductor memory device with an operation parameter corresponding to one of the first, second, and third operation modes, and

when the process information programmed in the semiconductor memory device as part of manufacturing the semiconductor memory device indicates the legacy process, the process used to manufacture peripheral circuits of the semiconductor memory device is not the high-K metal gate process, and the host does not set the semiconductor memory device with an operation parameter corresponding to one of the first, second, and third modes.

2. The electronic device as claimed in claim 1, wherein the process information corresponds to process information applied to a peripheral circuit to control a cell array of the semiconductor memory device.

3. The electronic device as claimed in claim 1, wherein the semiconductor memory device includes a program component for storing the process information.

4. The electronic device as claimed in claim 3, wherein the process information is output through a mode register read by the host.

5. The electronic device as claimed in claim 1, wherein, when the process information corresponds to the enhanced process, the host sets the semiconductor memory

device with an operation parameter corresponding to one selected in advance from among the plurality of operation modes.

6. The electronic device as claimed in claim 5, wherein the host performs a training operation for optimizing a reference voltage and a timing of the semiconductor memory device set with the operation parameter.

7. The electronic device as claimed in claim 1, wherein the semiconductor memory device includes a mode register set storing information about one or more of an operating voltage or an operating speed corresponding to the selected operation mode.

8. A method for setting a semiconductor memory device, the method comprising:

reading, by a host, process information from the semiconductor memory device, wherein the process information is programmed in the semiconductor memory device as part of a process of manufacturing the semiconductor memory device;

determining, by the host, whether the process information indicates an enhanced process or a legacy process;

determining, by the host, one of a plurality of operation modes, depending on the determination result of the process information; and

setting, by the host, a mode register set of the semiconductor memory device such that the semiconductor memory device operates according to the operation mode set by the host,

wherein the plurality of operation modes define a plurality of respectively different latencies, by which data are output from the semiconductor memory device in response to a read command, and include:

a first operation mode, in which the semiconductor memory device is set by the host to operate at a first latency and a first voltage,

a second operation mode, in which the semiconductor memory device is set by the host to operate at the first latency and a second voltage, the second voltage being less than the first voltage, and

a third operation mode, in which the semiconductor memory device is set by the host to operate at a second latency and the first voltage, the second latency being less than the first latency;

when the process information programmed in the semiconductor memory device as part of manufacturing the semiconductor memory device indicates the enhanced process, the process used to manufacture peripheral circuits of the semiconductor memory device is a high-K metal gate process, and the host sets the semiconductor memory device with an operation parameter corresponding to one of the first, second, and third operation modes, and

when the process information programmed in the semiconductor memory device as part of manufacturing the semiconductor memory device indicates the legacy process, the process used to manufacture peripheral circuits of the semiconductor memory device is not the high-K metal gate process, and the host does not set the semiconductor memory device with an operation parameter corresponding to one of the first, second, and third modes.

9. The method as claimed in claim 8, wherein:

the semiconductor memory device includes a cell array in which the data are stored, and a peripheral circuit configured to control the cell array and to control an input/output of the data, and

the process information corresponds to a process used to manufacture the peripheral circuit.

10. The method as claimed in claim 9, wherein the enhanced process corresponds to a high-K metal gate process or a fin field effect transistor process.

11. The method as claimed in claim 9, wherein the reading of the process information is performed by a mode register read for reading the process information stored in the mode register set of the semiconductor memory device.

12. The method as claimed in claim 9, wherein the reading of the process information is performed by a control operation for reading the process information programmed at a nonvolatile memory element provided in the semiconductor memory device.

13. The method as claimed in claim 12, wherein the semiconductor memory device includes a dedicated pin for outputting the process information.

14. The method as claimed in claim 8, further comprising performing a training operation for optimizing a timing and a reference voltage level of the semiconductor memory device, after the mode register set of the semiconductor memory device is set.