

controlled to reduce the amount of defects on the substrate, and achieve high etch selectivity of silicon nitride to silicon oxide, silicon and or other exposed substrate surface materials.

[0043] In operation 106, silicon nitride on the substrate is selectively etched, with the etch selective to other exposed materials on the substrate such as silicon oxide and silicon. Introduction of silicon from the silicon source may increase or decrease the etch rate. For example, some of the etching species may react with the silicon source, thereby reducing the etch rate of silicon nitride. In other embodiments, etch rate may increase, for example if the silicon source used is a silicon fluoride (SiF_x) gas. When the plasma is ignited, SiF_x generates silicon and fluorine plasma, whereby some fluorine plasma is used as the etching species for selectively etching silicon nitride.

[0044] Process conditions for the method described with respect to Figure 1 depend on the substrate size, substrate composition, amounts of etch chemistry, chamber volume, and types of plasma processing tools used. The pressure of the chamber may depend on the type of plasma chamber. The chamber pressure may be maintained at a level suitable for sustaining a plasma in the chamber. In some embodiments, the temperature of a solid silicon source may be monitored and controlled to be a temperature between about 0°C and about 500°C , or between about 10°C and about 400°C , or about 100°C , or about 200°C , or about 300°C , or about 400°C . In some embodiments, disclosed embodiments are performed at a temperature greater than about 100°C . For example, where a solid silicon source is located at or near a coil of a plasma generator, the solid silicon source may be heated up to a temperature greater than about 300°C .

[0045] In various embodiments, the etching process in the process chamber may be performed at a temperature, such as a substrate or pedestal temperature, different than or similar to the temperature of the solid silicon source. The temperature may be the substrate temperature, which may be coupled with the pedestal temperature. The pedestal temperature may be used as a proxy for substrate temperature for the disclosed embodiments. In some embodiments, the etching process is performed at a pedestal temperature between about 0°C and about 80°C . In some embodiments, the temperature may be higher or lower depending on the chamber volume, amount of fluorinating gas, amount of silicon sources, types of silicon sources used, and plasma processing conditions.

semiconductor manufacturing factory.

[0067] Alternatively, disclosed embodiments can be carried out in a capacitively-coupled plasma etch chamber such as chamber 400 shown in Figure 4. The chamber 400 includes an interior 402 maintained at a desired vacuum pressure by a vacuum pump connected to an outlet 404 in a lower wall of the chamber. Interior 402 includes a plasma region 450 where plasma may be generated. A solid silicon source may be a component of chamber 400, or attached to components of the chamber 400. In some embodiments, a solid silicon source such as adapter ring 450a may be placed at or near gas distribution plate 424 or at or near the cylindrical or conical heated liner 426. In some embodiments, the solid silicon source may be a diffuser ring (not shown), a rod (not shown), or a silicon piece (not shown) in the chamber 400.

[0068] Etching gas such as a fluorinating gas can be supplied to a showerhead arrangement to supply gas from one or more gas sources 406 to a plenum 408 extending around the underside of a dielectric window 410. A fluidic silicon source may also be supplied to the showerhead arrangement to a plenum 408. A high density plasma can be generated in the chamber by supplying RF energy from an RF source 412 to an external RF antenna 414 such as a planar spiral coil having one or more turns outside the dielectric window 410 on top of the chamber. The plasma generating source can be part of a modular mounting arrangement removably mounted in a vacuum tight manner on the upper end of the chamber.

[0069] A semiconductor substrate 416 such as a substrate including silicon nitride is placed within the chamber on the substrate support 418 such as a cantilever chuck arrangement removably supported by a modular mounting arrangement from a sidewall of the chamber. The substrate support 418 can include a bottom electrode for supplying an RF bias to the substrate during processing thereof.

[0070] The substrate support 418 is at one end of a support arm mounted in a cantilever fashion such that the entire substrate support/support arm assembly can be removed from the chamber by passing the assembly through an opening in the sidewall of the chamber. The substrate support 418 can include a chucking apparatus such as an electrostatic chuck 420 and the substrate 416 can be surrounded by a dielectric focus ring 422. The chuck can include an RF biasing electrode for applying an RF bias to the substrate during an etching process. The

at the same chamber pressure and pedestal temperature. The selectivity of SiN to TEOS was determined to be infinite.

EXPERIMENT 4

[0092] In another experiment, a non-N₂O-based chemistry was used in a capacitively coupled plasma at sub-torr pressure with no ICP power. The chamber pressure was set at 500 mTorr, 100 sccm CF₄ was flowed to the chamber, and a bias was applied at a power of 200W at 100°C for 30 seconds. In one trial, the plasma was generated in a ceramic dome and no silicon source was provided. The selectivity of silicon nitride to oxide was 2.3, and the selectivity of silicon nitride to poly-silicon was 0.85 (i.e., poly-silicon etched faster than silicon nitride). In a second trial, the plasma was generated in a ceramic dome including a silicon source. The selectivity of silicon nitride to oxide was 2.9, and the selectivity of silicon nitride to poly-silicon was 1.56 (poly-silicon etched slower than silicon nitride). The poly-silicon etch rate was reduced by 44%. These results indicate that disclosed embodiments improve etch selectivity for non-N₂O based silicon nitride etch processes.

CONCLUSION

[0093] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.