

Process for fabricating a substrate of the silicon-on-insulator type

Background of the invention

The present invention relates to the field of processes for fabricating
5 what are called SOI (silicon on insulator) substrates.

Such a substrate comprises a silicon oxide (SiO_2) layer buried
between a bulk silicon substrate and thin silicon layer.

These substrates are intended to be used in the fields of electronics,
optics or optoelectronics.

10 The invention relates more particularly to the finishing steps of these
substrates.

Description of the prior art

15 An example of a process for fabricating an SOI substrate is already
known from document US 2003/0181001.

That process involves simple implantation of hydrogen ions, or ions
of another rare gas, into a surface-oxidized substrate so as to form therein a plane of
weakness. This substrate is then bonded to a support and then an annealing
20 operation is carried out at temperatures between 400°C and 600°C so as to detach
an active layer from this implanted substrate and transfer it onto the support.

To reduce the roughness of this active layer, a finishing annealing
operation is then carried out in an atmosphere containing hydrogen, an inert gas or a
mixture of the two gases, at a temperature between 1100°C and 1350°C . This
25 temperature range is chosen so as, on the one hand, to limit the annealing time and,
on the other hand, to avoid any contamination by impurities, such as heavy metals.

The above document specifies that the aforementioned heat treatment
may be carried out by a technique called "long annealing" for a time between 10
minutes and 8 hours, or by a technique known to those skilled in the art by the name
30 RTA (rapid thermal annealing). In the latter case, this process is carried out in an
RTA annealing apparatus that allows rates of temperature rise of greater than
 10°C/s and relatively short annealing times, of around 30 seconds to 1 minute, to be
achieved.

Finally, this annealing step may be followed by a sacrificial oxidation
35 step.

However, the process described in that document has several drawbacks, which will be explained below, namely the partial dissolution of the buried oxide layer and the inhomogeneity of the reduction in roughness of the silicon active layer.

5 Annealing for several hours from the proposed temperature ranges, which may be up to 1350°C, results in at least partial dissolution of the buried silicon oxide (SiO_2) layer, by diffusion of the oxygen forming the silicon dioxide and by evaporation of this oxygen at the surface of the silicon active layer.

10 For high annealing temperatures, above about 1200°C, the dissolution phenomenon is also linked with the increase in solubility of oxygen in silicon and consequently its dissolution in the bulk substrate and the silicon active layer.

This effect is even more pronounced for thin silicon layers with a thickness of 200 nanometers or less.

15 In addition, the diffusion of oxygen is not homogeneous through the active layer. Consequently, the SOI substrate obtained has a buried oxide layer of poorly controlled thickness, that is to say the thickness is both less than that normally expected in the absence of the aforementioned diffusion phenomenon and also not uniform over the entire surface of the substrate.

20 Tests have been carried out so as to measure these drawbacks.

The results are plotted in the appended figure 1, which shows on the y-axis the thickness E_{SiO_2} of the buried silicon dioxide layer of an SOI substrate after thermal annealing and on the x-axis the average thickness E_{Si} of the silicon active layer before annealing. The thicknesses are expressed in nanometers.

25 Curves a, b and c represent the results obtained after annealing at temperatures of 1100°C, 1150°C and 1200°C, respectively.

Other complementary results are plotted in the appended figure 2, which represents on the y-axis the change in standard uniformity Δ_{SiO_2} as a result of annealing this buried silicon dioxide layer and on the x-axis the thickness E_{Si} of the silicon active layer before annealing, expressed in nanometers.

30 Curves d, e and f represent the results obtained after annealing at temperatures of 1100°C, 1150°C and 1200°C, respectively.

An annealing operation at 1200°C for example is an operation during which the temperature gradually rises over several hours and is then held for 5 minutes at 1200°C.

As may be seen in figure 1, the higher the annealing temperature the smaller the thickness of the SiO₂ for a given thickness of the silicon active layer. Moreover, the smaller the thickness of the silicon active layer the greater is this effect, especially for annealing above 1100°C.

5 Thus, after annealing at 1200°C (see curve c) and for silicon active layer thicknesses greater than 200 nanometers, a reduction in the thickness of the SiO₂ of around 6 nanometers (compared with curve a) is observed and without the thickness uniformity of this layer being substantially degraded (see figure 2).

10 The term "thickness uniformity" denotes the maximum deviation in thickness of the buried SiO₂ layer within the SOI wafer. A uniformity of 1 to 1.5 nm for an SiO₂ layer with an average thickness of 145 nm is acceptable and commonplace. Moreover, the "change in thickness uniformity" on the final product corresponds to the change between the thickness uniformity values measured before and after the annealing, respectively.

15 The 0% value of the change in uniformity in figure 2 corresponds to the case in which there is no change in thickness uniformity. The uniformity remains the same as that of the SiO₂ layer before the annealing, that is to say of about 1 to 1.5 nm for an SiO₂ layer whose thickness before annealing was 145 nm.

20 However, for a silicon active layer with a thickness of 100 nanometers or less, the reduction in the thickness of the SiO₂ layer exceeds 10 nanometers (see figure 1) and the change in uniformity may be up to 500% of the initial uniformity value of 1 to 1.5 nm considered as being acceptable, as may be seen in curve f, that is to say this change may reach 5 to 7.5 nm.

25 Figure 2 also shows that this phenomenon, namely the loss of uniformity of the buried oxide thickness, is even greater for SOI substrates in which the thin silicon layer is less than 60 nm.

30 In addition, other tests carried out have shown that long annealing in an atmosphere containing hydrogen and/or argon is not completely effective for minimizing the roughness of the surface of the silicon active layer and above all for minimizing it homogeneously.

35 It is also known, from document US 2003/0134489, that a fracture in a substrate, obtained by implantation followed by detachment annealing, leads to the formation, on the surface of the thin detached layer, of a particularly rough and damaged localized zone, hereafter in the description called "dense zone". This dense zone is located on the edge of the substrate wafer. It corresponds to the zone where the detachment was initiated, that is to say also to the zone in which the

hottest point in the furnace, in which the detachment annealing is carried out, is located. This effect is particularly appreciable when the detachment is carried out purely thermally and when the implanted species consists only of H^+ ions.

Typically, after a first rapid smoothing anneal, it has been observed
5 that the measured roughness in the dense zone can be more than 30% higher than on the rest of the wafer.

The technical solution to this problem, consisting in carrying out the annealing for long times and/or at high temperature, so as to minimize the roughness in the dense zone, is not appropriate as it further exacerbates the
10 abovementioned oxide dissolution phenomenon.

Summary of the invention

The aim of the invention is to solve the aforementioned drawbacks of
15 the prior art.

In particular, the object of the invention is to provide a fabrication process which makes it possible to obtain an "SOI" substrate, the thin silicon active layer of which has surface roughness that is uniform and preferably as small as possible, while still having a buried layer of uniform thickness.

For this purpose, the invention relates to a process for fabricating a
20 substrate of the SOI (silicon on insulator) type, comprising the following steps, consisting in:

a) atomic or ionic species are implanted into a silicon substrate called the "donor" substrate, so as to form therein a weakened zone which forms the
25 boundary between said thin layer and the remainder of the donor substrate;

b) this donor substrate is bonded to a substrate called the "receiver" substrate, by molecular adhesion, a layer of silicon oxide (SiO_2) being interposed between the two;

c) said remainder of the donor substrate is detached, along the
30 weakened zone, so as to obtain an SOI substrate comprising the silicon receiver substrate covered with a silicon dioxide layer and a thin silicon layer;

d) one or more finishing steps are carried out on said thin silicon layer, including at least one long thermal annealing step for a time of at least 10 minutes, in a gaseous atmosphere containing hydrogen and/or argon.

According to the invention, step a) is carried out by co-implantation
35 of atomic or ionic species and/or step c) is carried out by a mainly mechanical

detachment, and said long annealing step or steps are all carried out at a temperature of at least 950°C but not exceeding 1100°C.

According to other advantageous but nonlimiting features of the invention, taken individually or in combination:

- 5 - the finishing steps comprise at least one sacrificial oxidation of the free surface of said thin layer followed by a deoxidation so as to eliminate the thickness of material damaged by the detachment step c);
- step a) consists in carrying out a hydrogen/helium co-implantation;
- the detachment of step c) is initiated by a mechanical action on the
10 weakened zone;
- the detachment of step c) is carried out by:
 - applying a heat treatment for further weakening the weakened zone, without initiating thermal detachment from the remainder of the donor substrate, and
 - 15 • applying a pulse that induces self-sustained detachment from the remainder of the donor substrate;
- it consists in forming the silicon oxide (SiO₂) layer by thermal oxidation of the donor substrate and/or of the receiver substrate and in bonding the two substrates to each other so that said silicon oxide (SiO₂) layer lies at the
20 interface;
- the sacrificial oxidation is carried out under dry or wet conditions, at a temperature between 700°C and 1100°C;
- the annealing of step d) is carried out for a maximum time of 15 hours;
- 25 - said thin silicon layer has, over its entire extent, an RMS surface roughness of less than 3 ångströms over a scanning area of 30 µm × 30 µm;
- the thickness of the thin silicon layer is 200 nanometers or less;
- the thickness of the buried silicon oxide (SiO₂) layer is 50 nanometers or less; and
- 30 - the thickness uniformity of the buried silicon oxide (SiO₂) layer is 1.8 nm or better.

Brief description of the drawings

- 35 Other features and advantages of the invention will become apparent from the description that will now be given, with reference to the appended

drawings, which show, by way of indication but implying no limitation, one possible embodiment thereof.

In these drawings:

5 - figure 1 is a graph showing the thickness E_{SiO_2} of the silicon dioxide layer of an SOI substrate after annealing as a function of the thickness E_{Si} of the thin silicon layer before annealing, for heat treatments carried out at various temperatures and in accordance with the prior art;

10 - figure 2 is a graph showing the change in thickness uniformity Δ_{SiO_2} as a result of the annealing of the silicon dioxide layer of an SOI substrate as a function of the thickness E_{Si} of the thin silicon layer before annealing, for heat treatments carried out at various temperatures and in accordance with the prior art;

 - figures 3A to 3H are diagrams showing the various steps of the process according to the invention; and

15 - figure 4 is a graph showing the values of the surface roughness R of SOI substrates of two batches of substrates obtained by a process of the prior art and by the process according to the invention, respectively, the results shown by the fine lines representing the results of measurements carried out in the center of the substrates and the results shown in bold lines representing the results of measurements carried out on the edge of said substrates.

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Description of the preferred embodiments

This process will now be described in greater detail.

25 It comprises a first series of steps for the formation, detachment and transfer of a thin layer onto a donor substrate, illustrated in figures 3A to 3D, and a second series of steps for finishing, illustrated in figures 3E to 3H.

 Figure 3A shows a donor substrate 1 made of preferably single-crystal silicon (Si) covered with a silicon dioxide (SiO_2) layer 2, the free surface of which bears the numerical reference 20.

30 The oxide layer 2 may result from thermal oxidation of the donor substrate 1 or may have been formed by deposition, conventionally by one of the chemical vapor deposition techniques known to those skilled in the art by the acronyms "CVD" (*Chemical Vapor Deposition*) and "LPCVD" (*Low Pressure Chemical Vapor Deposition*).

35 Figure 3A also shows a receiver substrate 3, made of single-crystal or polycrystalline silicon.

As can be seen in figure 3B, the donor substrate 1 is then subjected to implantation of atomic or ionic species through the oxide layer 2.

The expression "implantation of atomic or ionic species" is understood to mean any bombardment by these species capable of introducing them into the donor substrate with a maximum concentration at a predetermined depth of the substrate with respect to the bombarded surface 20, for the purpose of creating therein said weakened zone 10. This type of implantation may be carried out for example using the process known by the name Smart-Cut®.

Further details concerning this process may be found in the document "Silicon-on-insulator technology: materials to VLSI", second edition, Jean-Pierre Colinge, Kluwer Academic Publishers, pages 50 and 51.

The weakened zone 10 forms the boundary between a thin layer 11 and the remainder 12 of the donor substrate 1.

The implantation of atomic or ionic species may be a single implantation, that is to say implantation of a single atomic species, such as for example an implantation of hydrogen, helium or another rare gas.

The implantation may also be a co-implantation of atomic or ionic species, that is to say successive implantation of at least two different species, such as for example co-implantation of hydrogen and helium.

The choice of one or other of these implantations will be explained later.

The following implantation conditions may be used as an example:

- implantation of just hydrogen: the implantation dose is preferably between $4 \times 10^{16} \text{ H}^+/\text{cm}^2$ and $7 \times 10^{16} \text{ H}^+/\text{cm}^2$ and the implantation energy between 20 keV and 100 keV;

- co-implantation of helium and hydrogen: preferably, in the case of helium, the implantation dose is between $0.5 \times 10^{16} \text{ He}^+/\text{cm}^2$ and $2 \times 10^{16} \text{ He}^+/\text{cm}^2$ and the implantation energy between 20 keV and 100 keV, and in the case of hydrogen, the implantation dose is between $0.5 \times 10^{16} \text{ H}^+/\text{cm}^2$ and $2 \times 10^{16} \text{ H}^+/\text{cm}^2$ and the implantation energy between 20 keV and 100 keV.

In the case of co-implantation of hydrogen and helium, the helium is preferably implanted before the hydrogen.

Figure 3C shows the step in which the receiver substrate 3 is brought into intimate contact via one of its faces, referenced 30, with the face 20 of the insulator layer 2 of the donor substrate 1.

The bonding between the two substrates takes place by molecular adhesion and the bonding interface bears the numerical reference 4.

Although this has not been shown in the figures, it would also be conceivable to form or deposit the insulator layer 2 on the receiver substrate 3 and then to bond the assembly to a donor substrate 1 that has already undergone the implantation for forming the weakened zone 10. However, in this case, it would be preferable to form or deposit a protective insulation layer on the donor substrate 1 before carrying out the implantation, it being possible, optionally, for this protective layer to be removed before the bonding.

Figure 3D shows that the process then continues with the detachment of the remainder 12 of the donor substrate, along the weakened zone 10, so as to transfer the thin layer 11 onto the support substrate 3, more precisely onto the oxide layer 2.

The detachment may be carried out either purely thermally or mainly mechanically, depending on selection criteria that will be explained later.

The purely thermal detachment consists in subjecting the multilayer stack obtained in figure 3C to thermal annealing, during which spontaneous detachment from the remainder 12 takes place along the weakened zone 10. This thermal detachment is carried out at temperatures between 300°C and 600°C, preferably at about 500°C, for a time long enough to obtain this detachment, typically around one hour.

In the rest of the description and the claims, the expression “mainly mechanical detachment” is understood to mean either a purely mechanical detachment, that is to say one initiated by a mechanical action, obtained for example by running a blade 5 along the weakened zone 10 from one side of the substrate, or a hybrid detachment involving both a heat treatment and a mechanical treatment.

More precisely, this hybrid treatment comprises:

- application of a heat treatment for controllably weakening the weakened zone 10, that is to say a treatment interrupted before detachment is initiated; and then

- application of an energy pulse that triggers “self-sustained” detachment along said zone 10.

An energy pulse may be applied using a machine for automatically separating wafers, for example a machine as described in document US 2006/138189.

The mechanical force exerted by such a separating machine is sufficient to induce "self-sustained" detachment, that is to say a shock is sufficient to initiate and sustain the detachment and, unlike purely mechanical detachment, there is no movement of a tool along the weakened zone.

5 Since the detachment is self-sustained, there is no actual sudden propagation of a fracture wave liable to generate surface undulations. Furthermore, since there is no movement of any tool along the newly created surfaces, there is no degradation of the surface finish of the surfaces thus freed.

10 The free surface 110 of the thin layer 11 thus has a much lower roughness than when such a thin layer is obtained by spontaneous detachment resulting from purely thermal annealing. In particular, the applicant has observed that the roughness of the surface 110 is greatly reduced on the edge of the wafer, in the dense zone that is observed with the techniques of the prior art.

15 According to the invention, during the first series of steps that have just been described, the aim is to carry out the implantation and detachment steps so as to minimize the occurrence of a dense zone with a high roughness. Consequently, the chosen procedure is:

- to form the weakened zone 10 by co-implantation of atomic or ionic species and/or
- 20 - to cause detachment from the remainder 12 by a mainly mechanical technique.

The finishing steps will now be described.

25 A sacrificial oxidation operation is carried out on the surface of the thin layer 11. This operation is made up of an oxidation step, shown in figure 3E, which may be followed by a heat treatment and then by a deoxidation step shown in figure 3F.

The first step consisting of an oxidation is preferably carried out at a temperature between 700°C and 1100°C.

30 It may be carried out under dry conditions, for example by heating the SOI substrate in a gaseous atmosphere, or under wet conditions, for example by heating in an atmosphere containing water vapor.

Whether the oxidation is carried out under dry or wet conditions, the oxidation atmosphere may also be charged with hydrochloric acid.

35 The oxidation step results in the formation of a silicon oxide (SiO_2) layer 111 on the surface of the thin silicon layer 11.

The optional heat treatment second step that follows may be carried out by increasing the temperature at a constant or varying rate until a temperature of above about 1000°C, and preferably between about 1100°C and 1200°C, is reached, in a nonoxidizing gaseous atmosphere. The gaseous atmosphere contains for example argon, nitrogen, hydrogen or other nonoxidizing gases, or a mixture of these gases. The heat treatment may also be carried out under a vacuum.

The duration of this heat treatment is typically about 2 hours.

It should be noted that this heat treatment may be carried out up to a temperature of 1200°C without any risk of the buried SiO₂ layer 2 dissolving, since the upper layer 110 of the silicon layer 11 which is oxidized at 111, prevents this phenomenon.

Finally, the total deoxidation step shown in figure 3F allows the oxide layer 111 formed during the oxidation step to be removed. This step is for example carried out by immersing the SOI substrate for a few minutes in a solution of hydrofluoric acid (HF) diluted in water to 10 or 20% by volume, for example.

A few minutes of immersion of the substrate in this solution are sufficient for removing the silicon oxide layer 111 formed beforehand, the thickness of which layer generally varies from about a hundred to a few hundred nanometers. This way, the thickness of silicon of the layer 11 that was damaged during detachment is removed.

The thin residual silicon layer bears the numerical reference 112. It is slightly thinner than the layer 11.

According to the invention, and as shown in figure 3G, a thermal annealing to smooth the SOI substrate is carried out in a gaseous atmosphere comprising hydrogen and/or argon, in the absence of oxygen, at a temperature of at least 950°C but not exceeding 1100°C, preferably at least 950°C but below 1100°C.

This annealing is called long annealing, that is to say the SOI substrate is held in the aforementioned temperature range for at least about 10 minutes and for a maximum time of a few hours, possibly even up to 15 hours. For a time of less than 10 minutes, the treatment is ineffective while for longer than 15 hours it is no longer economic in terms of production costs.

This annealing is carried out in a suitable furnace.

The SOI substrate obtained bears the reference 6.

It should be noted, on the one hand, that the sacrificial oxidation step shown in figures 3E and 3F is optional and, on the other hand, that, when it is carried out, this may be carried out after the long annealing step of figure 3G.

Finally, as shown in figure 3H, it is possible, optionally, to carry out a chemical-mechanical thinning operation on the thin silicon layer 112 which, once thinned, bears the reference 113.

5 The Applicant has carried out measurements and observed that by forming the weakened zone 10 by co-implantation of atomic or ionic species and/or by causing detachment by a mainly mechanical fracture, it is possible, surprisingly, to limit or even completely eliminate the dense zone observed with the techniques of the prior art.

10 The results are plotted in figure 4 on the y-axis, the RMS roughness **R** of the thin silicon layer of an SOI substrate, expressed in ångströms for a scanning area of $30\text{ }\mu\text{m} \times 30\text{ }\mu\text{m}$. The aforementioned roughness is expressed by an RMS (*Root Mean Square*) value. It is measured by AFM (*Atomic Force Microscopy*), the tip of which scans an area expressed in square microns.

The thickness of said thin silicon layer was 150 nm.

15 The measurements were made each time in the center of the substrate (results shown by the fine lines) and on the edge (results shown by the bold lines).

Figure 4 enables the surface roughness of the thin silicon layer during implementation of a sequence of weakened zone formation/detachment/finishing according to the prior art (A, on the left in figure 4) to be compared with that
20 according to the invention (B, on the right in figure 4).

In case A, the weakened zone was formed by simply implanting H^+ ions, followed by thermal detachment, and the finishing steps are the same as those carried out in case B.

25 In case B, the weakened zone was formed by co-implanting helium and hydrogen, followed by thermal detachment and then sacrificial oxidation and long annealing at a temperature not exceeding 1100°C .

It may be seen that the implementation of the method according to the invention does not achieve any roughness reduction in the center.

30 However, it may be seen that such implementation does have a markedly beneficial effect on the edge of the substrate, in the region where a dense zone is observed with the method according to the prior art. In addition, the RMS roughness values are low, less than 3 ångströms for a scanning area of $30\text{ }\mu\text{m} \times 30\text{ }\mu\text{m}$, are homogeneous over the entire area of the substrate, and are reproducible.

35 Furthermore, at annealing temperatures not exceeding 1100°C , the diffusion of oxygen coming from the silicon oxide layer is greatly reduced, so that the thickness of the oxide layer remains uniform.

Finally, by annealing at a temperature not exceeding 1100°C it is possible to control the risk of contamination by metals and the risk of defects created in the wafers, such as slip lines, caused by the thermal stresses. This make the annealing much easier to carry out on an industrial scale.

5 Several illustrative examples of the invention will be given below.

Example 1:

A silicon donor substrate, covered with a 150 nanometer silicon dioxide layer, underwent a successive co-implantation of hydrogen and then helium with the parameters mentioned below:

- 10 - helium: dose = $1 \times 10^{16} \text{ He}^+/\text{cm}^2$; energy = 50 keV;
- hydrogen: dose = $1 \times 10^{16} \text{ H}^+/\text{cm}^2$; energy = 30 keV.

After said SiO_2 layer was bonded onto a silicon receiver substrate, the process of detaching and transferring a thin silicon layer with a thickness of about 250 nanometers and the SiO_2 layer was carried out. This detachment step was
15 carried out by annealing at a temperature of about 500°C.

The thin silicon layer then underwent a sacrificial oxidation step, that is to say oxidation followed by deoxidation, so as to obtain on top of the buried silicon oxide layer a thin silicon layer of about 190 nanometers.

Finally, a thermal annealing operation was carried out for a time of 4
20 hours, at a temperature of 1100°C, in a gaseous atmosphere containing exclusively hydrogen and argon.

The RMS roughness of the surface of the thin silicon layer was homogeneous and from 2 to 3 ångströms for an AFM scanning area of $30 \mu\text{m} \times 30 \mu\text{m}$.

25 The thickness of the buried oxide (SiO_2) layer was not modified and remained practically homogeneous over the entire area. The measured uniformity was better than 1.8 nm, for an initial SiO_2 thickness of 145 nm.

Example 2:

30 A silicon donor substrate, covered with a 150 nanometer silicon dioxide layer, underwent a successive co-implantation of hydrogen and helium with the parameters mentioned below:

- hydrogen: dose = $2 \times 10^{16} \text{ H}^+/\text{cm}^2$; energy = 30 keV;
- helium: dose = $2 \times 10^{16} \text{ He}^+/\text{cm}^2$; energy = 50 keV.

After said SiO_2 layer was bonded onto a silicon receiver substrate,
35 the process of detaching and transferring a thin silicon layer with a thickness of about 250 nanometers on the SiO_2 layer was carried out.

This detachment step was carried out firstly by annealing at a temperature of about 350°C for 2 to 3 hours, which did not result in detachment, followed by the application of an energy pulse, for example a shock, which mechanically triggered self-sustained detachment.

5 Finally, a sacrificial oxidation was carried out, followed by thermal annealing under the same conditions as in the case of example 1.

The same results as in example 1 were obtained.

10 The process according to the invention therefore makes it possible to obtain an SOI substrate in which the thin silicon active layer has a uniform surface roughness, that is to say free of the dense zones as would be the case with the processes of the prior art, this being achieved while still having a buried oxide layer of uniform thickness. In addition, the various finishing treatments result in a silicon layer having a low RMS roughness, i.e. around 2 to 3 ångströms (Å) for an AFM microscope scan of 30 µm × 30 µm.

15 Thus, SOI substrates of excellent quality are obtained that are particularly suitable for applications in the fabrication of electronic components for which they are intended.

The invention is also particularly advantageous in the case of SOI substrates having:

20 - a thin upper silicon layer with a thickness of 200 nanometers (nm) or less since, despite this small thickness, dissolution of the buried oxide layer does not take place; and/or

25 - a thin buried oxide (SiO₂) layer having a thickness of 50 nanometers (nm) or less, since, even in this case, the loss of thickness uniformity remains small.

CLAIMS

1. A process for fabricating a substrate of the SOI (silicon on insulator) type, comprising the following steps, consisting in:

5 a) atomic or ionic species are implanted into a silicon substrate called the "donor" substrate, so as to form therein a weakened zone which forms the boundary between a thin layer and the remainder of the donor substrate;

b) this donor substrate is bonded to a substrate called the "receiver" substrate, by molecular adhesion, a layer of silicon oxide being interposed between the two;

10 c) said remainder of the donor substrate is detached, along the weakened zone, so as to obtain an SOI substrate comprising the silicon receiver substrate covered with a silicon dioxide layer and a thin silicon layer;

d) one or more finishing steps are carried out on said thin silicon layer, including at least one long thermal annealing step for a time of at least 10
15 minutes, in a gaseous atmosphere containing hydrogen and/or argon, wherein step a) is carried out by co-implantation of atomic or ionic species and/or wherein step c) is carried out by mainly a mechanical detachment, and wherein said long annealing step or steps are all carried out at a temperature of at least 950°C but not exceeding 1100°C.

20 2. The process as claimed in claim 1, wherein the finishing steps comprise at least one sacrificial oxidation of the free surface of said thin layer followed by a deoxidation so as to eliminate the thickness of material damaged by the detachment step c).

25 3. The process as claimed in claim 1 or 2, wherein step a) consists in carrying out a hydrogen/helium co-implantation.

4. The process as claimed in one of the preceding claims, wherein the detachment of step c) is initiated by a mechanical action on the weakened zone.

5. The process as claimed in claim 1, 2 or 3, wherein the detachment of step c) is carried out by:

30 - applying a heat treatment for further weakening the weakened zone, without initiating thermal detachment from the remainder of the donor substrate, and

- applying a pulse that induces self-sustained detachment from the remainder of the donor substrate.

6. The process as claimed in one of the preceding claims, which consists in forming the silicon oxide layer by thermal oxidation of the donor substrate and/or of the receiver substrate and in bonding the two substrates to each other so that said silicon oxide layer lies at the interface.
- 5 7. The process as claimed in one of the preceding claims, wherein the sacrificial oxidation is carried out under dry or wet conditions, at a temperature between 700°C and 1100°C.
8. The process as claimed in one of the preceding claims, wherein the annealing of step d) is carried out for a maximum time of 15 hours.
- 10 9. The process as claimed in one of the preceding claims, wherein said thin silicon layer has, over its entire extent, an RMS surface roughness of less than 3 ångströms over a scanning area of 30 µm × 30 µm.
10. The process as claimed in one of the preceding claims, wherein the thickness of the thin silicon layer is 200 nanometers or less.
- 15 11. The process as claimed in one of the preceding claims, wherein the thickness of the buried silicon oxide layer is 50 nanometers or less.
12. The process as claimed in one of the preceding claims, wherein the thickness uniformity of the buried silicon oxide layer is 1.8 nm or better.