

PID FILTER CIRCUIT AND FIFO CIRCUIT

Abstract

A PID (Packet Identifier) filter circuit includes a FIFO (First-in, First-out) memory. Filtering may be performed irrespective of the length of the PID and irrespective of whether the position of the PID is fixed in the packet. The circuit includes a comparison value table for storing therein comparison values and a comparator for taking comparison values successively from the comparison value table and for comparing value of the PID in the input packet data with the comparison values on a word by word basis. A FIFO memory stores input packet data. The FIFO memory does not implement a read operation until the input packet data is determined to contain desired data based on its PID. If the input packet data is determined not to contain desired data, any portion of the input packet data already stored in the FIFO is superseded.

Figure 4



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