FLIP CHIP THERMALLY ENHANCED BALL GRID ARRAY

BACKGROUND OF THE INVENTION

This application is related to Attorney Docket #STATS99-002 filed on ----, serial number -----, assigned to a common assignee.

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit (IC) devices, and more particularly, to a method to enhance the heat flow between flip-chip BGA devices and the motherboard. The method of the invention also reduces the length of the signal paths between the Integrated Circuit device and the package terminal.

(2) Description of the Prior Art

High density interconnect technology frequently leads to the fabrication of multilayer structures in order to connect closely spaced integrated circuits with each other. A single substrate serves as an interconnect medium to which multiple chips are connected thereby forming a device package with high packaging density and dense chip wiring. The metal layers that

make up the interconnect network and the via and contact points that establish connections between the interconnect networks are separated by layers of dielectric (such as polyimide) or insulating layers. In the design of the metal interconnects, strict rules must be adhered to in order to avoid problems of package performance and reliability. For instance, the propagation directions of primary signals must typically intersect under 90 degree angles to avoid electrical interference between adjacent lines. It is further required that planarity is maintained throughout the construction of multi-layer chip packages for considerations of photolithography and package reliability. Many of the patterned layers within such a structure form the base for subsequent layers and their lack of planarity can therefore have a multiplying effect on overlying layers.

Quad Flat Packages (QFP) have in the past been used to created surface mounted; high pin count integrated packages with various pin configurations. The electrical connections with these packages are typically established by closely spaced leads that are distributed along the four edges of the flat package. This limits the usefulness of the QFP since a high I/O count cannot be accommodated in this manner. To address this problem, the Ball Grid Array (BGA) package has been created whereby the

I/O points for the package are distributed not only around the periphery of the package but over the complete bottom of the package. The BGA package can therefore support more I/O points making this a more desirable package for high circuit density with high I/O count. The BGA contact points are solder balls that in addition facilitate the process of flow soldering of the package onto a printed circuit board. The solder balls can be mounted in an array configuration and can use 40, 50 and 60 mils spacings in a regular or staggered pattern.

Where circuit density keeps increasing and device features continue to be reduced in size, the effect of the interconnect metal within the package becomes relatively more important to the package performance. Factors that have a negative impact on circuit performance, such as line resistance, parasitic capacitance, RC delay constants, crosstalk and contact resistance have a significant impact on the package design and its limitations. A significant power drop may for instance be introduced along the power and ground buses where the reduction of the interconnect metal does not match the reduction in device features. Low resistance metals (such as copper) are therefore finding wider application in the design of dense semiconductor packages.

Increased I/O combined with increased high demands for high performance IC's has led to the development of Flip Chip packages. Flip chip technology fabricates bumps (typically Pb/Sn solder) on Al pads and interconnects the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package through the shortest paths. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger and to mote sophisticated substrates that accommodate several chips to form larger functional units.

The flip-chip technique, using an area array, has the advantage of achieving the highest density of interconnection to the device and a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and Coefficient of Thermal Expansion (CTE) matching to avoid solder bump fatigue are still challenges. In mounting several packages together, such as surface mounting a ceramic package to a plastic board, the CTE mismatch can cause a large thermal stress on the solder lead joints that can lead to joint breakage caused by solder fatigue from temperature cycling operations.

Prior Art substrate packaging uses ceramic and plastic BGA packaging. Ceramic substrate packaging is expensive and has proven to limit the performance of the overall package. Recent years have seen the emergence of plastic BGA packaging, this packaging has become the main stream design and is frequently used in high volume BGA package fabrication. The plastic substrate BGA package performs satisfactorily when used for low-density flip-chip IC's. If the number of pins emanating from the IC is high, that is in excess of 350 pins, or if the number of pins coming from the IC is less than 350 but the required overall package size is small, or if the chip power dissipation is high (in excess of 4 Watts per chip), the plastic structure becomes complicated and expensive.

In mounting a large number of flip chip packages, the following aspects are key aspects in the design of the interfaces onto which the flip chip dies are mounted:

- interconnect of the flip-chip contact points to the surrounding electrical components
- thermal transmission between the flip-chip and its environment and
- firmness of the overall package that contains the large number of flip-chips.

Interconnecting of the flip-chip contact points to the surrounding electrical components can be accomplished by mounting the flip chip on the surface of a package substrate or by interconnecting the flip-chip to a flex circuit or any other circuit type that contains the interconnect lines. The contact points of the flip-chip IC device make contact with contact points in the circuit, the circuit re-distributes (fan-out) the flip-chip IC device to the contact points. The interconnect lines contained within the circuit are connected to contact balls that are mounted on the device or on the motherboard and form the interface between the final package assembly and the motherboard. It must thereby also be understood that the original contact balls of the flip chip IC device are encased in a material (for instance epoxy) for protection of these balls. The epoxy is therefore encased between the lower surface of the flip-chip IC device and the upper surface of the flex circuit. This epoxy is referred to as underfill since it is filled in under the original flip-chip device.

Firmness of the overall package is assured by mounting the flip-chip devices on the surface of a motherboard, the motherboard provides, in addition to electrical interconnects, the rigidity of the overall package.

Thermal transmission between the flip-chip and its environment is assured by providing a heat sink that is typically attached to the flex circuit.

The invention addresses the aspect of thermal transmission between the flip-chip and its environment. The invention teaches a method that provides excellent heat flow properties whereby the heat that is generated in the die is removed from both the top and the bottom surface of the die. The invention further provides for a reduction in the length of the signal path since signals travel directly from the IC device to the circuit contact balls without having to travel through vias or other transmission paths.

US 5,898,224 (Akram) shows a Flip chip assembly with underlayer and a heat sink and an outer top encapsulant.

US 5,883,430 (Johnson) shows a flip chip encapulated on the bottom and sides, a heat sink on top and an underlayer.

US 5,817,545 (Wang et al.) teaches a process for underfill for a flip chip.

US 5,866,949 (Schueller) teaches a BGA process with an encapsulant.

US 5,896,271 (Jensen et al.) recites a flex substrate with a heat sink on top.

US 5,355,283 (Marrs et al.) provides a method of mounting a ball grid array on a substrate in which vias are formed.

US 5,583,378 (Marrs et al.) provides a ball grid array package that includes a thermal conductor which is a linearly co-extensive outer layer of an interconnect substrate and that forms the outer surface of the ball grid array package.

SUMMARY OF THE INVENTION

A principle objective of the invention is to enhance heat flow between a flip-chip and the environment that is provided for the flip-chip.

It is another objective of the invention to reduce the length of the path that electrical signals must travel between the IC device and the package contact balls.

In accordance with the objectives of the invention a new method is provided for the conduction of heat between a flip-chip and the motherboard and heatsink onto which the flip-chip is mounted. In a flip-chip package of the invention the heatsink is in direct contact with the circuit, the contact balls of the flip chip make contact with the circuit. The flip-chip is attached and reflow is performed thereby attaching the contact balls to the flex circuit. The flip chip is encased in an epoxy compound in a one step process that is in accordance with Attorney Docket #STATS99-002, assigned to a common assignee. The flip-chip is now placed on the motherboard with the contact balls and the underfill facing upwards. The underfill provides direct contact between the flip-chip and the circuit/heatsink. This direct contact significantly increases the heat flow between the flip-chip and the heatsink. The top surface of the flip-chip rests, after the flip-chip has been mounted onto the motherboard, on the motherboard thereby providing maximum heat flow between the top of the flip-chip and the motherboard.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross-section of a flip chip that is attached to a flex circuit and its heat sink.

Fig. 2a shows the cross section of Fig. 1 after the flip chip has been encased in a molding in accordance with Attorney Docket #STATS99-002.

Fig. 2b shows the cross section of Fig. 1 after the flip chip has been attached and underfill has been inserted.

Fig. 2c shows a cross section of the IC device after the flip chip has been attached to the flex circuit and the heat sink assembly, underfill has been inserted and contact balls have been attached.

Fig. 3 shows the package of the flip-chip being matched with the motherboard.

Fig. 4 shows a cross section of the flip-chip mounted on the motherboard after reflow of the underfill of the chip and the motherboard solder balls.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now specifically to Fig. 1, there is shown a cross section of a flip-chip 10 that is mounted on a flex circuit 12 and makes contact with this flex circuit by means of

contact balls 16. The flex circuit 12 is in direct physical contact with the heatsink 14; the heatsink 14 is typically made of copper.

The flex circuit 12 can also be made using a Printed Wiring Board (PWB) or other similar circuit material that can transmit electrical signals.

Fig. 2a shows the cross section of Fig. 1 after the flip chip has been encased in a molding in accordance with Attorney Docket #STATS99-002. Fig. 2a shows a cross section of the flip-chip 10 after the molding compound 18 has been put in place. This molding compound 18 can be an epoxy mold compound. It must be noted that the molding compound 18 is in place not only between the underside of the IC chip 10 and the flex circuit 12 (the underfill) but is also present around the sides of the IC chip 10. This "spill-over" of the mold around the sides of the IC chip is used at a later time to increase the surface of the underfill where this underfill makes contact with the flex circuit. This will become apparent under the description of Fig. 4.

The method of encasing the flip chip in the molding compound 18 is in accordance with Attorney Docket #STATS99-002,

this docket provides a method wherein the Integrated Circuit chip is encased in one processing step including the underfill of the chip. In the invention submitted under Attorney Docket #STATS99-002, the top surface of the BGA chip is in contact with a heat sink while the bottom surface of the BGA chip (the contact balls) makes electrical contact with a substrate (board) through which the lines of electrical interconnect are spread out. The bottom surface of the substrate under Attorney Docket #STATS99-002 has contact balls for connection of the overall package to the surrounding circuitry.

Fig. 2b shows a cross-section of the version of the flip-chip 10 to which underfill 18 has been added. The flex circuit 12 is highlighted, as is the heatsink 14.

Fig. 2c shows a cross section of the IC device after the flip-chip 10 has been attached to the flex circuit 12 and to the heat sink assembly 14. Underfill 18 has been added, the contact balls 24 can then be attached and re-flowed to create the final flip-chip BGA device with the die mounted in the downward position (the die-down BGA device).

Fig. 3 shows a cross section of the flip-chip chip after the flip-chip has been placed on the motherboard 20. Layer 22 is

typically made using copper or tin/lead or any other electrically conductive material and is provided over the surface of the motherboard to affect the reflow of the contact balls 24 of the motherboard 20. Layer 25 is on the same plane as layer 22 and is normally made of the same copper or tin/lead material but this layer is electrically isolated from layer 22. This allows layer 25 to act as a thermal shield and as an EMI shield. The distance X1 that has been highlighted in Fig. 3 is the distance between the surface of flex circuit 12 and layer 22, this distance is used under the following discussion of Fig. 4.

Fig. 4 shows a cross-section after reflow of the motherboard contact balls 24 has been completed. During the process of reflow the contact balls 24 will melt and form a bond with layer 22. During this bonding process the surface 12 will naturally collapse toward layer 22. During this collapse, the distance X_1 shown in Fig. 3 will be reduced to a smaller distance X_2 and will allow the flip chip IC to come into contact with the layer 25. Since the flip-chip IC is now in direct contact with layer 25, the heat exchange between the flip chip and the motherboard 10 has been increased.

It is further clear from Fig. 4 that the flip-chip is in maximum (possible) physical contact with the motherboard thereby providing for maximum heat interchange between the flip-chip 10 and the motherboard 20. It is further possible to allow the distance X_1 and X_2 to remain the same after reflow and to therefore prevent the die from forming contact with layer 25.

Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and modifications which fall within the scope of the appended claims and equivalents thereof.

What is claimed is:

1. A method of packaging Integrated Circuit devices, comprising:

creating a first intermediary IC device package;

creating a second intermediary IC device package; and

creating a final IC device package.



2. The method of claim 1 wherein said creating first intermediary IC device package is:

providing an Integrated Circuit device said IC having been provided with external contact points;

providing a heat sink with an attached flexible circuit or other circuit for said Integrated Circuit device;

bringing said heatsink with said flex circuit attached in close physical contact with said IC device; and

attaching and reflowing said Integrated Circuit device to said flex circuit and heat sink assembly.

3. The method of claim 2 wherein said heat sink contains a relatively large upper and a relatively large lower surface both surfaces being essentially of equal size and both surface being essentially parallel to each other.

4. The method of claim 2 wherein said heatsink is replaced by a surface of geometric dimensions that are equal to the geometric dimensions of said heatsink whereby said surface does not have the heat dissipating requirements or characteristics of a typical heatsink.



5. The method of claim 2 wherein said flex circuit contains an relatively large upper and a relatively large lower surface both surfaces being essentially of equal size and both surface being essentially parallel to each other whereby one surface of said flex circuit contains electrical contact points while the other surface of said flex circuit is electrically insolated.

6. The method of claim 1 wherein said creating a second intermediary IC package is:
providing said first intermediary IC device package; and
encasing the IC device of said first intermediary IC package in a molding compound thereby including the underfill for said Integrated Circuit device.

7. The method of claim 6 wherein said encasing the IC device of said first intermediary IC package in a molding compound is:
creating a cavity;
inserting said Integrated Circuit device into said cavity; and

injecting a molding compound into said cavity.

8. The method of claim 7 wherein said creating a cavity is:

creating a surface 1 that is parallel with the plane of said flex circuit of said first intermediary IC device package;

creating four planer spacer surfaces that separate said flex circuit from said surface that is parallel with the plane of said flex circuit by a measurable amount said amount to be selected such that the contact points of said IC device make contact with said flex circuit while the top surface of said IC device makes contact with said surface 1 that is parallel with the plane of said flex circuit; and

forming a cubic cavity whereby said surface 1 and said flex circuit form opposite walls of said cavity while said four planer spacers form two sets of two opposing walls of said cavity whereby the two walls that make up each of these sets of opposing walls have the same geometric dimensions whereby furthermore the planes of said heat sink is parallel with the plane of said substrate while at the same time the two planes of each of the two sets of planar spacers that belong to the same set are parallel.

9. The method of claim 8 wherein the cross section of said cavity in a plane that is parallel to the plane of the largest surfaces of said heat sink is smaller than the cross section of said heat sink by a measurable amount and wherein the geometric center of said cavity is located on the line that is drawn through the geometric center of said heat sink whereby said line is perpendicular to the plane of largest surfaces of said heatsink.



10. The method of claim 1 wherein said creating a final IC device package is:

providing a motherboard for said second intermediary IC device package;

depositing a wetting or adhesion enhancer over the surface of said motherboard;

providing contact balls for the motherboard said contact balls to establish electrical contact between said flex circuit and said motherboard;

placing said contact balls on the surface of said motherboard;

placing said second intermediary Integrated Circuit device package on the surface of a motherboard thereby facing the Integrated Circuit device contact points upwards; and

reflowing said assemblage of said Integrated Circuit package, said contact balls and said motherboard thereby creating the final BGA assembly.



11. The method of claim 10 wherein said contact balls for the motherboard have a diameter that is essentially the same as the distance between the flex circuit and the surface 1 of the cavity used for the encasing the IC device of said first intermediary IC package.

12. The method of claim 10 wherein said motherboard contains:
an upper surface;
electrical contact points in said upper surface therewith forming motherboard contact points said contact points being provided as a means to make electrical contact with said contact points of said flex circuit; and
a network of conducting interconnect lines that interconnects said contact points with electrical circuits of which said IC device forms a functional part said network to be contained in one or more planes within said motherboard.

13. The method of claim 1 wherein said IC device is selected from the group consisting of Ball Grid Array (BGA), Land Grid Array (LGA) and Pin Grid Array (PGA), Chip Scale Packaging (CSP) and Quad Flat Pack (QFP) devices.



14. The method of claim 2 wherein said flex circuit contains a relatively large upper and a relatively large lower surface whereby both surfaces are essentially parallel to each other whereby furthermore one surface of said flex circuit contains electrical contact points while the other or both surfaces of said flex circuit are electrically connected to said heat sink in pre-determined locations and electrically isolated from said heat sink in pre-determined locations.