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DIGITAL SIGNAL DEMODULATOR

This invention relates to digital signal demodulators such as can be used, in a television receiver in which the detected video signal is processed by digital circuitry, to provide filtered demodulated color signals.

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For reasons relating to factors such as bandwidth, speed and complexity, television signal processing circuits are conventionally constructed in analog form. However, recent advances in analog to digital converter speed and large scale integrated circuit technology have made the implementation of television circuits using digital technology realizable. Due to bandwidth requirements, television intermediate frequency circuitry is yet constrained to construction in analog form, but baseband video signal processing is susceptible to digital techniques.

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In a digital baseband receiver, the detected video signal is converted to a digital signal by an analog to digital converter, which samples the video signal at a rate greater than or equal to the Nyquist sampling rate for the video signal band (e.g., the NTSC video signal of 4.2 MHz must be sampled at a frequency of at least 8.4 MHz). Sampling an analog signal at or above the Nyquist sampling rate prevents loss of information due to the sampling process. The digitized video signal is then separated into luminance and chrominance components by digital filtering, such as digital comb filtering. The luminance and chrominance components may then be processed in separate digital signal paths, converted back to analog form, and recombined in a matrix to produce red (R), green (G) and blue (B) signals for the kinescope in the receiver.

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The chrominance component of the composite video signal comprises a quadrature amplitude modulated, suppressed subcarrier signal. Two color representative signals (e.g., I and Q in an NTSC video signal) amplitude modulate the quadrature phases of the subcarrier. (The

1 subcarrier has a frequency of 3.58 MHz in an NTSC video
signal). A phase reference is also transmitted in the
composite video signal and is a burst of subcarrier
5 having a predetermined phase (e.g., $-(B-Y)$ in an NTSC
video signal). Thus, to derive R, G and B information
from the chrominance component, the component must be
both demodulated and filtered.

10 In the chrominance channel, the digital color
signals are generally amplified and bandpass filtered or
peaked prior to demodulation. The color signals are then
demodulated at selected phase angles of the color
subcarrier signal to produce either I and Q color mixture
signals or R-Y and B-Y color mixture (difference)
15 signals. The demodulated color mixture signals are then
filtered to remove high frequency noise from the
signals. In the instance of the I and Q signals, the I
signal has a bandwidth of 1.5 MHz and the Q signal has a
bandwidth of 0.5 MHz. The color difference signals both
20 have bandwidths of 0.5 MHz. The color difference signals
can then be combined to produce the G-Y difference
signal, and all three difference signals may then be
converted to analog form, filtered to remove sampling
frequency components, and matrixed with the luminance
signal (Y) to produce the R, G and B signals. In the
25 case of the filtered I and Q signals, these signals can
be converted to analog form, filtered to remove sampling
frequency components, and matrixed with the Y signal to
produce the R, G and B signals.

30 In accordance with the principles of the
present invention, an arrangement is provided for
demodulating and filtering digital information-bearing
signals. This arrangement is in a system including a
source of information-bearing digital signals to be
demodulated and filtered, and a source of reference
35 signals which have a predetermined phase relationship
with the information-bearing signals. The arrangement
includes a means responsive to the reference signals for
producing a clock signal with a predetermined phase
relationship to the reference signals. The arrangement

1 also includes a digital filter with inputs responsive to
the digital signals and the clock signal, which develops
the demodulated and filtered information signals at its
output.

5 In one embodiment of the present invention, a
digital finite impulse response (FIR) filter arrangement
is provided which both demodulates and filters the color
mixture signals in a television receiver. Such a filter
10 can be either an input tap weighted, or an output tap
weighted arrangement. In this embodiment of the
invention, an output tap weighted FIR is provided wherein
samples of the separated digital chrominance signal are
15 clocked into first and second registers such that the
first register contains samples of a first color mixture
signal and the second register contains samples of a
second color mixture signal. Output taps are connected
between the outputs of various ones of the stages of the
first and second registers and weighting function
20 circuits. The weighting function circuits associated
with each register are in turn coupled to respective
ladder networks of adders, which combine the weighted
signal samples so as to exhibit, at an output stage
adder, a lowpass response characteristic which is
25 appropriate for the respective color mixture signal. The
two digital registers are aligned in time in accordance
with their respective impulse response characteristic to
produce filtered color mixture signals in a proper timed
relationship.

30 The clock signals which load the samples into
the registers are in a predetermined time relationship.
In accordance with a further aspect of the present
invention, the clock signals are derived from a phase
locked loop signal which produces a signal aligned in
phase to the color burst signal. The phase locked loop
35 signal may be controllably shifted in phase by a tint
control circuit, then phase-shifted by a given delay to
align the signal with the desired nominal demodulation
angle. The phase-shifted signal is increased in
frequency to a multiple of the subcarrier signal, thereby

1 producing a sampling signal for the analog to digital
converter. The multiple subcarrier frequency signal has
multiple cycles in the same period as one cycle of the
phase-shifted signal. Certain cycles of the multiple
5 subcarrier frequency signal are gated out to the digital
filter arrangement, at the color subcarrier frequency, to
be used as the clock signals for the two color mixture
signal registers.

In the drawings:

10 FIGURE 1 illustrates in block diagram form a
portion of a television receiver including a digital
baseband signal processor constructed in accordance with
the principles of the present invention;

15 FIGURE 2 illustrates, partially in block
diagram form and partially in schematic diagram form, a
clock generator arrangement suitable for use in the
television receiver of FIGURE 1 and constructed in
accordance with the principles of the present invention;

20 FIGURE 3 illustrates, in schematic diagram
form, I and Q clock logic circuitry suitable for use in
the clock generator of FIGURE 2;

25 FIGURE 4 illustrates, in block diagram form, a
digital color signal demodulator and filter constructed
in accordance with the principles of the present
invention;

FIGURE 5 illustrates a color demodulator phasor
diagram;

FIGURE 6 shows waveforms illustrating the
operation of the arrangements of FIGURES 2-4;

30 FIGURE 7 illustrates, in block diagram form,
the weighting function and adder ladder network of the Q
filter of FIGURE 4;

35 FIGURE 8 illustrates, in block diagram form,
the weighting function and adder ladder network of the I
filter of FIGURE 4;

FIGURE 9 illustrates, in block diagram form, a
more detailed arrangement of the signal averaging
circuits of FIGURE 4;

1 FIGURE 10 illustrates the amplitude versus
frequency response of the Q filter of FIGURE 4; and
 FIGURE 11 illustrates the amplitude versus
frequency response of the I filter of FIGURE 4.

5 In FIGURE 1, a television signal is received by
an antenna 10 and successively processed by a tuner 12,
intermediate frequency circuits 14, and a video detector
16, which are constructed in a conventional manner. The
detected video signal at the output of the detector 16 is
10 applied to the input of an analog to digital (A/D)
converter 20. The A/D converter 20 samples the video
signal at a rate equal to four times the color subcarrier
frequency ($4f_{sc}$), and produces digital samples of the
video signal at this rate. Each digital sample, or word,
15 may comprise, for example, eight bits produced in
parallel. In an eight-bit system, the analog video
signal will be quantized to one of two-hundred and
fifty-six discrete levels. The $4f_{sc}$ sampling clock for
the A/D converter 20 is developed by a clock generator
20 22, which produces the signal in phase and frequency
synchronism with the color burst signal of the analog
video signal provided by the video detector 16.

 The digitized video signal produced by the A/D
converter 20 is applied to an input of a digital comb
25 filter 24, which may be constructed as shown in the
article "Digital Television Image Enhancement" by
John P. Rossi, 84 SMPTE at 545-51 (1974). The comb
filter 24 produces a separated luminance signal, Y, which
is applied to a luminance signal processor 26. The
30 luminance processor 26 is responsive to a viewer
controlled contrast control signal and produces a
processed luminance signal, which is applied to the
inputs of a digital to analog (D/A) converter 28. The
luminance signal, now in analog form, is filtered by a
35 lowpass filter 30 to remove sampling frequency
components, and a processed luminance signal Y' is
applied to one input of a matrix arrangement 60.

1 The comb filter 24 also produces a separated
chrominance signal C, which is applied to the input of a
chroma amplifier 32. The chroma amplifier 32 amplifies
the chrominance signal in response to a viewer controlled
5 color saturation control signal, and applies the
amplified chrominance signal to the input of a digital
chroma peaker 34. The chroma peaker 34 is a digital
filter which modifies the response characteristic
exhibited by the chrominance signal at this point to
10 compensate for the response characteristic of the
intermediate frequency circuits 14. The intermediate
frequency circuits generally locate the color subcarrier
frequency on the lower frequency slope of the I.F.
passband, causing the color sidebands to exhibit a
15 rolloff of 6dB per octave. The chroma peaker 34
compensates for this rolloff to cause the chrominance
signal to exhibit an essentially flat amplitude versus
frequency response. If the I.F. circuits 14 are designed
to provide an essentially flat amplitude versus frequency
20 response for color signals, the chroma peaker 34 may be
replaced by a chroma bandpass filter with a response
characteristic located about the color subcarrier
frequency.

25 The peaked or bandpassed chrominance signals
are then applied to an input of an I-Q demodulator 40.
The I-Q demodulator demodulates the chrominance signal
into its baseband I and Q signal components. The
demodulated I signal is applied to an input of an I
finite impulse response (FIR) filter 42, and the
30 demodulated Q signal is applied to an input of a Q FIR
filter 44. The I filter has a passband extending from
zero to approximately 1.5 MHz, and the Q filter has a
passband extending from zero to 0.5 MHz. The I and Q
filters remove high frequency noise contained in the
35 color signals by reason of the broad bandwidth of the
preceding processing circuitry.

1 The filtered I and Q signals are converted to
analog signals by D/A converters 46 and 48, respectively,
and the analog signals are then filtered by lowpass
filters 50 and 52 to remove sampling frequency
5 components. The resultant I' and Q' signals are applied
to the matrix arrangement 60, where they are matrixed
with the Y' signal to produce R, G and B output signals.
The matrix arrangement may comprise, for example, a
resistive signal combining matrix.

10 The clock generator 22 of FIGURE 1 is shown in
further detail in FIGURE 2. The video detector 16
applies the detected video signal to a synchronization
signal separator 200 and a chroma bandpass filter 202.
Separated sync pulses and signals of the chrominance
15 frequency are applied to inputs of a gating circuit 204,
which gates the color burst signal provided by the chroma
bandpass filter 202 to a phase detector 212. The phase
detector 212 is coupled in a phase locked loop²¹⁰ with a
filter 214 and a voltage controlled oscillator 216 to
20 cause the oscillator 216 to produce a reference signal at
the color subcarrier frequency which is aligned in phase
with the color burst signal.

 The color reference signal is applied to a tint
control circuit 220, which is capable of shifting the
25 phase of the reference signal in accordance with the
setting of a viewer controlled tint control 222. The
reference signal, as adjusted for tint, is applied to a
squaring circuit 224, which includes a capacitor 226 and
a comparator 228. The capacitor A.C. couples the
30 reference signal to one input of the comparator 228 which
swings the signal about a reference voltage level
(ground). Since the second input of the comparator is
coupled to ground, the comparator will produce a
square-wave replica of the reference signal.

35 The output of the squaring circuit 224 is
coupled to the input of a delay element 230, and to the
input of control logic 250. The delay element 230 shifts
the phase of the reference signal by 57° for demodulation

1 of the color signal along the I and Q axes. The
phase-shifted reference signal is then applied to the
input of a phase detector 242 of a phase-locked loop
240. The phase-locked loop 240 additionally includes a
5 filter 244, a voltage-controlled oscillator 246, and a
divider 248. The voltage-controlled oscillator 246 will
thus produce a sampling signal at a frequency of four
times the reference signal frequency ($4f_{sc}$) which is
aligned in phase with the phase of the reference signal
10 applied to the phase detector 242. In the NTSC system,
the reference signal has a frequency of 3.58 MHz, and
thus the sampling signal $4f_{sc}$ has a frequency of 14.32
MHz. The sampling signal $4f_{sc}$ is applied to the A/D
converter 20 as shown in FIGURE 1, and is also applied to
15 inputs of AND gates 252 and 254 as shown in FIGURE 2.
Outputs from the control logic 250 are also coupled to
inputs of AND gates 252 and 254 to gate selected ones of
the sampling signal pulses to the I and Q FIR filters 42
and 44.

20 The control logic 250 and its connections to
AND Gates 252 and 254 are shown in further detail in
FIGURE 3. A "D" type flip-flop 256 has its D (data)
input coupled to a logical "1" voltage source, and its
C (clock) input is coupled to receive the square wave
25 3.58 MHz reference signal produced by the squaring
circuit 224. The Q output of the flip-flop 256 is
coupled to an input of the AND gate 252.

30 The output of AND gate 252 is coupled to the
clock input of a JK flip-flop 258. The J input of
flip-flop 258 is coupled to the logical "1" voltage
source, and its K input is coupled to a logical "0"
voltage source. The Q output of flip-flop 258 is coupled
to an input of the AND gate 254, and the $\bar{Q}$ output of the
flip-flop is coupled to the reset (R) input of the "D"
35 type flip-flop 256.

The output of AND gate 254 is coupled to the
clock input of a second JK flip-flop 259. The J input of
flip-flop 259 is coupled to the logical "1" voltage
source, and its K input is coupled to the logical "0"

1 voltage source. The $\bar{Q}$ output of flip-flop 259 is coupled
to the reset (R) inputs of the JK flip-flops 258 and 259.

5 The operation of the clock generating
arrangement of FIGURES 2 and 3 is explained by referring
to the phasor diagram of FIGURE 5 and the waveforms of
FIGURE 6. The phase locked loop 210 produces a reference
signal f_{sc} locked in phase and frequency with the color
burst signal as represented by waveform 260 of FIGURE
6a. FIGURE 5 shows that the color difference signals
10 $-(B-Y)$ and $B-Y$ may be recovered by demodulating the
chrominance signal at 0° to 180° with respect to the
burst-locked reference signal f_{sc} . The $R-Y$ and $-(R-Y)$
color difference signals may be recovered by demodulating
the chrominance signal at $+90^\circ$ and -90° with respect to
15 the phase of the reference signal f_{sc} . When the phase of
the reference signal f_{sc} is shifted by 57° as by delay
element 230, the I and $-I$ color mixture signals may be
recovered by demodulating the chrominance signal at 0°
and 180° with respect to this phase-shifted reference
20 signal. Similarly, the Q and $-Q$ color mixture signals
may be recovered by demodulating the chrominance signal
at $+90^\circ$ and -90° with respect to the phase-shifted
reference signal. These demodulation phase angles are
indicated on the burst-locked reference signal f_{sc} of
25 FIGURE 6a.

For purposes of the present example, it will be
assumed that the tint control 222 is at a setting such
that the reference signal f_{sc} undergoes no phase shift in
the tint circuit 220. The f_{sc} reference signal is squared
30 by squaring circuit 224 to produce a waveform 266 as
shown in FIGURE 6d, and indicated in FIGURE 2 by the
circled letter "d". The square wave reference signal 266
is applied to the delay element 230, which produces a
phase-shifted square wave 268 as shown in FIGURE 6e and
35 indicated by the circled "e" in FIGURE 2. The
phase-locked loop 240 will produce a 14.32 MHz sampling
signal as shown in FIGURE 6c and indicated in FIGURE 2 by
the circled "c". Since the reference signal was
phase-shifted to the I axis by delay element 230, the

1 pulses of the $4f_{sc}$ sampling signal will be aligned to
sample the I, Q, -I and -Q signals as shown in FIGURE 6c
with reference to the waveform 260 of FIGURE 6a. If it
5 is desired to demodulate the color difference signals,
the delay element 230 can be deleted from the arrangement
of FIGURE 2, causing the $4f_{sc}$ sampling signal to be
phased for recovery of the -(B-Y), R-Y, B-Y, and (-R-Y)
signals, as shown in FIGURE 6b.

10 The f_{sc} reference signal 266 of FIGURE 6d is
applied to the C input of "D" type flip-flop 256 of
FIGURE 3, causing this flip-flop to "set" upon the
occurrence of a rising edge of waveform 266, as shown by
pulse 270 in FIGURE 6f. When the I pulse of waveform 264
15 occurs, both inputs of AND gate 252 are enabled, and the
AND gate produces an output pulse for the duration of the
I pulse, as indicated by the shaded area of pulse 270.
At the end of the I pulse, the I clock pulse terminates,
which clocks flip-flop 258 to the "set condition". As
20 flip-flop 258 sets, its Q output goes "high", as shown by
pulse 272 in FIGURE 6g. Simultaneously, the $\bar{Q}$ output of
flip-flop 258 goes low, resetting flip-flop 256, as
indicated by the termination of pulse 270 in FIGURE 6f.
When the Q pulse of waveform 264 occurs, both inputs of
AND gate 254 are enabled, which produces a Q clock pulse
25 for the duration of the Q pulse, as indicated by the
shaded area of pulse 272. When the Q pulse of waveform
264 terminates, the Q clock pulse goes low, setting
flip-flop 259 and causing its $\bar{Q}$ output to go low, as
shown by pulse 274 in FIGURE 6h. The low-going $\bar{Q}$ output
30 of flip-flop 259 resets flip-flops 258 and 259, as
indicated by the termination of pulses 272 and 274 in
FIGURES 6g and 6h. Thus, AND gates 252 and 254 produce
pulses at the frequency of the f_{sc} reference signal and
at the proper times for recovering the I and Q signals
35 from the digital chrominance signal in the arrangement of
FIGURE 1. The clock generating arrangement is described
in further detail in our co-filed application ^{No. 8223986} ~~(RCA 76736)~~
based on U.S. application number 298,270, entitled "CLOCK
GENERATOR FOR A DIGITAL COLOR TELEVISION SIGNAL RECEIVER".

1 The I-Q demodulator 40, the I FIR filter 42,
and the Q FIR filter 44 of FIGURE 1 are constructed in
accordance with the principles of the present invention
as shown in FIGURES 4, 7 and 8. Referring to FIGURE 4,
5 the eight-bit chrominance signal produced by the digital
chroma peaker 34 is applied in parallel to two shift
registers 420 and 440 which are capable of shifting
eight-bit words. (In the remaining FIGURES, the broad
10 stripe connections represent multiple parallel lines of
digital information.)

 The eight-bit words of the chrominance signal
are clocked into the first stage r_{I1} of the I register
420 by the I clock, which also shifts the words through
the register 420 to the last stage r_{I9} . A new data word
15 is loaded in the first stage r_{I1} during every I pulse of
FIGURE 6c, which occur at a phase angle of 57° with
respect to the color burst signal of FIGURE 6a. The I
data words are thus clocked through the register at a
3.58 MHz rate.

20 The shift register stages r_{I1} through r_{I9} are
tapped to provide eight-bit output words for weighting
function circuits shown at 422. Each of the weighting
function circuits multiplies the tapped shift register
signal by weighting coefficient shown in the respective
25 block in FIGURE 4. The weighted tap signals are then
applied to a summing network 424, which combines the
weighted tap signals to produce a filtered I signal. The
filtered I signal is then applied to the input of a
signal averaging circuit 426, which will be described
30 subsequently. The signal averaging circuit improves the
signal to noise ratio of the applied signal, and its
output is coupled to the input of the D/A converter 46,
which reproduces the I signal in analog form.

35 In a similar manner, Q signal samples are
clocked into and through the Q register 440 at a 3.58 MHz
rate by the Q clock. Stages r_{Q1} and r_{Q2} of this register
provide delay prior to tapped stages r_{Q3} through r_{Q7} .
Output signals from stages r_{Q3} through r_{Q7} are applied to
weighting function circuits shown at 442, and weighted

1 tap signals are then combined in a summing network 444.
The filtered Q signal at the output of the summing
network 444 is applied to a second signal averaging
circuit 446, the output of which is coupled to the input
5 of D/A converter 48 to convert the filtered Q signal to
an analog signal.

The digital I and Q filters of FIGURE 4 perform
I and Q demodulation due to the clocking of registers 420
and 440 by the I and Q clocks, respectively, which shift
10 I signal samples into the I register 420 and Q signal
samples into the Q register 440. Since the
registers are both clocked at a 3.58 MHz rate, the two
filters exhibit equal group delays for proper phasing of
the demodulated signals, and since the values of the
15 weighting functions are symmetrical about the center taps
of the two filters, the filters will exhibit linear phase
characteristics. The I FIR filter 42 attenuates
frequencies above the 1.5 MHz upper frequency of the I
signal passband, to eliminate high frequency noise, such
20 as white noise, from the color mixture signal.
Similarly, the Q FIR filter 44 eliminates noise above the
0.5 MHz upper frequency of the Q signal. In the
illustrated embodiment, the I FIR filter has nine
weighting function circuits 422, and the Q FIR filter has
25 five weighting function circuits 442. The number of
weighting function circuits shown has been found to
provide desirable response characteristics for the I and
Q filters using inverse power of two coefficients without
excessive circuitry requirements. Lesser numbers of
30 weighting function circuits was found to provide
unsatisfactory response characteristics and greater
number of weighting function circuits were found not to
provide a significant improvement in performance.

35 In addition, the proper phase relationship of
the demodulated I and Q signals is maintained by aligning
the FIR filters in time in accordance with their impulse
response characteristics. The impulse responses of the
two FIR filters are centered about their center taps:
tapped stage τ_{I5} of the I filter 42 and tapped stage τ_{Q5}

1 of the Q filter 44. In order to align these taps in
time, stages τ_{Q1} and τ_{Q2} are coupled ahead of tapped Q
filter stages τ_{Q3} through τ_{Q7} .

5 The substantially equal group delays of the
analog I and Q signals produced by D/A converters 46 and
48 are maintained by constructing lowpass filters 50 and
52 to have substantially equal response characteristics.
These filters are used to eliminate clock signal
frequencies from the I and Q signals, and therefore must
10 attenuate signals of the 3.58 MHz I and Q clock signal
frequency. In addition, it is desirable to attenuate the
first subharmonic frequency of the clock frequency, of
1.79 MHz. Thus, filters 50 and 52 are each designed to
have a 3 dB point in the vicinity of 1.5 to 1.6 MHz.

15 The weighting function circuits 442 and the
summing network 444 of the Q FIR filter of FIGURE 4 are
shown in greater detail in FIGURE 7. The weighting
function circuits and summing network are configured in a
shift and add adder tree arrangement. The eight bit
20 lines from the shift register 440 are identified as
 $2^7 \dots 2^0$, from most significant bit (MSB) to least
significant bit (LSB). The weighting function values of
circuits 442 in FIGURE 4 are all seen to be multiples of
inverse powers of two. Thus, the 8/64 weight, for
25 instance, may be produced by shifting the eight-bit word
from the shift register to the right by three places, so
that the 2^7 input is in the 2^4 output bit location, the
 2^6 input bit is in the 2^3 output bit location, etc.
Furthermore, shift registers are not needed to perform
30 this shift. In practice, the same effect is achieved in
the arrangement of FIGURE 7 by applying the 2^7 bit of the
output of stage τ_{Q3} to the 2^4 bit input of an adder 470,
the 2^6 bit to the 2^3 bit input of the adder, etc. The
weighting function circuit 460 in FIGURE 7 connotes this
35 coupling, as do weighting function circuits 461, 462, and
463, which couple the outputs of stages τ_{Q4} , τ_{Q6} , and τ_{Q7}
to the inputs of adders 470 and 472.

In a similar manner, weighting function
circuits 464 and 465 divide signals from stages τ_{Q4} and

1 r_{Q6} by 16/64 by shifting the signals two places to the
right in their coupling to the inputs of an adder 474.
Weighting function circuit 466 divides the signal from
stage r_{Q5} by 32/64 by shifting the signal to the right by
5 one place in coupling it to an adder 478.

The adders 470, 472, 474 and 478 receive
weighted words scaled so that the LSB has a value of
 2^{-1} . Bits of lesser significance are not used.

10 It is also seen in FIGURE 4 that the signals
from stages r_{Q4} and r_{Q6} are weighted by 24/64. This
weight is achieved by dividing the outputs of stages r_{Q4}
and r_{Q6} by 8/64 and 16/64 by circuits 461, 464, 462, and
465, respectively. The addition of these two weighted
15 signals in the adder tree produces signal components
weighted by 24/64 in the final output.

In the adder tree, outputs of adders 470 and
472 are coupled to inputs of an adder 476, the output of
which is coupled to an input of an adder 480. The
20 outputs of adder 474 is coupled to a second input of
adder 478, the output of which is coupled to a second
input of adder 480. A ten bit Q signal ($2^8 \dots 2^{-1}$) is
used by the signal averaging circuit 426, which is
constructed to receive eight bit data words. The Q FIR
25 filter, when constructed as shown in FIGURE 4 and 7,
exhibits a response characteristic as shown in FIGURE
10. The characteristic is seen to exhibit a secondary
response between approximately 1.25 and 1.6 MHz, which
will contain noise, but is attenuated by at least 30 dB
relative to the Q signal in the band of 0 to 0.5 MHz.
30 The noise components will be even further reduced by the
signal averaging circuit 446.

The weighting function circuits 422 and the
summing network 424 of the I FIR filter of FIGURE 4 are
shown in FIGURE 8 in further detail. As in the
35 arrangement of FIGURE 7, the weighting functions used are
all multiples of inverse powers of two, permitting the
use of the shift and add technique for signal weighting.
Signal weighting is again accomplished by applying
selected most significant bits of the data words from the

1 shift register 420 to the first rank of adders in an
adder tree arrangement, in which the LSB has a value of
2⁻¹.

5 In FIGURE 8, data words from stages r_{I1} and r_{I2}
are weighted by 1/64 by applying the three most
significant bits of these words to the inputs of an adder
540, as indicated by weighting function blocks 502 and
504. Blocks 506 and 508 indicate that similar weights
10 are applied to data words from stages r_{I8} and r_{I9} , which
are applied to inputs of an adder 541. Similarly, data
words from stages r_{I3} and r_{I7} are weighted by 1/64 as
indicated by blocks 518 and 520, and are applied to
inputs of an adder 544.

15 Data words from stages r_{I2} and r_{I8} are
weighted by 2/64 by applying the four most significant
bits of these words to inputs of an adder 542. Data
words from stages r_{I4} and r_{I6} are also weighted by 2/64
and applied to inputs of an adder 545.

20 Data words from stages r_{I3} and r_{I7} are weighted
by 8/64 by applying the six most significant bits of
words from these stages to the inputs of an adder 543.
Data words from stages r_{I4} and r_{I6} are weighted by 16/64
by applying the seven most significant bits of words from
these stages to the inputs of an adder 546. Finally,
25 data words from stages r_{I5} are weighted by 32/64 and
16/64 by applying the eight and seven most significant
bits, respectively, to inputs of an adder 547. The adder
547 will then produce data words of stage r_{I5} weighted by
48/64, which is the desired weight for words of this
30 stage.

35 The outputs of adders 540 and 541 are coupled
to inputs of an adder 550, the output of which is coupled
to an input of an adder 562. The output of adder 542 is
coupled to an input of an adder 552. The outputs of
adders 544 and 545 are coupled to inputs of an adder
554. The outputs of adders 546 and 547 are coupled to
inputs of an adder 556, the output of which is coupled to
an input of an adder 564.

1 In FIGURE 4, it is seen that data words from
stages τ_{I3} and τ_{I7} are weighted by minus $9/64$. The minus
sign is produced by subtractively combining weighted data
5 from these stages with the other data words in FIGURE 8.
As in ordinary arithmetic, digital words may be
subtractively combined by additively combining the
negative of the digital word. Digital words are negated
by an operation called two's complementing. To two's
10 complement a digital word the bits of that digital word
are inverted, and a binary '1' added to the result.
Words from these two taps are weighted by $8/64$ at the
output of adder 543. These words are then subtractively
combined with weighted data from adder 542 in adder 552.
15 Output data of adder 543 is two's complemented for
subtraction by, first, inverting all bits of the data in
inverting circuit 534, then adding a "one" to the
inverted data by applying a logical "1" to the carry in
input of adder 552. The output of adder 552, including
20 two terms weighted by $-(8/64)$, is coupled to a second
input of adder 564.

Similarly, the output data produced by adder
554 is subtractively combined with the rest of the data
in the adder tree by inverting all bits in an inverting
circuit 536, then applying the inverted data together
25 with a carry in logical "1" to a second input of adder
562. The outputs of adders 562 and 564 are coupled to
inputs of an adder 560, which produces the filtered I
signal. In adder 560, weighted tap values of $-(8/64)$
coupled from stages τ_{I3} and τ_{I7} by way of adder 564 are
30 combined with weighted values of $-(1/64)$ from the same
stages by way of adder 562 to produce the desired
weighted value of $-(9/64)$ of the data from stages τ_{I3} and
 τ_{I7} in the final output. Similarly, the final adder 560
combines weighted values of $-(2/64)$ from stages τ_{I4} and
35 τ_{I6} with weighted values of $(16/64)$ from these stages to
produce the desired term of $(14/64)$ of data from stages
 τ_{I4} and τ_{I6} in the final output. The frequency response
characteristic of the I filter is shown in FIGURE 11.

1 It has been found that a certain amount of time
is required for the I and Q FIR filters to settle between
the moment that the I and Q clocks shift a new data array
into the tapped stages of shift registers 420 and 440
5 (FIGURE 4), and the moment that stable output signals are
produced at the outputs of adders 480 (FIGURE 7) and 560
(FIGURE 8). This settling time is a function of the
number of levels, or ranks, of adders in the trees and
the propagation delay times of the adders. In addition,
10 different signal paths from the shift registers to the
filter outputs have different delays. For instance, in
the weighting function circuit and adder ladder of the Q
filter of FIGURE 7, data words from r_{Q5} pass through only
two adders (478 and 480) on their path to the filter
15 output, whereas all other signals must pass through three
adders. During the time required for the tapped signals
to pass to the outputs, the filter output signals are
unreliable and can produce ripple in the output signals
as the filters settle. To prevent this ripple from
20 disturbing the output signal, signal averaging circuits
426 and 446 (FIGURE 4) are used at the filter outputs to
latch the output signals during stable time periods, and
to average consecutive signals to provide a 3 dB
improvement in the signal-to-noise ratio of the I and Q
25 signals.

 Signal averaging circuit 446 is shown in
greater detail in FIGURE 9. Signal averaging circuit 426
is constructed in a similar manner. In FIGURE 9, the
final adder 480 of the Q FIR filter has its output
30 coupled to the input of an eight-bit latch or storage
register 600. The output of eight-bit latch 600 is
coupled to the input of a second eight-bit latch 602, and
to an adder 604. The output of latch 602 is coupled to a
second input of adder 604. Latches 600 and 602 are
35 clocked by the filter clock, in this case, the Q clock.

 In operation, the Q clock transition that
shifts the Q data words through the shift register 440
also latches the filtered Q signal into the latch 600.

1 The new shift register data now begins to pass through
the adder tree, but the output is now isolated because
the latch has stored the previous filtered Q signal
value. As the latch 600 is storing this Q signal, the Q
5 signal previously stored in latch 600 is simultaneously
latched into latch 602. The latches now contain
consecutive Q signal values, which are applied to adder
604. The latches apply eight-bit words ($2^8 \dots 2^1$) to
adder 604, which adds the two words to produce a nine-bit
10 sum word. Only the eight most significant bits of the
sum word ($2^9 \dots 2^2$) are passed on to the D/A converter,
effectively averaging the latched Q words. A three dB
signal-to-noise improvement is provided by this signal
averaging.

15 By use of the signal averaging circuit, the Q
filter adder tree has almost a full cycle of the 3.58 MHz
Q clock to settle before its output is again sampled and
latched into latch 600. This substantial settling time
period permits the use of relatively slow logic in the
20 adder tree. Moreover, it is seen that only a single
clocking signal, the Q clock, is needed to clock both the
shift register and the signal averaging circuit. The
signal averaging circuits are described in greater detail
in United States patent application number 298,255,
25 entitled "DIGITAL VIDEO SIGNAL PROCESSING FILTERS WITH
SIGNAL-TO-NOISE ENHANCEMENT".

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CLAIMS

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1. In a television receiver, including a source of color reference signal, and a source of digital chrominance signals, a color signal demodulator and filter arrangement comprising:

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means for producing a first clock signal having a first phase relationship with respect to said color reference signal;

10

means for producing a second clock signal having a second phase relationship with respect to said color reference signal;

15

a first digital filter having inputs responsive to said digital chrominance signal and said first clock signal, and an output at which a first demodulated and filtered color mixture signal is produced, including a first tapped shift register arrangement through which samples of said digital chrominance signal are shifted in response to said first clock signal; first weighting means coupled to taps of said first shift register for weighting signals on said taps; and means for combining said tap weighted signals produced by said first weighting means and having an output at which said first demodulated and filtered color mixture signal is produced; and

20

25

a second digital filter having inputs responsive to said digital chrominance signal and said second clock signal, and an output at which a second demodulated and filtered color mixture signal is produced, including a second tapped shift register arrangement through which samples of said digital chrominance signal are shifted in response to said second clock signal; second weighting means coupled to taps of said second shift register for weighting signals on said taps; and means for combining said tap weighted signals produced by said second weighting means and having an output at which said second demodulated and filtered color mixture signal is produced.

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1 2. An arrangement according to claim 1, further
comprising a source of analog video signals including a
color burst signal of a given frequency as said color
reference signal, and wherein said source of digital
5 chrominance signals comprises:

means responsive to said color burst component
for producing a sampling signal having a frequency which
is a multiple of the frequency of said color burst signal
and a given phase relationship with respect to
10 said color burst signal;

means responsive to said analog video signals
for sampling said signals in response to said sampling
signal to produce digital video signal samples; and

15 means responsive to said digital video signal
samples for producing separated digital chrominance signals.

3. An arrangement according to Claim 2, wherein said
sampling signal producing means includes means for generat-
20 ing a plurality of pulses during a time interval equal to
one cycle of said color burst signal;

said first clock signal producing means includes
means for producing a clock pulse every color burst signal
cycle in response to a first one of said plurality of samp-
25 ling signal pulses; and

said second clock signal producing means includes
means for producing a clock pulse every color burst signal
cycle in response to a second one of said plurality of
30 sampling signal pulses.



1 4. An arrangement according to any of claims 1-3 wherein said
first digital filter comprises a FIR filter, said first
tapped shift register comprises a plurality of serially
coupled stages including a first stage coupled to receive
5 said digital chrominance signal, said stages including a
plurality of output taps; said first-named combining means
comprises an adder tree arrangement; and said first weighting
means includes means for coupling ones of said output taps
of said adder tree arrangement in a shift-and-add type
10 configuration.

5. An arrangement according to any of claims 1-4 wherein said
second digital filter comprises a FIR filter; said second
tapped shift register comprises a plurality of serially
coupled stages, including a first stage coupled to receive
15 said digital chrominance signal, said stages including a
plurality of output taps; said second-named combining means
comprises a second adder tree arrangement; and said second
weighting means includes means for coupling ones of said
output taps of said second tapped shift register to said
20 second adder tree arrangement in a shift-and-add type
configuration.

6. An arrangement according to claim 4 and claim 5
25 wherein said second FIR filter exhibits an impulse response
concentrated about one of said second shift register
taps and a group delay between said input and said one tap
of said second shift register which is substantially
equal to said given group delay of said first FIR
30 filter.

7. An arrangement according to claim 6 wherein
the number of tapped shift register stages and
weighting function circuits of said first FIR filter
35 exceed the number of tapped shift register stages and
weighting function circuits of said second FIR filter;



1 and wherein said shift register of said second
FIR filter includes at least one untapped shift register
stage coupled between said input and said tapped stages.

5
8. An arrangement according to claim 6 or 7, further
comprising:

10 first processing means coupled to the output of
said first FIR filter, and having an output for producing
a first processed analog color signal;

15 a first lowpass filter coupled to said output
of said first processing means and exhibiting a given
phase versus frequency response characteristic;

second processing means coupled to the output
of said second FIR filter, and having an output for
producing a second processed analog color signal; and

20 a second lowpass filter coupled to said output
of said second processing means and exhibiting a phase
versus frequency response characteristic which is sub-
stantially the same as said given characteristic of said
first lowpass filter.

25 9. An arrangement according to claim 8, wherein the
frequency of said first clock signal is substantially
equal to the frequency of said second clock signal; and
wherein said first and second lowpass filters are construct-
30 ed to exhibit transition bands substantially below the
second subharmonic frequencies of said clock signal frequen-
cies.



1 10. An arrangement according to any of claims 6-9 wherein the
frequencies of said first and second clock signals are sub-
stantially equal to the frequency of said color reference
5 signal; the number of tapped shift register stages of said
first FIR filter is nine; and the number of tapped shift
register stages of said second FIR filter is five.

11. An arrangement according to claim 10 wherein said
shift register of said second FIR filter includes two un-
10 tapped stages coupled between said input and said tapped
stages.

12. An arrangement according to claim 6 wherein:
a sampling signal producing means and said first
15 and second clock signal producing means are comprised in
a clock signal generator having an input responsive to
said color reference signal, a first output at which said
sampling signal is produced having sampling pulses aligned
in phase with the phases of respective color representative
20 components of a received television signal, a second
output at which said first clock signal is produced having
pulses aligned with one of said components, and a third
output at which said second clock signal is produced
having pulses aligned with the other of said components;
25 said first filter is an FIR filter clocked by
said first clock signal and producing at its said output
a filtered version of said one color representative
component, this filter exhibiting a transition band over
a given band of frequencies; and

30 said second filter is an FIR filter clocked
by said second clock signal and producing at its said
output a filtered version of said other component,
said second filter exhibiting a transition band over a
band of frequencies which is lower in frequency than said
35 given band; said arrangement further including:



1 first processing means coupled to the output of
said first FIR filter, and having an output for producing a
first processed analog color signal;

5 a first lowpass filter coupled to said output of
said first processing means and exhibiting a given amplitude
versus frequency response characteristic;

10 second processing means coupled to the output
of said second FIR filter, and having an output for producing a
second processed analog color signal; and

15 a second lowpass filter coupled to said output
of said second processing means and exhibiting an amplitude
versus frequency characteristic which is substantially equal
to said given characteristic.

20 13. A digital television color signal demodulator
and filter arrangement substantially as hereinbefore
described with reference to the accompanying drawings.

