

METHOD OF OPERATING HOST DEVICE AND MEMORY DEVICE, AND MEMORY SYSTEM COMPRISING THE HOST DEVICE AND MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

5 **[0001]** This patent application claims the benefit of and priority to Korean Patent Application No. 10-2021-0072614 filed on 4 June 2021, the disclosure of which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

10 **[0002]** Embodiments of the present disclosure relate to a method of operating a host device and a memory device, and a memory system including the host device and the memory device.

BACKGROUND

15 **[0003]** An eye opening monitor (EOM) is used to determine quality characteristics of signals transmitted and received on a channel. For example, a signal transmission/reception quality between a memory device and a host device may be improved by measuring an eye of a signal received at a signal receive end (e.g., a receiver of a memory device) in a memory system.

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SUMMARY

[0004] Aspects of the present disclosure provide a method of operating a host device capable of efficiently and reliably performing an eye open monitor (EOM).

[0005] Aspects of the present disclosure also provide a method of operating a memory
25 device capable of efficiently and reliably performing an EOM.

[0006] Aspects of the present disclosure also provide a memory system capable of efficiently and reliably performing an EOM.

[0007] According to some aspects of the present disclosure, there is provided a method of operating a host device including transmitting a read command that requests information related to an eye open monitor (EOM) operation performed in a memory device to the memory device, and receiving a response signal including the information related to the EOM operation performed in the memory device from the memory device.

[0008] According to some aspects of the present disclosure, there is provided a method of operating a memory device including receiving a read command that requests information related to an EOM operation performed in the memory device from a host device, identifying an indication field of the read command, and transmitting a response signal including information corresponding to a value of the indication field among the information related to the EOM operation to the host device.

[0009] According to some aspects of the present disclosure, there is provided a memory system including a host device including a host controller, and a memory device including a device controller. The host controller transmits a read command that requests information related to an EOM operation performed in the memory device to the memory device, the read command includes an indication field indicating information to be included in a response signal among the information related to the EOM operation performed in the memory device, and the device controller transmits the response signal including information corresponding to a value of the indication field among the information related to the EOM operation to the host device in response to the read command.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The above and other aspects and features of the present disclosure will become more apparent by describing in detail embodiments thereof with reference to the accompanying drawings, in which:

5 [0011] FIG. 1 is a diagram illustrating a memory system according to some embodiments;

[0012] FIG. 2 is a diagram illustrating a universal flash storage (UFS) interconnect (UIC) layer of FIG. 1 according to some embodiments;

[0013] FIG. 3 is a diagram illustrating a clock data recovery (CDR) block of FIG. 2 according to some embodiments;

10 [0014] FIG. 4 is a diagram for describing an eye open monitor (EOM) operation according to some embodiments;

[0015] FIG. 5 is a diagram illustrating reconfiguration of a UFS device controller, a storage interface, and a nonvolatile memory storage of FIG. 1 according to some embodiments;

15 [0016] FIG. 6 is an illustrative block diagram illustrating a storage device of FIG. 5 according to some embodiments;

[0017] FIG. 7 is a diagram illustrating a three-dimensional (3D) V-NAND structure according to some embodiments;

[0018] FIG. 8 is a flowchart illustrating an operation of a memory system according to some embodiments;

20 [0019] FIGS. 9 to 14 are diagrams for describing an operation of a memory system according to some embodiments;

[0020] FIG. 15 is a flowchart illustrating an operation of a memory system according to some embodiments;

25 [0021] FIG. 16 is a flowchart illustrating a method of performing an EOM operation according to some embodiments;

[0022] FIG. 17 is a flowchart illustrating an operation of a memory system according to some embodiments;

[0023] FIGS. 18 to 25 are diagrams for describing an operation of a memory system according to some other embodiments;

5 **[0024]** FIG. 26 is a diagram illustrating a memory system according to embodiments; and

[0025] FIG. 27 is a diagram illustrating a memory system according to embodiments.

DETAILED DESCRIPTION OF THE EMBODIMENTS

10 **[0026]** Embodiments of the present disclosure will be described more fully hereinafter with reference to the accompanying drawings. Like reference numerals may refer to like elements throughout the accompanying drawings.

[0027] It will be understood that the terms “first,” “second,” “third,” etc. are used herein to distinguish one element from another, and the elements are not limited by these terms. Thus, a “first” element in an embodiment may be described as a “second” element in
15 another embodiment.

[0028] It should be understood that descriptions of features or aspects within each embodiment should typically be considered as available for other similar features or aspects in other embodiments, unless the context clearly indicates otherwise.

20 **[0029]** As used herein, the singular forms “a,” “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise.

[0030] Herein, when one value is described as being about equal to another value or being substantially the same as or equal to another value, it is to be understood that the values are identical, the values are equal to each other within a measurement error, or if measurably unequal, are close enough in value to be functionally equal to each other as would be
25 understood by a person having ordinary skill in the art. For example, the term “about” as

used herein is inclusive of the stated value and means within an acceptable range of deviation for the particular value as determined by one of ordinary skill in the art, considering the measurement in question and the error associated with measurement of the particular quantity (i.e., the limitations of the measurement system). For example, “about”
5 may mean within one or more standard deviations as understood by one of the ordinary skill in the art. Further, it is to be understood that while parameters may be described herein as having “about” a certain value, according to embodiments, the parameter may be exactly the certain value or approximately the certain value within a measurement error as would be understood by a person having ordinary skill in the art.

10 **[0031]** FIG. 1 is a diagram illustrating a memory system according to some embodiments. FIG. 2 is a diagram illustrating a universal flash storage (UFS) interconnect (UIC) layer of FIG. 1 according to some embodiments. FIG. 3 is a diagram illustrating a clock data recovery (CDR) block of FIG. 2 according to some embodiments. FIG. 4 is a diagram for describing an eye open monitor (EOM) operation according to some embodiments.

15 **[0032]** Hereinafter, a memory system according to embodiments of the present disclosure will be described with reference to a system conforming to a universal flash storage (UFS) standard implemented by Joint Electron Device Engineering Council (JEDEC) as an example. However, embodiments of the present disclosure are not limited thereto, and aspects of a memory system according to embodiments of the present disclosure may be
20 variously modified.

[0033] Referring to FIG. 1, a memory system 1 may include a host device 100, a memory device 200, and a UFS interface 300.

[0034] The host device 100 and the memory device 200 may be interconnected through the UFS interface 300. In some embodiments, the host device 100 may be implemented as a
25 portion of an application processor.

[0035] The host device 100 may include a UFS host controller 110, an application 120, a UFS driver 130, a host memory 140, and a UFS interconnect (UIC) layer 150.

[0036] The memory device 200 may include a UFS device controller 210, a nonvolatile memory storage 220, a storage interface 230, a device memory 240, a UIC layer 250, and a regulator 260.

[0037] The nonvolatile memory storage 220 may include a plurality of storage units 221. Such a storage unit 221 may include a V-NAND flash memory having a two-dimensional (2D) structure or a three-dimensional (3D) structure, but may also include other types of nonvolatile memories such as, for example, a phase-change random access memory (PRAM) and/or a resistive random access memory (RRAM).

[0038] The UFS device controller 210 and the nonvolatile memory storage 220 may be interconnected through the storage interface 230. The storage interface 230 may be implemented to comply with a standard convention such as, for example, toggle or open NAND flash interface (ONFI). An operation between the UFS device controller 210 and the nonvolatile memory storage 220 using the toggle will be described further below.

[0039] The application 120 may refer to a program that communicates with the memory device 200 to use a function of the memory device 200. The application 120 may transmit an input-output request (IOR) to the UFS driver 130 for input/output to/from the memory device 200. The input-output request (IOR) may refer to, for example, a read request, a write request, and/or an erase request of data, but is not limited thereto.

[0040] The UFS driver 130 may manage the UFS host controller 110 through a UFS-host controller interface (HCI). The UFS driver 130 may convert the input-output request generated by the application 120 into a UFS command defined by the UFS standard, and transfer the converted UFS command to the UFS host controller 110. One input-output request may be converted into multiple UFS commands. The UFS command may be a

command defined by a small computer system interface (SCSI) standard, but is not limited thereto. For example, in some embodiments, the UFS command may be a command dedicated to the UFS standard.

[0041] The UFS host controller 110 may transmit the UFS command converted by the UFS driver 130 to the UIC layer 250 of the memory device 200 through the UIC layer 150 and the UFS interface 300. In this process, a UFS host register 111 of the UFS host controller 110 may serve as a command queue (CQ).

[0042] The UIC layer 150 of the host device 100 may include MIPI M-PHY and MIPI UniPro, and the UIC layer 250 of the memory device 200 may also include MIPI M-PHY and MIPI UniPro.

[0043] The UFS interface 300 may include a line transmitting a reference clock REF_CLK, a line transmitting a hardware reset signal RESET_n for the memory device 200, a pair of lines transmitting a pair of differential input signals DIN_T and DIN_C, and a pair of lines transmitting a pair of differential output signals DOUT_T and DOUT_C.

[0044] A frequency value of the reference clock provided from the host device 100 to the memory device 200 may be, for example, about 19.2 MHz, about 26 MHz, about 38.4 MHz, or about 52 MHz, but is not necessarily limited thereto. The host device 100 may change the frequency value of the reference clock during operation, that is, during a period in which data transmission/reception is performed between the host device 100 and the memory device 200.

[0045] The memory device 200 may generate clocks of various frequencies from the reference clock provided from the host device 100 using, for example, a phase-locked loop (PLL). In addition, the host device 100 may set a value of a data rate between the host device 100 and the memory device 200 through the frequency value of the reference clock.

That is, the value of the data rate may be determined depending on the frequency value of the reference clock.

[0046] The UFS interface 300 may support multiple lanes, and each lane may be implemented as a differential pair. For example, the UFS interface 300 may include one or more receive lanes and one or more transmit lanes. In FIG. 1, the pair of lines transmitting the pair of differential input signals DIN_T and DIN_C may constitute the receive lane, and the pair of lines transmitting the pair of differential output signals DOUT_T and DOUT_C may constitute the transmit lane. Although one pair of transmit lanes and one pair of receive lanes are illustrated in FIG. 1, the number of transmit lanes and receive lanes is not limited thereto, and may be modified.

[0047] The receive lane and the transmit lane may transmit data in a serial communication manner, and the host device 100 and the memory device 200 may communicate with each other in a full-duplex manner by a structure in which the receive lane and the transmit lane are separated from each other. That is, the memory device 200 may transmit data to the host device 100 through the transmit lane while receiving data from the host device 100 through the receive lane. In addition, control data such as a command from the host device 100 to the memory device 200 and user data that the host device 100 intends to store in or read from the nonvolatile memory storage 220 of the memory device 200 may be transmitted through the same lane. Accordingly, in some embodiments, a separate lane for data transmission between the host device 100 and the memory device 200 is not utilized in addition to a pair of receive lanes and a pair of transmit lanes.

[0048] Referring to FIG. 2, the UIC layer 250 may include equalizers 251 each including an analog front end (AFE), clock data recovery (CDR) blocks 253, decoders 256, descramblers 257, symbol removers 258, a lane merger 259, and a symbol translator 259a.

[0049] The equalizer 251 may receive the pair of differential input signals DIN_T and DIN_C from the host device 100 (see FIG. 1), perform equalization, and output a serial bit SB. In some embodiments, the host device 100 (see FIG. 1) may provides the pair of differential input signals DIN_T and DIN_C, which are serial signals, to the equalizer 251, and the equalizer 251 may output the serial bit SB from the pair of differential input signals DIN_T and DIN_C.

[0050] The CDR block 253 may perform clock data recovery (CDR) and data deserialization, and output an N-bit signal, where N is a natural number. The CDR block 253 may include an eye opening monitor (EOM) block 255 performing an EOM operation to measure a signal quality of a communication channel with the host device 100 (see FIG. 1).

[0051] In some embodiments, the EOM operation performed in the CDR block 253 may be performed using, for example, a special function register (SFR) 252, but embodiments are not limited thereto.

[0052] Referring to FIGS. 2 and 3, the EOM operation performed in the CDR block 253 may be performed by measuring a quality of a signal received from the host device 100 under a specific offset condition using the SFR 252.

[0053] For example, the EOM operation may be performed by comparing a main path signal MS of a main path indicated by a solid line in FIG. 3 with an EOM path signal ES of an EOM path indicated by a dotted line in FIG. 3.

[0054] The main path may recover a clock from the serial bit SB received from the host device 100 and passing through the equalizer 251 using a clock recovery circuit 253b, extract data of the serial bit SB using the recovered clock RCK, and then generate the main path signal MS through a deserializer 253a. The main path signal MS generated as such may be transferred to a comparator 255b.

[0055] The EOM path may generate a clock dxRCK by reflecting a specific offset value dX in the clock recovered from the serial bit SB received from the host device 100 and passing through the equalizer 251, extract data of the serial bit SB by reflecting the clock dxRCK and a specific offset value dY, and then generate the EOM path signal ES through a deserializer 255a. The EOM path signal MS generated as such may be transferred to the comparator 255b.

[0056] For example, the main path signal MS may be data extracted under reference conditions XR and YR of FIG. 4, and the EOM path signal ES may be data extracted under offset conditions dX and dY of FIG. 4.

[0057] The comparator 255b does not output an error count signal EC when the EOM path signal ES is recognized as the same signal as the main path signal MS, and may output the error count signal EC when the EOM path signal ES is not recognized as the same signal as the main path signal MS. That is, error counting may be performed by the error count signal EC output from the comparator 255b.

[0058] In addition, the comparator 255b may output a sampling count signal SC whenever such sampling (e.g., comparison between the EOM path signal ES and the main path signal MS) is performed once.

[0059] In some embodiments, the offset value dX may include, for example, a time offset value, a phase offset value, etc., and the offset value dY may include, for example, a voltage offset value, but embodiments are not limited thereto.

[0060] In some embodiments, the offset dX, the offset dY, an error count value according to the error count signal EC, information on the number of sampling operations according to the sampling count signal SC, etc., may be stored in the SFR 252, but embodiments are not limited thereto.

[0061] Referring back to FIG. 2, the decoder 256 may decode the N-bit signal output from the CDR block 253 into an M-bit signal, where M is a natural number smaller than N, and a discrimination signal DS. In some embodiments, the N-bit signal may be a 10-bit signal, and the M-bit signal may be an 8-bit signal, but embodiments are not limited thereto.

5 **[0062]** The decoder 256 may output a data signal D as the discrimination signal DS when the input N-bit signal is a data symbol, and output a control signal K as the discrimination signal DS when the input N-bit signal is a control symbol.

[0063] The descrambler 257 may descramble and output the input M-bit signal. The symbol remover 258 may remove skip symbols such as, for example, a marker and a filler
10 symbol from the input M-bit signal. The lane merger 259 may merge signals input to each lane and provide the merged signal to the symbol translator 259a. The symbol translator 259a may translate and output the symbol.

[0064] Referring back to FIG. 1, the UFS device controller 210 of the memory device 200 may generally control an operation of the memory device 200.

15 **[0065]** The UFS device controller 210 may manage the nonvolatile memory storage 220 through logical units (LUs) 211 which are logical data storage units. The number of LUs 211 may be, for example, eight, but embodiments are not limited thereto.

[0066] The UFS device controller 210 may include a flash translation layer (FTL), and may convert a logical data address, for example, a logical block address (LBA), transferred from
20 the host device 100, to a physical data address, for example, a physical data address or a physical page number using address mapping information of the FTL. In the memory system 1, a logical block for storing user data may have a size in a predetermined range. For example, a minimum size of the logical block may be set to 4 Kbytes.

[0067] When a command from the host device 100 is input to the memory device 200
25 through the UIC layer 250, the UFS device controller 210 may perform an operation

according to the input command, and may transmit a completion response to the host device 100 when the operation is completed.

[0068] As an example, when the host device 100 intends to store user data in the memory device 200, the host device 100 may transmit a data write command to the memory device 200. When a response indicating that the memory device 200 has been ready-to-receive the user data is received from the memory device 200, the host device 100 may transmit the user data to the memory device 200. The UFS device controller 210 may temporarily store the received user data in the device memory 240, and may store the user data temporarily stored in the device memory 240 in a selected position of the nonvolatile memory storage 220 based on the address mapping information of the FTL.

[0069] As another example, when the host device 100 intends to read user data stored in the memory device 200, the host device 100 may transmit a data read command to the memory device 200. The UFS device controller 210 receiving the data read command may read the user data from the nonvolatile memory storage 220 based on the data read command and temporarily store the read user data in the device memory 240. In such a read process, the UFS device controller 210 may detect and correct an error in the read user data using a built-in error correction code (ECC) circuit. In addition, the UFS device controller 210 may transmit the user data temporarily stored in the device memory 240 to the host device 100.

[0070] In addition, the UFS device controller 210 may further include an advanced encryption standard (AES) circuit. The AES circuit may encrypt or decrypt data input to the UFS device controller 210 using a symmetric-key algorithm.

[0071] The host device 100 may sequentially store commands to be transmitted to the memory device 200 in the UFS host register 111 that may function as the command queue, and sequentially transmit the commands to the memory device 200. In this case, even

when the previously transmitted command is still being processed by the memory device 200, that is, even before a notification indicating that processing of the previously transmitted command by the memory device 200 has been completed is received, the host device 100 may transmit the next command queued in the command queue to the memory device 200. Accordingly, the memory device 200 may receive the next command from the host device 100 while processing the previously transmitted command. The maximum number of commands (queue depth) that may be stored in such a command queue may be, for example, 32. In addition, the command queue may be implemented as a circular queue type that indicates a start and an end of a command string stored in the queue through a head pointer and a tail pointer, respectively.

[0072] Each of the plurality of storage units 221 may include a memory cell array and a control circuit that controls an operation of the memory cell array. The memory cell array may include a two-dimensional memory cell array or a three-dimensional memory cell array. The memory cell array may include a plurality of memory cells, each of which may be a single level cell (SLC) storing information of one bit, but is not limited thereto, and may be a cell storing information of two or more bits, such as, for example, a multi level cell (MLC), a triple level cell (TLC), or a quadruple level cell (QLC). The three-dimensional memory cell array may include a vertical NAND string vertically oriented so that at least one memory cell is positioned on another memory cell. This will be described in further detail below.

[0073] VCC, VCCQ1, and VCCQ2 may be input to the memory device 200 as power supply voltages. VCC is a main power supply voltage for the memory device 200 and may have a value of, for example, about 2.4 V to about 3.6 V. VCCQ1 is a power supply voltage for supplying a voltage in a low range, is primarily used for the UFS device controller 210, and may have a value of, for example, about 1.14 V to about 1.26 V.

VCCQ2 is a power supply voltage for supplying a voltage lower than VCC but higher than VCCQ1, is primarily used for an input/output interface such as MIPI M-PHY 250, and may have a value of, for example, about 1.7 V to about 1.95 V. The power supply voltages may be supplied to respective components of the memory device 200 through the regulator 260. The regulator 260 may be implemented as a set of unit regulators each connected to different ones of the above-described power supply voltages.

[0074] FIG. 5 is a diagram illustrating reconfiguration of a UFS device controller, a storage interface, and a nonvolatile memory storage of FIG. 1 according to some embodiments.

[0075] The storage interface 230 of FIG. 1 may include a controller interface circuit 230a and a memory interface circuit 230b of FIG. 5. In some embodiments, a storage device 224 illustrated in FIG. 5 may correspond to one storage unit 221 of FIG. 1. In addition, in some embodiments, the storage device 224 may correspond to the nonvolatile memory storage 220 of FIG. 1.

[0076] The storage device 224 may include first to eighth pins P11 to P18, the memory interface circuit 230b, a control logic circuit 510, and a memory cell array 520.

[0077] The memory interface circuit 230b may receive a chip enable signal nCE from the device controller 210 through the first pin P11. The memory interface circuit 230b may transmit and receive signals to and from the device controller 210 through the second to eighth pins P12 to P18 according to the chip enable signal nCE. For example, when the chip enable signal nCE is in an enable state (e.g., at a low level), the memory interface circuit 230b may transmit and receive signals to and from the device controller 210 through the second to eighth pins P12 to P18.

[0078] The memory interface circuit 230b may receive a command latch enable signal CLE, an address latch enable signal ALE, and a write enable signal nWE from the device controller 210 through the second to fourth pins P12 to P14. The memory interface circuit

230b may receive a data signal DQ from the device controller 210 or transmit a data signal DQ to the device controller 210 through the seventh pin P17. A command CMD, an address ADDR, and data DATA may be transferred through the data signal DQ. For example, the data signal DQ may be transferred through a plurality of data signal lines. In this case, the seventh pin P17 may include a plurality of pins corresponding to a plurality of data signals.

[0079] The memory interface circuit 230b may obtain the command CMD from the data signal DQ received in an enable section (e.g., a high level state) of the command latch enable signal CLE based on toggle timings of the write enable signal nWE. The memory interface circuit 230b may obtain the address ADDR from the data signal DQ received in an enable section (e.g., a high level state) of the address latch enable signal ALE based on the toggle timings of the write enable signal nWE.

[0080] In some embodiments, the write enable signal nWE may be maintained in a static state (e.g., a high level or a low level), and then toggle between a high level and a low level. For example, the write enable signal nWE may toggle in a section in which the command CMD or the address ADDR is transmitted. Accordingly, the memory interface circuit 230b may obtain the command CMD or the address ADDR based on the toggle timings of the write enable signal nWE.

[0081] The memory interface circuit 230b may receive a read enable signal nRE from the device controller 210 through the fifth pin P15. The memory interface circuit 230b may receive a data strobe signal DQS from the device controller 210 or transmit a data strobe signal DQS to the device controller 210 through the sixth pin P16.

[0082] In a data output operation of the storage device 224, the memory interface circuit 230b may receive the toggling read enable signal nRE through the fifth pin P15 before outputting the data DATA. The memory interface circuit 230b may generate the toggling

data strobe signal DQS based on the toggling of the read enable signal nRE. For example, the memory interface circuit 230b may generate the data strobe signal DQS starting to toggle after a delay (e.g., tDQSRE) predefined on the basis of a toggling start time of the read enable signal nRE. The memory interface circuit 230b may transmit the data signal DQ including the data DATA based on a toggle timing of the data strobe signal DQS. Accordingly, the data DATA may be aligned with the toggle timing of the data strobe signal DQS and transmitted to the device controller 210.

[0083] In a data input operation of the storage device 224, when the data signal DQ including the data DATA is received from the device controller 210, the memory interface circuit 230b may receive the toggling data strobe signal DQS together with the data DATA from the device controller 210. The memory interface circuit 230b may obtain the data DATA from the data signal DQ based on the toggle timing of the data strobe signal DQS. For example, the memory interface circuit 230b may obtain the data DATA by sampling the data signal DQ at a rising edge and a falling edge of the data strobe signal DQS.

[0084] The memory interface circuit 230b may transmit a ready/busy output signal nR/B to the device controller 210 through the eighth pin P18. The memory interface circuit 230b may transmit state information of the storage device 224 to the device controller 210 through the ready/busy output signal nR/B. When the storage device 224 is in a busy state (e.g., when internal operations of the storage device 224 are being performed), the memory interface circuit 230b may transmit the ready/busy output signal nR/B indicating the busy state to the device controller 210. When the storage device 224 is in a ready state (e.g., when internal operations of the storage device 224 are not performed or have been completed), the memory interface circuit 230b may transmit the ready/busy output signal nR/B indicating the ready state to the device controller 210. For example, while the storage device 224 reads the data DATA from the memory cell array 520 in response to a

page read command, the memory interface circuit 230b may transmit the ready/busy output signal nR/B indicating the busy state (e.g., a low level) to the device controller 210. For example, while the storage device 224 programs the data DATA in the memory cell array 520 in response to a program command, the memory interface circuit 230b may transmit the ready/busy output signal nR/B indicating the busy state to the device controller 210.

[0085] The control logic circuit 510 may generally control various operations of the storage device 224. The control logic circuit 510 may receive the command/address CMD/ADDR obtained from the memory interface circuit 230b. The control logic circuit 510 may generate control signals for controlling other components of the storage device 224 according to the received command/address CMD/ADDR. For example, the control logic circuit 510 may generate various control signals for programming the data DATA in the memory cell array 520 or reading the data DATA from the memory cell array 520.

[0086] The memory cell array 520 may store the data DATA obtained from the memory interface circuit 230b under the control of the control logic circuit 510. The memory cell array 520 may output the stored data DATA to the memory interface circuit 230b under the control of the control logic circuit 510.

[0087] The memory cell array 520 may include a plurality of memory cells. For example, the plurality of memory cells may be flash memory cells. However, embodiments of the present disclosure are not limited thereto. For example, in some embodiments, the memory cells may be, for example, resistive random access memory (RRAM) cells, ferroelectric random access memory (FRAM) cells, phase change random access memory (PRAM) cells, thyristor random access memory (TRAM) cells, or magnetic random access memory (MRAM) cells. Hereinafter, embodiments of the present disclosure will be described with a focus on an embodiment in which the memory cells are NAND flash memory cells.

[0088] The device controller 210 may include first to eighth pins P21 to P28 and the controller interface circuit 230a. The first to eighth pins P21 to P28 may correspond to the first to eighth pins P11 to P18 of the storage device 224, respectively.

[0089] The controller interface circuit 230a may transmit the chip enable signal nCE to the storage device 224 through the first pin P21. The controller interface circuit 230a may transmit and receive signals to and from the storage device 224 selected through the chip enable signal nCE through the second to eighth pins P22 to P28.

[0090] The controller interface circuit 230a may transmit the command latch enable signal CLE, the address latch enable signal ALE, and the write enable signal nWE to the storage device 224 through the second to fourth pins P22 to P24. The controller interface circuit 230a may transmit the data signal DQ to the storage device 224 or receive the data signal DQ from the storage device 224 through the seventh pin P27.

[0091] The controller interface circuit 230a may transmit the data signal DQ including the command CMD or the address ADDR together with the toggling write enable signal nWE to the storage device 224. The controller interface circuit 230a may transmit the data signal DQ including the command CMD to the storage device 224 as it transmits the command latch enable signal CLE having an enable state, and transmit the data signal DQ including the address ADDR to the storage device 224 as it transmits the address latch enable signal ALE having an enable state.

[0092] The controller interface circuit 230a may transmit the read enable signal nRE to the storage device 224 through the fifth pin P25. The controller interface circuit 230a may receive the data strobe signal DQS from the storage device 224 or transmit the data strobe signal DQS to the storage device 224 through the sixth pin P26.

[0093] In the data output operation of the storage device 224, the controller interface circuit 230a may generate the toggling read enable signal nRE and transmit the read enable signal

nRE to the storage device 224. For example, the controller interface circuit 230a may generate the read enable signal nRE changed from a fixed state (e.g., a high level or a low level) to a toggle state before the data DATA is output. Accordingly, the toggling data strobe signal DQS may be generated based on the read enable signal nRE in the storage device 224. The controller interface circuit 230a may receive the data signal DQ including the data DATA together with the toggling data strobe signal DQS from the storage device 224. The controller interface circuit 230a may obtain the data DATA from the data signal DQ based on the toggle timing of the data strobe signal DQS.

[0094] In the data input operation of the storage device 224, the controller interface circuit 230a may generate the toggling data strobe signal DQS. For example, the controller interface circuit 230a may generate the data strobe signal DQS changed from a fixed state (e.g., a high level or a low level) to a toggle state before transmitting the data DATA. The controller interface circuit 230a may transmit the data signal DQ including the data DATA to the storage device 224 based on the toggle timings of the data strobe signal DQS.

[0095] The controller interface circuit 230a may receive the ready/busy output signal nR/B from the storage device 224 through the eighth pin P28. The controller interface circuit 230a may determine the state information of the storage device 224 based on the ready/busy output signal nR/B.

[0096] FIG. 6 is an illustrative block diagram illustrating a storage device of FIG. 5 according to some embodiments.

[0097] Referring to FIG. 6, the storage device 224 may include a control logic circuit 510, a memory cell array 520, a page buffer unit 550, a voltage generator 530, and a row decoder 540. In some embodiments, the storage device 224 may further include the memory interface circuit 230b illustrated in FIG. 5, and may further include, for example, a column logic, a pre-decoder, a temperature sensor, a command decoder, an address decoder, etc.

[0098] The control logic circuit 510 may generally control various operations in the storage device 224. The control logic circuit 510 may output various control signals in response to the command CMD and/or the address ADDR from the memory interface circuit 230b. For example, the control logic circuit 510 may output a voltage control signal CTRL_vol, a row address X-ADDR, and a column address Y-ADDR.

[0099] The memory cell array 520 may include a plurality of memory blocks BLK1 to BLKz, where z is a positive integer, each of which may include a plurality of memory cells. The memory cell array 520 may be connected to the page buffer unit 550 through bit lines BL, and may be connected to the row decoder 540 through word lines WL, string selection lines SSL, and ground selection lines GSL.

[00100] In an embodiment, the memory cell array 520 may include a three-dimensional (3D) memory cell array, and the 3D memory cell array may include a plurality of NAND strings. Each NAND string may include memory cells each connected to word lines vertically stacked on a substrate. U.S. Patent No. 7,679,133, U.S. Patent No. 8,553,466, U.S. Patent No. 8,654,587, U.S. Patent No. 8,559,235, and U.S. Patent Application Publication No. 2011/0233648 are incorporated herein by reference. In an embodiment, the memory cell array 520 may include a two-dimensional (2D) memory cell array, and the 2D memory cell array may include a plurality of NAND strings arranged along row and column directions.

[00101] The page buffer unit 550 may include a plurality of page buffers PB1 to PBn, where n is a positive integer equal to 3 or more, and the plurality of page buffers PB1 to PBn may be connected, respectively, to the memory cells through a plurality of bit lines BL. The page buffer unit 550 may select at least one of the bit lines BL in response to the column address Y-ADDR. The page buffer unit 550 may operate as a write driver or a sense amplifier according to an operation mode. For example, at the time of a program

operation, the page buffer unit 550 may apply a bit line voltage corresponding to data to be programmed to the selected bit line. At the time of a read operation, the page buffer unit 550 may sense a current or voltage of the selected bit line to sense data stored in the memory cell.

5 **[00102]** The voltage generator 530 may generate various types of voltages for performing program, read, and erase operations based on the voltage control signal CTRL_vol. For example, the voltage generator 530 may generate a program voltage, a read voltage, a program verification voltage, an erase voltage, etc., as word line voltages VWL.

10 **[00103]** The row decoder 540 may select one of a plurality of word lines WL and may select one of a plurality of string selection lines SSL in response to the row address X-ADDR. For example, the row decoder 540 may apply the program voltage and the program verification voltage to the selected word line at the time of the program operation, and may apply the read voltage to the selected word line at the time of the read operation.

15 **[00104]** FIG. 7 is a diagram illustrating a three-dimensional (3D) V-NAND structure according to some embodiments.

[00105] When the storage module of a UFS device is implemented as a 3D V-NAND-type flash memory, each of a plurality of memory blocks constituting the storage module may be represented by an equivalent circuit as illustrated in FIG. 7.

20 **[00106]** A memory block BLK_i illustrated in FIG. 7 is a three-dimensional memory block formed in a three-dimensional structure on a substrate. For example, a plurality of memory NAND strings included in the memory block BLK_i may be formed in a direction perpendicular to the substrate.

25 **[00107]** Referring to FIG. 7, the memory block BLK_i may include a plurality of memory NAND strings NS11 to NS33 connected between bit lines BL1, BL2, and BL3 and a common source line CSL. Each of the plurality of memory NAND strings NS11 to NS33

may include a string selection transistor SST, a plurality of memory cells MC1, MC2, ..., MC8, and a ground selection transistor GST. It has been illustrated in FIG. 6 that each of the plurality of memory NAND strings NS11 to NS33 includes eight memory cells MC1, MC2, ..., MC8, but embodiments of the present disclosure are not necessarily limited thereto.

[00108] The string selection transistor SST may be connected to a corresponding string selection line SSL1, SSL2, or SSL3. The plurality of memory cells MC1, MC2, ..., MC8 may be connected to corresponding gate lines GTL1, GTL2, ..., GTL8, respectively. The gate lines GTL1, GTL2, ..., GTL8 may correspond to word lines, and some of the gate lines GTL1, GTL2, ..., GTL8 may correspond to dummy word lines. The ground selection transistor GST may be connected to a corresponding ground selection line GSL1, GSL2, or GSL3. The string selection transistor SST may be connected to a corresponding bit line BL1, BL2, or BL3, and the ground selection transistor GST may be connected to the common source line CSL.

[00109] Word lines (for example, WL1) having the same height may be connected in common, and the ground selection lines GSL1, GSL2, and GSL3 and the string selection lines SSL1, SSL2, and SSL3 may be separated from each other, respectively. It has been illustrated in FIG. 7 that the memory block BLKi is connected to eight gate lines GTL1, GTL2, ..., GTL8 and three bit lines BL1, BL2, and BL3, but embodiments of the present disclosure are not necessarily limited thereto.

[00110] FIG. 8 is a flowchart illustrating an operation of a memory system according to some embodiments. FIGS. 9 to 14 are diagrams for describing an operation of a memory system according to some embodiments.

[00111] First, referring to FIG. 8, the host device 100 transmits a command for requesting the memory device 200 to perform an eye open monitor (EOM) operation to the memory device 200 (S110).

[00112] In some embodiments, such a request command may be implemented in the form of a WRITE BUFFER COMMAND illustrated in FIG. 9 according to a JEDEC UFS standard. FIG. 9 is a diagram illustrating a command descriptor block (CDB) of the WRITE BUFFER COMMAND according to the JEDEC UFS standard, and FIG. 10 is a diagram illustrating set values of a mode field Mode of the WRITE BUFFER COMMAND.

[00113] For example, referring to FIGS. 1, 9, and 10, the UFS host controller 110 of the host device 100 may request the UFS device controller 210 of the memory device 200 to perform an EOM operation by setting a mode field Mode of the WRITE BUFFER COMMAND to 1F. In addition, the UFS device controller 210 receiving such a request may prepare for the EOM operation.

[00114] In some embodiments, operations of the UFS host controller 110 and operations of the UFS device controller 210 may be performed by controlling the UFS host controller 110 and the UFS device controller 210 by predetermined firmware, but embodiments are not limited thereto.

[00115] Referring to FIG. 10, an embodiment in which the UFS device controller 210 requests to perform the EOM operation when a set value of the mode field Mode of the WRITE BUFFER COMMAND is 1F is illustrated, but embodiments of the present disclosure are not limited thereto. For example, in some embodiments, the set value of the mode field Mode for requesting the UFS device controller 210 to perform the EOM operation may be modified into other set values (e.g., other set values set as reserved in standard specifications, such as 1D and 1E).

[00116] Referring to FIGS. 1 and 9, the UFS host controller 110 may transfer a size of EOM data, which is described in further detail below, to the UFS device controller 210 using a parameter list length field **PARAMETER LIST LENGTH** of the **WRITE BUFFER COMMAND**.

5 **[00117]** Then, referring to FIG. 8, the memory device 200 transmits a response to the **WRITE BUFFER COMMAND** to the host device 100 (S120).

[00118] In some embodiments, such a response may include receivable data capacity information of the memory device 200. That is, when the memory device 200 responds to the host device 100 with, for example, k bytes, where k is a natural number, the host device
10 100 may divide and transmit data to be subsequently transmitted to the memory device 200 (e.g., data utilized for performing the EOM operation) in units of k bytes.

[00119] Then, referring to FIG. 8, the host device 100 transmits generated EOM data to the memory device 200 (S130), and the memory device 200 transmits a response to reception of the EOM data to the host device 100 (S140).

15 **[00120]** In some embodiments, the host device 100 may generate the EOM data utilized for the EOM operation to be performed in the memory device 200.

[00121] A generation point in time of the EOM data may be earlier than a point in time corresponding to S110 when the host device 100 transmits the command for requesting the memory device 200 to perform the EOM operation to the memory device 200, or may be
20 later than a point in time corresponding to S120 when the host device 100 receives the response to the **WRITE BUFFER COMMAND** from the memory device 200.

[00122] Alternatively, in some embodiments, a generation point in time of the EOM data may be between a point in time corresponding to S110 when the host device 100 transmits the command for requesting the memory device 200 to perform the EOM operation to the
25 memory device 200 and a point in time corresponding to S120 when the host device 100

receives the response to the WRITE BUFFER COMMAND from the memory device 200. That is, a timing when the host device 100 generates the EOM data utilized for the EOM operation to be performed in the memory device 200 may be variously modified.

[00123] In some embodiments, the EOM data generated by the host device 100 may include parameters utilized for performing the EOM operation and pattern data utilized for performing the EOM operation.

[00124] In some embodiments, the parameter utilized for performing the EOM operation may include the offset values dX and dY for performing the EOM operation of the memory device 200 described above.

[00125] The offset value dX may include, for example, a time offset value, a phase offset value, etc., and the offset value dY may include, for example, a voltage offset value, but embodiments are not limited thereto.

[00126] In addition, the parameter utilized for performing the EOM operation may include, for example, phase resolution information. Such phase resolution information may be used for the memory device 200 to receive the pattern data from the host device 100.

[00127] In some embodiments, the pattern data utilized for performing the EOM operation may be the serial bit SB (see FIG. 3) provided from the host device 100, which is utilized for performing the EOM operation of the memory device 200 described above.

[00128] In some embodiments, the host device 100 may generate a plurality of pattern data, and the plurality of pattern data may be generated by as many combinations of bit sequences as possible and be generated using data patterns in which results of performing the EOM operation are consistent.

[00129] Examples of such pattern data may include pseudorandom binary sequence (PRBS) data, compliant random test pattern (CRPAT) data, compliant jitter tolerance pattern (CJTPAT) data, etc., but embodiments are not limited thereto.

[00130] FIG. 11 is a diagram illustrating a structure of EOM data transmitted by the host device 100 to the memory device 200 according to some embodiments.

[00131] Referring to FIG. 11, the EOM data may include an EOM data header EDH and an EOM data pattern EDP.

5 **[00132]** The EOM data header EDH may include parameters utilized for performing the EOM operation. For example, a phase selection field PHASE SELECT may include a time offset value or a phase offset value to be transferred to the memory device 200, and a reference voltage control field VREF CONTROL may include a voltage offset value to be transferred to the memory device 200.

10 **[00133]** That is, the time offset value or the phase offset value utilized for the memory device 200 to perform the EOM operation described above with reference to FIGS. 3 and 4 may be provided from the host device 100 to the memory device 200 through the phase selection field PHASE SELECT. In addition, the voltage offset value utilized for the memory device 200 to perform the EOM operation described above with reference to FIGS.
15 3 and 4 may be provided from the host device 100 to the memory device 200 through the reference voltage control field VREF CONTROL.

[00134] The phase resolution information (e.g., gear information) referred to for the memory device 200 to receive the pattern data from the host device 100 may be provided from the host device 100 to the memory device 200 through a phase resolution field PHASE
20 RESOLUTION.

[00135] In addition, the number of sampling operations that the memory device 200 executes while performing the EOM operation may be provided from the host device 100 to the memory device 200 through a number-of-sampling field NUMBER OF SAMPLING.

[00136] In addition, a size of the pattern data to be received by the memory device 200 from the host device 100 may be provided from the host device 100 to the memory device 200 through a data length field EOM DATA LENGTH.

[00137] Although an example of the EOM data header EDH including 12 bytes is illustrated in FIG. 11, embodiments are not limited thereto, and a size of the EOM data header EDH may be variously modified.

[00138] The EOM data pattern EDP may include pattern data utilized for performing the EOM operation. As illustrated in FIG. 11, the EOM data pattern EDP may include a plurality of pattern data. In some embodiments, N illustrated in FIG. 11 may be a natural number greater than 12.

[00139] Referring to FIG. 12, the EOM data header EDH and the EOM data pattern EDP may be transmitted from the host device 100 to the memory device 200 multiple times. In this case, in determining a method of transmitting the EOM data header EDH and the EOM data pattern EDP to the memory device 200 by the host device 100, the receivable data capacity information transmitted by the memory device 200 to the host device 100 as the response in S120 of FIG. 8 may be considered.

[00140] For example, assuming that the receivable data capacity information transmitted by the memory device 200 to the host device 100 as the response in S110 of FIG. 8 is 12 bytes, the host device 100 may transmit the EOM data header EDH and the EOM data pattern EDP to the memory device 200 using a method according to FIG. 12.

[00141] For example, in some embodiments, the host device 100 first transmits an EOM data header EDH having a size of 12 bytes to the memory device 200 (S130a). Then, the memory device 200 transmits a response indicating that the EOM data header EDH has been received to the host device 100 (S140a).

[00142] Then, the host device 100 transmits an EOM data pattern EDP having a size of 12 bytes among EOM data patterns EDP to the memory device 200 (S130b). Then, the memory device 200 transmits a response indicating that the EOM data pattern EDP has been received to the host device 100 (S140b). Then, the host device 100 transmits a subsequent EOM data pattern EDP having a size of 12 bytes among the EOM data patterns EDP to the memory device 200 (S130c). Then, the memory device 200 transmits a response indicating that the EOM data pattern EDP has been received to the host device 100 (S140c). By repeating these operations, all of the EOM data patterns EDP illustrated in FIG. 12 may be provided from the host device 100 to the memory device 200.

[00143] The structure of the EOM data transmitted by the host device 100 to the memory device 200 is not limited to the example illustrated in FIG. 11.

[00144] FIG. 13 is a diagram illustrating a structure of EOM data transmitted by a host device 100 to a memory device 200 according to some embodiments.

[00145] Referring to FIG. 13, the EOM data may include an EOM data header EDH and an EOM data pattern EDP.

[00146] The EOM data header EDH may include parameters utilized for performing the EOM operation.

[00147] For example, a timing offset field Timing Offset and a timing step field Timing Step may include a time offset value or a phase offset value to be transferred to the memory device 200, and a voltage offset field Voltage Offset and a voltage step field Voltage Step may include a voltage offset value to be transferred to the memory device 200.

[00148] That is, the time offset value or the phase offset value utilized for the memory device 200 to perform the EOM operation described above with reference to FIGS. 3 and 4 may be provided from the host device 100 to the memory device 200 through the timing offset field Timing Offset and the timing step field Timing Step. In addition, the voltage

offset value utilized for the memory device 200 to perform the EOM operation described above with reference to FIGS. 3 and 4 may be provided from the host device 100 to the memory device 200 through the voltage offset field Voltage Offset and the voltage step field Voltage Step.

5 **[00149]** That is, in some embodiments, the offset value dX and the offset value dY illustrated in FIGS. 3 and 4 are not expressed as one value as in an embodiment illustrated in FIG. 11, but rather, are expressed as two fields: a reference value (a reference phase or a reference voltage) and an offset value (an offset phase value or a offset voltage value) with respect to the reference value.

10 **[00150]** The number of sampling operations that the memory device 200 executes while performing the EOM operation may be provided from the host device 100 to the memory device 200 through a number-of-sampling field Number of Sampling.

15 **[00151]** In addition, a size of the pattern data to be received by the memory device 200 from the host device 100 may be provided from the host device 100 to the memory device 200 through a data length field Total Data Length.

[00152] Referring back to FIG. 8, the memory device 200 receiving the EOM data performs the EOM operation (S150).

20 **[00153]** In some embodiments, such an EOM operation may be performed after the EOM data header EDH (see FIG. 12) is received and while the EOM data pattern EDP (see FIG. 11) is received. However, embodiments are not limited thereto, and the EOM operation may also be performed after all of the EOM data patterns EDP (see FIG. 12) are received.

25 **[00154]** Referring back to FIGS. 1 to 4, the EOM block 255 may perform the operation described above with reference to FIGS. 3 and 4 whenever one pattern data is received from the host device 100. That is, the error count signal EC and the sampling count signal SC may be output for each received pattern data.

[00155] The sampling count signal SC may be used to determine whether the number of sampling operations of the number-of-sampling field NUMBER OF SAMPLING provided from the host device 100 to the memory device 200 is the same as the number of sampling operations performed by the memory device 200.

5 **[00156]** The error count signal EC may be used to calculate an error count value corresponding to the phase offset value provided through the phase selection field PHASE SELECT and the voltage offset value provided through the reference voltage control field VREF CONTROL for all pattern data received from the host device 100.

[00157] For example, assuming that the host device 100 has transmitted one hundred
10 pieces of pattern data for the memory device 200 to perform the EOM operation and the number of error count signals EC output by the EOM block 255 receiving the one hundred pieces of pattern data is 30, the error count value according to the performance of the EOM operation may be 30. Such an error count value may be used to calculate an error rate (e.g., 30% in the present example).

15 **[00158]** Referring back to FIG. 8, the memory device 200 that has performed the EOM operation transmits a response signal including a result of performing the EOM operation to the host device 100 (S160).

[00159] In this case, the response signal may include information indicating whether the performance of the EOM operation has been successful, the error count value corresponding
20 to the phase offset value and the voltage offset value, and the parameters utilized for performing the EOM operation.

[00160] For example, when the number of sampling operations of the number-of-sampling field NUMBER OF SAMPLING provided from the host device 100 to the memory device 200 is the same as the number of sampling count signals SC output by the comparator 255b
25 of the memory device 200, the memory device 200 may determine that the performance of

the EOM operation has been completed and transmit complete information to the host device 100.

[00161] Alternatively, when the number of sampling operations of the number-of-sampling field NUMBER OF SAMPLING provided from the host device 100 to the memory device 200 is different from the number of sampling count signals SC output by the comparator 255b of the memory device 200, the memory device 200 may determine that the performance of the EOM operation has not been completed and transmit failure information to the host device 100.

[00162] In some embodiments, the information indicating whether the performance of the EOM operation has been successful may be provided to the host device 100 through a response field Response illustrated in FIG. 14, but embodiments are not limited thereto.

[00163] In addition, in some embodiments, the error count values described above may be provided to the host device 100 through, for example, four sense data fields Sense Data[0], Sense Data[1], Sense Data[2], and Sense Data[3] illustrated in FIG. 14, but embodiments are not limited thereto.

[00164] In addition, in some embodiments, the parameters (e.g., the time offset value, the phase offset value, the voltage offset value, the information on the number of sampling operations, etc.) stored in the memory device 200 and utilized for performing the EOM operation may be provided to the host device 100 through, for example, fourteen sense data fields Sense Data[4] to Sense Data[17] illustrated in FIG. 14, but embodiments are not limited thereto.

[00165] In addition, in some embodiments, the response signal may include preset information. Such preset information may be referred to and be used to change signal driving characteristics of the host device 100 or change signal reception characteristics of the memory device 200.

[00166] In the memory system described above according to embodiments of the present disclosure, a separate external device to be attached to or detached from the memory device 200 to determine quality characteristics of signals transmitted and received between the host device 100 and the memory device 200 may be omitted, and the quality characteristics of the signals may be determined without utilization of such a separate external device. Further, in some embodiments, a signal line on which the EOM operation is performed is the same as a signal line on which the host device 100 and the memory device 200 exchange signals with each other. Accordingly, the EOM operation may be efficiently and reliably performed.

[00167] FIG. 15 is a flowchart illustrating an operation of a memory system according to some embodiments.

[00168] Hereinafter, for convenience of explanation, a further description of elements and technical aspects previously described may be omitted, and the description will focus primarily on differences from embodiments described above.

[00169] Referring to FIG. 15, the host device 100 transmits a command for requesting the memory device 200 to perform an EOM operation to the memory device 200 (S200). Then, the memory device 200 transmits a response to the WRITE BUFFER COMMAND to the host device 100 (S210).

[00170] Next, the memory device 200 transmits pattern data utilized to perform the EOM operation to the host device 100 (S220).

[00171] Referring back to FIG. 1, in some embodiments, the pattern data utilized to perform such an EOM operation may be stored in the nonvolatile memory storage 220 of the memory device 200 and then transmitted to the host device 100, but embodiments are not limited thereto.

[00172] That is, unlike an embodiment described above with reference to FIG. 8, in an embodiment according to FIG. 15, the host device 100 does not generate the pattern data utilized to perform the EOM operation, and rather, the pattern data stored in the memory device 200 may be used to perform the EOM operation.

5 **[00173]** Then, the host device 100 transmits EOM data including parameters utilized for performing the EOM operation and the pattern data received from the memory device 200 to the memory device 200 (S230). Then, the memory device 200 transmits a response to reception of the EOM data to the host device 100 (S240). The memory device 200 receiving the EOM data performs the EOM operation (S250), and the memory device 200
10 that has performed the EOM operation transmits a response signal including a result of performing the EOM operation to the host device 100 (S260).

[00174] FIG. 16 is a flowchart illustrating a method of performing an EOM operation according to some embodiments.

[00175] Referring to FIG. 16, an initial offset value is set (S300).

15 **[00176]** For example, referring to FIGS. 1 and 12, the host device 100 may set the offset values to be included in the EOM data header EDH (e.g., a value to be included in the phase selection field PHASE SELECT and/or a value to be included in the reference voltage control field VREF CONTROL), which are the parameters utilized for performing the EOM operation.

20 **[00177]** Then, the EOM operation is performed with the set offset value (S310). Then, an EOM result is identified (S320).

[00178] For example, the host device 100 and the memory device 200 may perform the EOM operation with the offset value described above and identify the EOM result.

[00179] When the EOM operation has not been performed for all offset values (NO in
25 S330), the offset value is changed (S340), the EOM operation is performed with the

changed offset value (S310), and an EOM result is identified (S320). That is, the EOM operation may be performed for a sufficient number of offset values to determine quality characteristics of signals transmitted and received between the host device 100 and the memory device 200.

5 **[00180]** When the EOM operation has been performed for all offset values (YES in S330), transmit parameters of a transmit end and receive parameters of a receive end of the host device 100 and the memory device 200 are set based on the EOM results (S350).

10 **[00181]** For example, the host device 100 may set transmit parameters of a transmit end related to signal transmission based on the EOM results, and then store the set transmit parameters in, for example, a PHY register of the host device 100.

[00182] In addition, the memory device 200 may also set receive parameters related to signal reception based on the EOM results, and then store the set receive parameters in, for example, a PHY register of the memory device 200.

15 **[00183]** In some embodiments, such receive parameters may be, for example, a CDR bandwidth, an amplitude of a receive end (TX/RX amplitude), etc., but embodiments are not limited thereto.

[00184] FIG. 17 is a flowchart illustrating an operation of a memory system according to some embodiments. FIGS. 18 to 25 are diagrams for describing an operation of a memory system according to some embodiments.

20 **[00185]** First, referring to FIG. 17, the host device 100 transmits a command for requesting information related to an EOM operation to the memory device 200 (S410).

25 **[00186]** In some embodiments, such a request command may be implemented in the form of a READ BUFFER COMMAND illustrated in FIG. 18 according to the JEDEC UFS standard. FIG. 18 is a diagram illustrating a command descriptor block (CDB) of the READ BUFFER COMMAND according to the JEDEC UFS standard.

[00187] In some embodiments, the information related to the EOM operation that the host device 100 requests from the memory device 200 using the READ BUFFER COMMAND may refer to, for example, information related to the EOM operation performed in the memory device 200 by the WRITE BUFFER COMMAND described above (e.g., the parameters utilized for performing the EOM operation, such as the offset information stored in the memory device 200 and the error count). However, embodiments are not limited thereto.

[00188] First, referring to FIGS. 1, 10, and 18, the UFS host controller 110 of the host device 100 may request the information related to the EOM operation from the UFS device controller 210 of the memory device 200 by setting a mode field Mode of the READ BUFFER COMMAND to 1F.

[00189] In some embodiments, operations of the UFS host controller 110 and operations of the UFS device controller 210 may be performed by controlling the UFS host controller 110 and the UFS device controller 210 by predetermined firmware, but embodiments are not limited thereto.

[00190] A value of the mode field Mode of the READ BUFFER COMMAND may be defined, for example, as described with reference to FIG. 10 above. Accordingly, the host device 100 may request the information related to the EOM operation from the memory device 200 by setting a set value of the mode field Mode of the READ BUFFER COMMAND to 1F, but embodiments are not limited thereto.

[00191] The set value of the mode field Mode for requesting the information related to the EOM operation may be modified into other set values (e.g., other set values set as Reserved in standard specifications, such as 1D).

[00192] Then, referring to FIG. 17, the memory device 200 transmits a response signal including the information related to the EOM operation to the host device 100 in response to the command for requesting the information related to the EOM operation (S420).

[00193] In some embodiments, when the host device 100 requests the information related to the EOM operation from the memory device 200 through the READ BUFFER COMMAND, the host device 100 may include an indication field indicating information to be included in the response signal from the memory device 200 in the READ BUFFER COMMAND. Although an embodiment that uses a buffer ID field BUFFER ID of the READ BUFFER COMMAND as such an indication field is described herein, embodiments are not limited thereto.

[00194] The memory device 200 may identify the buffer ID field BUFFER ID of the READ BUFFER COMMAND received from the host device 100, and transmit a response signal including information corresponding to the buffer ID field BUFFER ID among the information related to the EOM operation to the host device 100.

[00195] Hereinafter, this process will be described in further detail with reference to FIGS. 19 to 25.

[00196] FIG. 19 is a diagram illustrating a description of set values of the buffer ID field BUFFER ID of the READ BUFFER COMMAND.

[00197] Referring to FIG. 19, when the host device 100 desires that an error count value for an offset value of a specific coordinate is included in the response signal from the memory device 200, the host device 100 may set the buffer ID field BUFFER ID of the READ BUFFER COMMAND to 00 and transmit the READ BUFFER COMMAND to the memory device 200.

[00198] In this case, some fields of the READ BUFFER COMMAND transmitted from the host device 100 to the memory device 200 may include an offset value of a specific coordinate, as illustrated in FIG. 20.

[00199] That is, the host device 100 may write X-axis coordinate information (X-axis offset information) and Y-axis coordinate information (Y-axis offset information) as illustrated in FIG. 20 in a buffer offset field BUFFER OFFSET of the READ BUFFER COMMAND of FIG. 18, and transmit the READ BUFFER COMMAND to the memory device 200. The memory device 200 that has received the READ BUFFER COMMAND may include an error count value ERR_CNT corresponding to the received X-axis coordinate information (X-axis offset information) and Y-axis coordinate information (Y-axis offset information) in the response signal, as illustrated in FIG. 21, and transmit the response signal to the host device 100, as a response to the reception of the READ BUFFER COMMAND.

[00200] For example, when the dX and dY offset values illustrated in FIG. 4 have been included in the READ BUFFER COMMAND received from the host device 100, the memory device 200 may include error count values for the dX and dY offset values in the response signal and transmit the response signal to the host device 100.

[00201] In some embodiments, the memory device 200 may transmit the response signal to the host device 100 based on a data capacity that may be transmitted between the memory device 200 and the host device 100 at a certain time. For example, when the data capacity that may be transmitted between the memory device 200 and the host device 100 at a certain time is 12 bytes, the memory device 200 may include the error count value ERR_CNT corresponding to the received X-axis coordinate information (X-axis offset information) and Y-axis coordinate information (Y-axis offset information) in the response signal and transmit the response signal to the host device 100 in units of 12 bytes.

[00202] Referring back to FIG. 19, when the host device 100 desires that the offset values of the EOM operation performed in the memory device 200 are included in the response signal from the memory device 200, the host device 100 may set the buffer ID field BUFFER ID of the READ BUFFER COMMAND to 01 and transmit the READ BUFFER
5 COMMAND to the memory device 200.

[00203] For example, when the host device 100 desires that the parameters utilized for performing the EOM operation, such as the phase selection field PHASE SELECT, the reference voltage control field VREF CONTROL, and the number-of-sampling field NUMBER OF SAMPLING stored in the memory device 200 in an EOM performing
10 process and included in the EOM data header EDH of FIG. 11 are included in the response signal, the host device 100 may set the buffer ID field BUFFER ID of the READ BUFFER COMMAND to 01 and transmit the READ BUFFER COMMAND to the memory device 200.

[00204] The memory device 200 that has received the READ BUFFER COMMAND may
15 include the phase selection field PHASE SELECT, the reference voltage control field VREF CONTROL, the number-of-sampling field NUMBER OF SAMPLING, etc., stored in the memory device 200 in the EOM performing process in the response signal, as illustrated in FIG. 22, and transmit the response signal to the host device 100, as a response to the reception of the READ BUFFER COMMAND. In addition, in this case, the memory
20 device 200 may include an error count value ERR_CNT of the EOM operation performed using the corresponding phase selection field PHASE SELECT, reference voltage control field VREF CONTROL, and number-of-sampling field NUMBER OF SAMPLING in the response signal and transmit the response signal to the host device 100.

[00205] The memory device 200 may transmit the response signal to the host device 100
25 based on a data capacity that may be transmitted between the memory device 200 and the

host device 100 at a certain time. For example, when the data capacity that may be transmitted between the memory device 200 and the host device 100 at a certain time is 12 bytes, the memory device 200 may transmit the phase selection field PHASE SELECT, the reference voltage control field VREF CONTROL, and the number-of-sampling field
5 NUMBER OF SAMPLING stored in the memory device 200 and the error count value ERR_CNT of the EOM operation performed using the phase selection field PHASE SELECT, the reference voltage control field VREF CONTROL, and the number-of-sampling field NUMBER OF SAMPLING to the host device 100, in units of 12 bytes.

10 **[00206]** Referring back to FIG. 19, when the host device 100 desires that the receive parameters of the receive end of the memory device 200 are included in the response signal from the memory device 200, the host device 100 may set the buffer ID field BUFFER ID of the READ BUFFER COMMAND to 02 and transmit the READ BUFFER COMMAND to the memory device 200.

15 **[00207]** As described above with reference to FIG. 16, after the EOM operation is performed, the receive parameters related to the signal reception, such as the CDR bandwidth and the amplitude (TX/RX amplitude) of the receive end, may be set based on the EOM results, in, for example, the PHY register of the receive end of the memory device 200.

20 **[00208]** For example, when the host device 100 desires that the receive parameters set in, for example, the PHY register of the memory device 200 as a result of performing the EOM operation are included in the response signal, the host device 100 may set the buffer ID field BUFFER ID of the READ BUFFER COMMAND to 02 and transmit the READ BUFFER COMMAND to the memory device 200.

[00209] The memory device 200 that has received the READ BUFFER COMMAND may include the receive parameters set in the PHY register of the memory device 200 in the response signal, as illustrated in FIG. 23, and transmit the response signal to the host device 100, as a response to the reception of the READ BUFFER COMMAND.

5 **[00210]** The receive parameters of the receive end of the memory device 200 may include, for example, a receive amplitude (RX amplitude) value setting a receive equalizer 251 included in a UIC layer 250 of a memory device 200 illustrated in FIG. 24, a CDR bandwidth setting a clock recovery circuit 253b of the memory device 200, etc., but embodiments are not limited thereto.

10 **[00211]** The transmit parameters of the transmit end of the host device 100 may include, for example, setting values for setting a serializer 152, a PLL 154, and a transmit equalizer 156 included in a UIC layer 150 of a host device 100 illustrated in FIG. 24, but embodiments are not limited thereto.

[00212] In addition, in this case, the memory device 200 may include the error count value
15 ERR_CNT of the EOM operation performed in the memory device 200 in the response signal and transmit the response signal to the host device 100.

[00213] The memory device 200 may transmit the response signal to the host device 100 based on a data capacity that may be transmitted between the memory device 200 and the host device 100 at a certain time. For example, when the data capacity that may be
20 transmitted between the memory device 200 and the host device 100 at a certain time is 12 bytes, the memory device 200 may transmit the receive parameters set in, for example, the PHY register of the memory device 200 and the error count value ERR_CNT of the EOM operation performed in the memory device 200 to the host device 100 in units of 12 bytes.

[00214] Referring back to FIG. 19, when the host device 100 desires that the parameters
25 utilized for performing the EOM operation, such as the phase selection field PHASE

SELECT, the reference voltage control field VREF CONTROL, and the number-of-sampling field NUMBER OF SAMPLING stored in the memory device 200 and the receive parameters of the receive end of the memory device 200 are included in the response signal from the memory device 200, the host device 100 may set the buffer ID
5 field BUFFER ID of the READ BUFFER COMMAND to 03 and transmit the READ BUFFER COMMAND to the memory device 200.

[00215] That is, when both of a response when the buffer ID field BUFFER ID is 01 and a response when the buffer ID field BUFFER ID is 02 are utilized, the host device 100 may set the buffer ID field BUFFER ID of the READ BUFFER COMMAND to 03 and transmit
10 the READ BUFFER COMMAND to the memory device 200.

[00216] The memory device 200 that has received the READ BUFFER COMMAND may include the parameters utilized for performing the EOM operation, such as the phase selection field PHASE SELECT, the reference voltage control field VREF CONTROL, and the number-of-sampling field NUMBER OF SAMPLING and the receive parameters set in
15 the PHY register of the memory device 200 in the response signal, as illustrated in FIG. 25, and transmit the response signal to the host device 100, as a response to the reception of the READ BUFFER COMMAND.

[00217] In addition, in this case, the memory device 200 may include the error count value ERR_CNT of the EOM operation performed in the memory device 200 in the response
20 signal and transmit the response signal to the host device 100.

[00218] The memory device 200 may transmit the response signal to the host device 100 based on a data capacity that may be transmitted between the memory device 200 and the host device 100 at a certain time. For example, when the data capacity that may be transmitted between the memory device 200 and the host device 100 at a certain time is 12
25 bytes, the memory device 200 may transmit the phase selection field PHASE SELECT, the

reference voltage control field VREF CONTROL, and the number-of-sampling field
NUMBER OF SAMPLING stored in the memory device 200, the receive parameters set in
the PHY register of the memory device 200, and the error count value ERR_CNT of the
EOM operation performed in the memory device 200 to the host device 100, in units of 12
5 bytes.

[00219] As described above, in an embodiment, various parameters applied to the EOM
operation performed in the memory device 200 and the receive parameters set in the receive
end of the memory device 200 may be easily identified using the READ BUFFER
COMMAND, such that the EOM may be efficiently and reliably performed.

10 **[00220]** FIG. 26 is a diagram illustrating a memory system according to embodiments.
Hereinafter, for convenience of explanation, a further description of elements and technical
aspects previously described may be omitted, and the description will focus primarily on
differences from embodiments described above.

[00221] Referring to FIG. 26, in an embodiment, the UIC layer 150 of the host device 100
15 performs the EOM operation described above. For example, the UIC layer 150 of the host
device 100 may perform the EOM operation on a pair of differential output signals
DOUT_T and DOUT_C received from the memory device 200.

[00222] For example, while embodiments in which the host device 100 transmits data and
the memory device 200 receives the data have been described above, in an embodiment
20 according to FIG. 26, the memory device 200 transmits data and the host device 100
receives the data. In this case, the above description for the transmit end may be applied to
the memory device 200, and the above description for the receive end may be applied to the
host device 100. That is, the role of the host device 100 described above may be
exchanged with the role of the memory device 200 described above.

[00223] FIG. 27 is a diagram illustrating a memory system according to embodiments. Hereinafter, for convenience of explanation, a further description of elements and technical aspects previously described may be omitted, and the description will focus primarily on differences from embodiments described above.

5 **[00224]** Referring to FIG. 27, in an embodiment, both of the UIC layer 150 of the host device 100 and the UIC layer 250 of the memory device 200 perform the EOM operation described above.

[00225] In this case, the above description for the transmit end may be applied to both the host device 100 and the memory device 200, and the above description for the receive end
10 may also be applied to both the host device 100 and the memory device 200.

[00226] As is traditional in the field of the present disclosure, embodiments are described, and illustrated in the drawings, in terms of functional blocks, units and/or modules. Those skilled in the art will appreciate that these blocks, units and/or modules are physically implemented by electronic (or optical) circuits such as logic circuits, discrete components, microprocessors, hard-wired circuits, memory elements, wiring connections, etc., which
15 may be formed using semiconductor-based fabrication techniques or other manufacturing technologies. In the case of the blocks, units and/or modules being implemented by microprocessors or similar, they may be programmed using software (e.g., microcode) to perform various functions discussed herein and may optionally be driven by firmware and/or software. Alternatively, each block, unit and/or module may be implemented by
20 dedicated hardware, or as a combination of dedicated hardware to perform some functions and a processor (e.g., one or more programmed microprocessors and associated circuitry) to perform other functions.

[00227] While the present disclosure has been particularly shown and described with
25 reference to embodiments thereof, it will be understood by those of ordinary skill in the art

that various changes in form and detail may be made therein without departing from the spirit and scope of the present disclosure as defined by the following claims.

What is claimed is:

1. A method of operating a host device, comprising:
transmitting a read command that requests information related to an eye open
5 monitor (EOM) operation performed in a memory device to the memory device; and
receiving a response signal including the information related to the EOM operation
performed in the memory device from the memory device.

2. The method of claim 1, wherein the read command includes a READ
10 BUFFER COMMAND.

3. The method of claim 2, wherein a mode field of the READ BUFFER
COMMAND is set to 1F.

15 4. The method of claim 1, wherein the read command includes an indication
field indicating information to be included in the response signal among the information
related to the EOM operation performed in the memory device.

5. The method of claim 4, wherein the read command includes a READ
20 BUFFER COMMAND, and
the indication field includes a buffer ID field.

6. The method of claim 4 or claim 5, wherein the read command includes an
offset value, and
25 the response signal includes an error count value corresponding to the offset value.

7. The method of claim 4 or claim 5, wherein the response signal includes an offset value of the EOM operation performed in the memory device.

5 8. The method of claim 4 or claim 5, wherein the response signal includes a receive parameter of a receive end of the memory device.

9. The method of claim 4 or claim 5, wherein the response signal includes an offset value of the EOM operation performed in the memory device and a receive parameter
10 of a receive end of the memory device.

10. A method of operating a memory device, comprising:
receiving a read command that requests information related to an eye open monitor
(EOM) operation performed in the memory device from a host device;
15 identifying an indication field of the read command; and
transmitting a response signal including information corresponding to a value of the
indication field among the information related to the EOM operation to the host device.

11. The method of claim 10, wherein the read command includes a READ
20 BUFFER COMMAND.

12. The method of claim 11, wherein a mode field of the READ BUFFER
COMMAND is set to 1F.

13. The method of claim 10, wherein the read command includes a READ BUFFER COMMAND, and

the indication field includes a buffer ID field.

5 14. The method of claim 13, wherein in response to the indication field having a certain value, the response signal includes an error count value corresponding to an offset value included in the read command.

10 15. The method of claim 13, wherein in response to the indication field having a certain value, the response signal includes an offset value of the EOM operation performed in the memory device and an error count value of the EOM operation performed in the memory device.

15 16. The method of claim 13, wherein in response to the indication field having a certain value, the response signal includes a receive parameter of a receive end of the memory device and an error count value of the EOM operation performed in the memory device.

20 17. The method of claim 13, wherein in response to the indication field having a certain value, the response signal includes an offset value of the EOM operation performed in the memory device, a receive parameter of a receive end of the memory device, and an error count value of the EOM operation performed in the memory device.

18. A memory system, comprising:

25 a host device comprising a host controller; and

a memory device comprising a device controller,

wherein the host controller transmits a read command that requests information related to an eye open monitor (EOM) operation performed in the memory device to the memory device,

5 the read command includes an indication field indicating information to be included in a response signal among the information related to the EOM operation performed in the memory device, and

the device controller transmits the response signal including information corresponding to a value of the indication field among the information related to the EOM
10 operation to the host device in response to the read command.

19. The memory system of claim 18, wherein the read command includes a READ BUFFER COMMAND, and

the indication field includes a buffer ID field of the READ BUFFER COMMAND.

15 20. The memory system of claim 19, wherein the device controller transmits at least one of an offset value of the EOM operation performed in the memory device and a receive parameter of a receive end of the memory device to the host device, according to the buffer ID field.