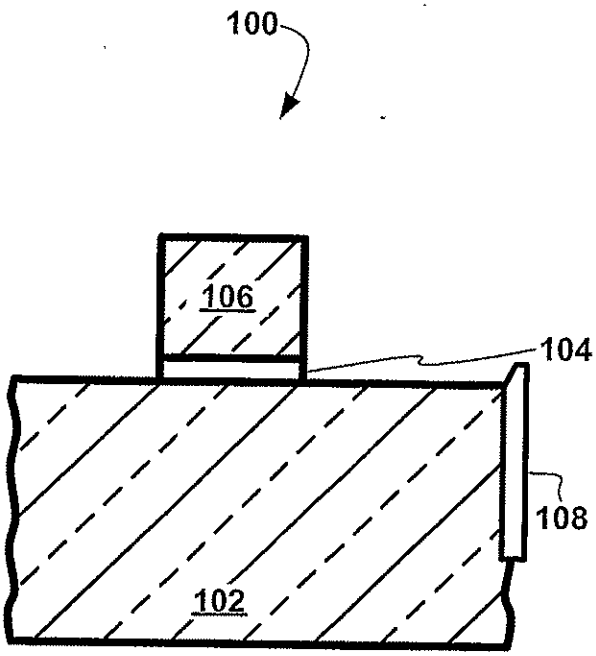


FIG. 1

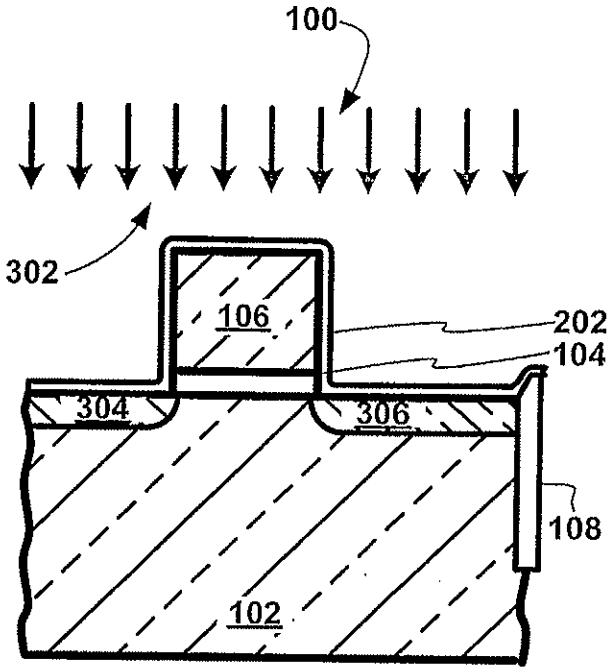


FIG.3

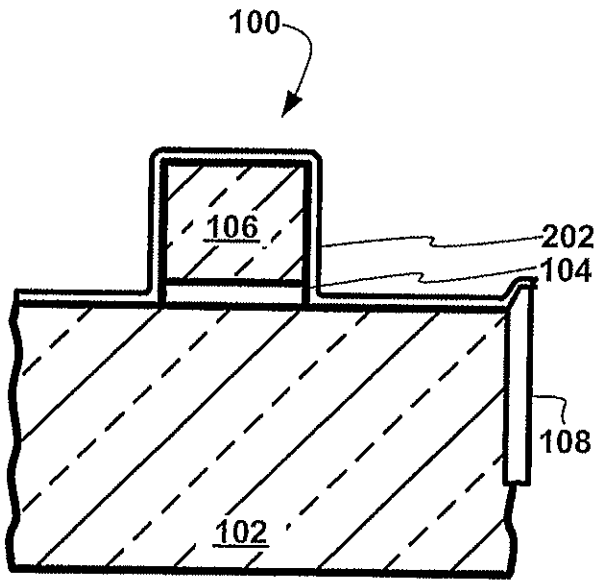


FIG. 2

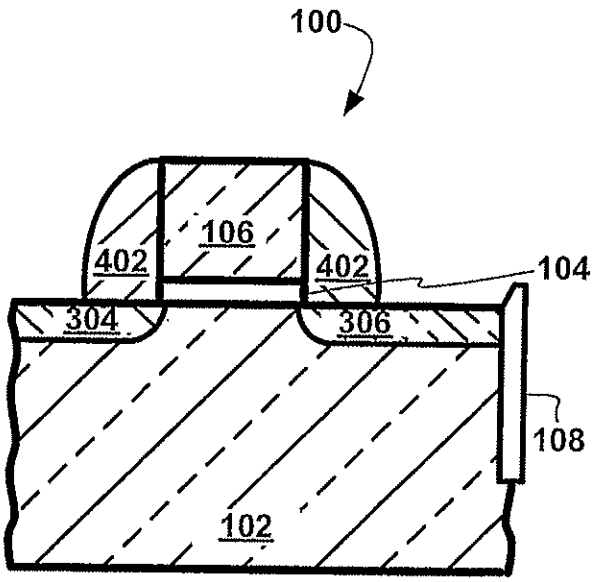


FIG. 4

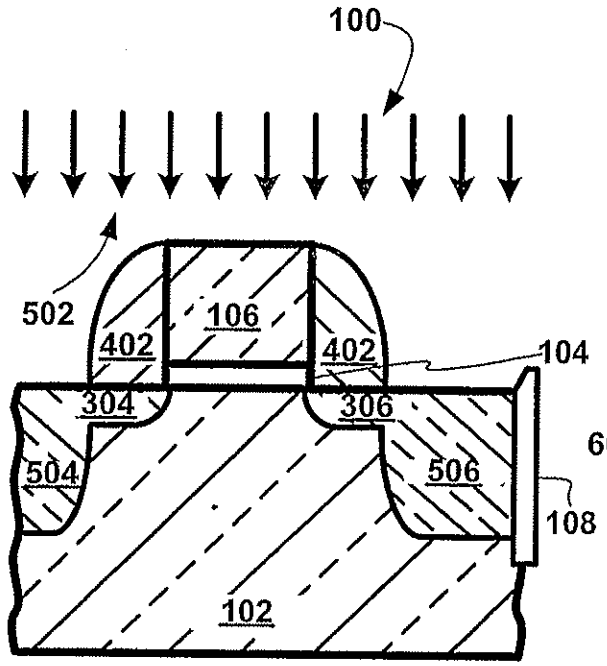


FIG. 5

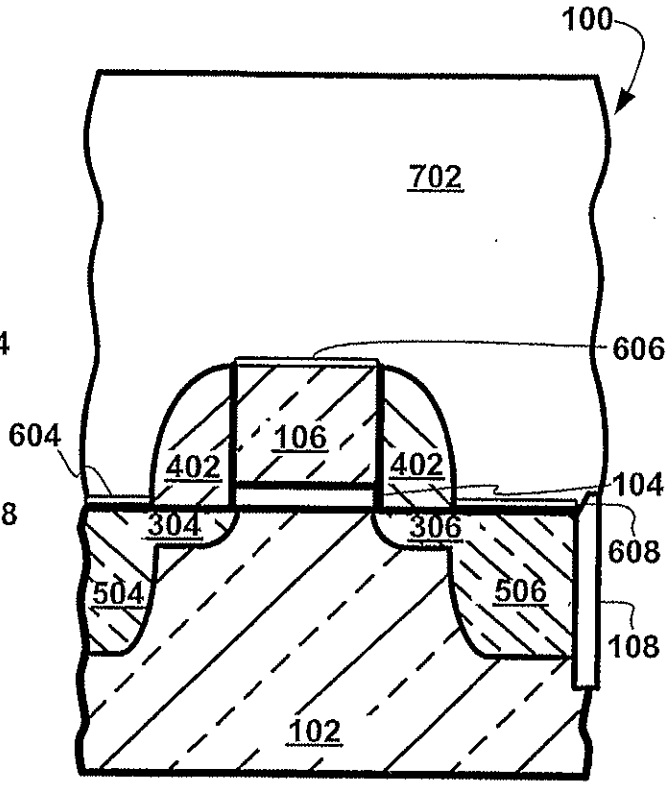


FIG. 7

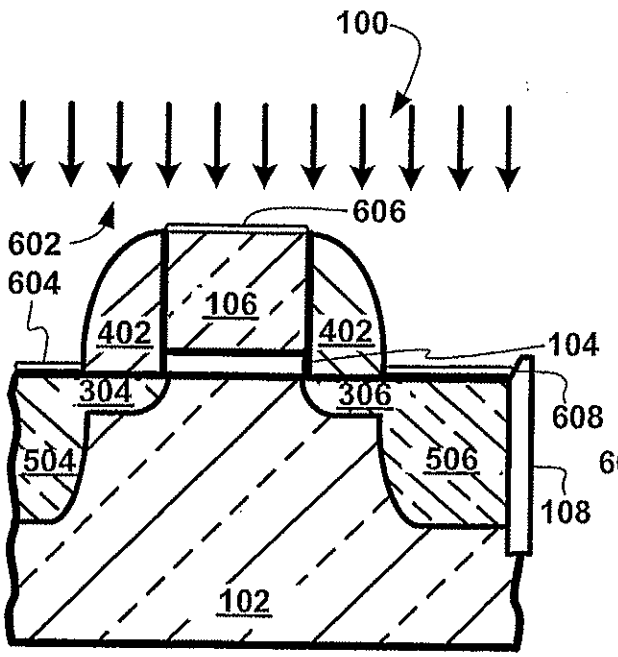


FIG. 6

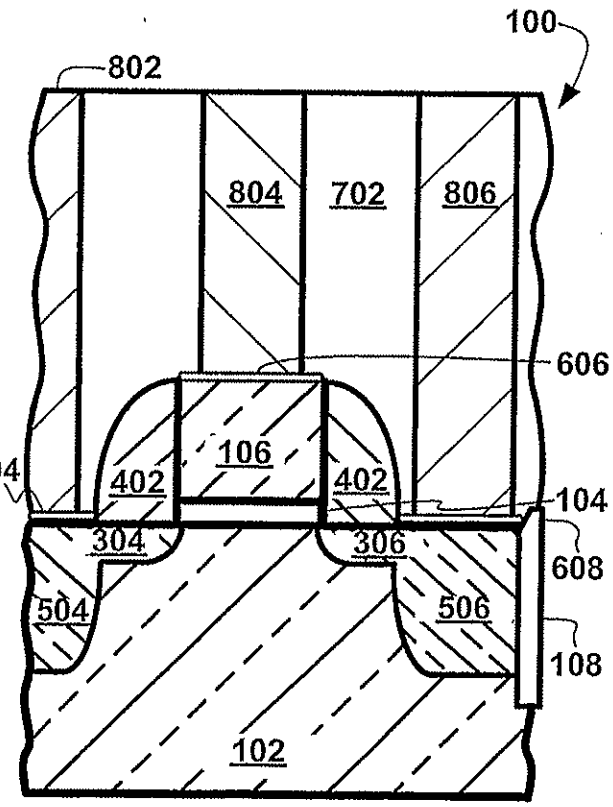


FIG. 8

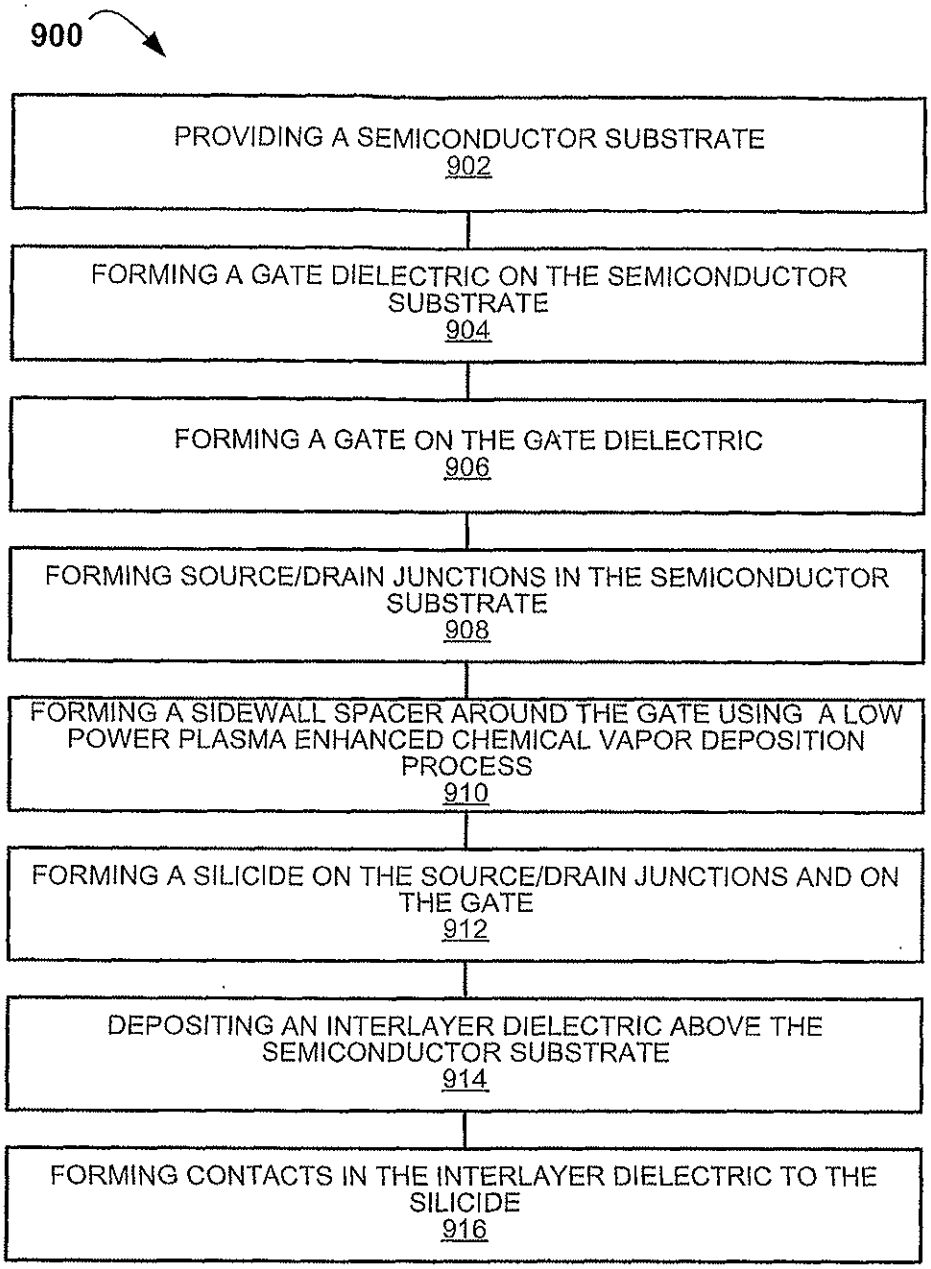

900
PROVIDING A SEMICONDUCTOR SUBSTRATE
902
FORMING A GATE DIELECTRIC ON THE SEMICONDUCTOR SUBSTRATE
904
FORMING A GATE ON THE GATE DIELECTRIC
906
FORMING SOURCE/DRAIN JUNCTIONS IN THE SEMICONDUCTOR SUBSTRATE
908
FORMING A SIDEWALL SPACER AROUND THE GATE USING A LOW POWER PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION PROCESS
910
FORMING A SILICIDE ON THE SOURCE/DRAIN JUNCTIONS AND ON THE GATE
912
DEPOSITING AN INTERLAYER DIELECTRIC ABOVE THE SEMICONDUCTOR SUBSTRATE
914
FORMING CONTACTS IN THE INTERLAYER DIELECTRIC TO THE SILICIDE
916

FIG. 9