

SPECIFICATION Camera focussing system

The present invention relates to a focussing system for a photographic or cinematographic camera having a lens for adjusting the lens in accordance with the distance between a subject to be photographed and the camera and/or for indicating when the lens is focussed, the system including a pulse generator circuit, a radiation emitting element driven by the pulse generator circuit for producing a measuring beam, a pair of radiation receiving elements for receiving radiation produced by the radiation emitting elements, and a signal processing circuit responsive to the radiation receiving elements.

In such a system, where the measuring beam produced by the radiation emitting element is reflected by a subject to be photographed which is distant from the camera or which is poorly reflecting the signal received by the radiation receiving elements may be very low and cause difficulty in signal processing. This can be overcome by increasing the intensity of the measuring beam but this results in greater expense and a greater energy requirement. Under some circumstances, the signal generated by the receiving elements upon receiving the reflected radiation may be of the same order as the noise generated by the receiving elements and also by the processing circuit.

According to the present invention there is provided in a focussing system for adjusting a photographic or cinematographic camera lens in accordance with the distance between a subject to be photographed and the camera and/or for indicating when the lens is focussed, the system including a pulse generator circuit, a radiation emitting element driven by the pulse generator circuit for producing a measuring beam, radiation receiving means for receiving, in use, the radiation produced by the radiation emitting element and reflected back from the subject to be focussed, a signal processing circuit responsive to the radiation receiving means, an integrator circuit responsive to the output of the signal processing circuit, and a threshold circuit responsive to the output of the integrator circuit and including at least one memory element, the threshold circuit being set to a predetermined threshold value, the integrator circuit being reset at the end of each measuring cycle, and each measuring cycle including a number of pulses produced by the pulse generator circuit.

The provision of the integrator circuit results in the noise being integrated over a period of time and thereby suppressed so that only a limited noise component remains. An output signal will only be transmitted to an output stage when the threshold value of the threshold circuit is exceeded. Where the intensity of the signal falling on the radiation receiving means is low, a large number of measuring pulses will be required before the threshold value is exceeded whilst where the intensity of the signal falling on the

radiation receiving means is relatively large only a relatively low number of measuring pulses is required. The provision of the integrator circuit increases the sensitivity of the system and increases its resolution. Also the integrator circuit to some extent separates the output signal of the radiation receiving elements from the background noise signal.

Conveniently, the radiation receiving means comprises a pair of radiation receiving elements. The integrator circuit may comprise two individual integrator sections, each section being associated with a respective one of the receiving elements and, under the control of pulses produced by the pulse generator circuit, each integrator section being rendered responsive to the output of the signal processing circuit when a pulse is expected from its associated receiving element. By rendering the integrator sections responsive to the output of the signal processing circuit when the pulse is expected, the output signal of the receiving elements is transmitted to the integrator sections without having its AC component removed.

Each individual integrator section may comprise an operational amplifier having a feed back integration capacitor and the threshold circuit may comprise a pair of voltage comparators, each of which is associated with a respective integrator section.

Conveniently said at least one memory element comprises at least one flip-flop responsive to the output signal of each voltage comparator and transfers said output signal to an output stage upon receiving a control signal at the end of each measuring cycle.

The pulse generator circuit may include a logic circuit clocked at a predetermined frequency.

The duration of each measuring cycle may be determined by first counter receiving clock pulses derived from the pulse generator circuit, the counter producing a control signal each time it receives a predetermined number of clock pulses.

The pulse generator circuit may be connected to the input of a delay circuit, the output of which provides the clock pulses for the first counter, and the integrator circuit may be rendered responsive to the output of the signal processing circuit under the control of the output signal of the delay circuit. Conveniently, the system includes a second counter receiving clock pulses derived from the pulse generator circuit and responsive to said flip-flops, each flip-flop being connected to its associated voltage comparator by a gate, during each measuring cycle the second counter being enabled upon receiving a signal from one of the flip-flops corresponding to the input of its associated voltage comparator exceeding the threshold value, and thereafter upon counting a pre-determined or variable number of pulses issuing a blocking signal to said gates.

In one arrangement, the second counter issues a blocking signal after counting a predetermined number of pulses and in this arrangement a regulating circuit is provided for controlling the

radiation emitting element, the regulating circuit reducing the radiation intensity of the radiation emitting element in at least the close-up range of the camera in accordance with the intensity of the radiation incident on the receiving element so that this intensity does not exceed a predetermined value.

The intensity of the radiation incident on the receiving element may be less than or equal to a predetermined tolerance value.

In another arrangement, the radiation intensity of the radiation emitting element is uncontrolled and the number of pulses counted by the second counter before issuing a blocking signal is varied in accordance with the amplitude of the output signals of the radiation receiving elements by a coding circuit in such a manner that, during each measuring cycle, the ratio of the number of pulses counted by the second counter before issuing a blocking signal to the number of pulses produced by the pulse generator circuit before the output of one of the integrator sections exceeds the threshold value does not exceed a predetermined value. Conveniently, where the integrator circuit comprises a pair of individual integrator sections, said at least one memory element comprises a pair of D-flip-flops associated with each integrator section, in each pair the first flip-flop having its clock input response to the output of the associated integrator section and its Q-output connected to the D-input of the second flip-flop, and the clock input of the second flip-flop receiving a control signal at the end of each measuring cycle.

The Q output of the first flip-flop of each pair may be connected by an OR-gate to the first input of a further gate, the second input of which is responsive to the pulse generator circuit and the third input of which is connected by an inverter to the output of the second counter, the output of the further gate being connected to the clock input of the second counter.

Conveniently, the signal processing circuit includes sections common to both radiation receiving elements, the common sections being connected between first and second multiplex stages controlled by the pulse generator circuit and the clock input of the second counter is connected to the pulse generator circuit via a frequency halving element.

The provision of multiplex stages greatly reduces the chance of an interference signal being transmitted to the integrator circuit. Further, by providing that the multiplex stages only transmit a signal when a pulse is expected from one of the receiving elements, optimum signal integration is achieved and the removal of a wanted signal component is avoided. Further, by connecting the second counter to the pulse generator circuit by a frequency halving element, it is ensured that the second counter issues its blocking signal after an even number of measuring pulses have been emitted with the result that the output signals of the two receiving elements always receive equal signal processing.

The present invention will now be described in more detail, by way of example, with reference to Figures 1 and 2 of the accompanying drawings which show a circuit diagram of a focussing system embodying the present invention.

Referring now to Figure 1, the system there shown comprises a battery 1, the negative pole of which is connected to a negative supply line and the positive pole of which is connected by a switch 2 to the anode of the diode 5. The cathode of diode 5 is connected through a resistor 6 to a positive supply line. A capacitor 3 is connected in parallel with battery 1 and switch 2 and a further capacitor 4 is connected between the positive and negative supply lines, the capacitors 3 and 4, the diode 5 and the resistor 6 serving to stabilise the voltage between the positive and negative supply lines. Two equal value resistors 7 and 8 are connected in series between the positive and negative supply lines and the junction between these two resistors is connected to an earth line, the potential of which is exactly mid-way between the positive and negative supply lines. The system includes a pair of radiation receiving elements in the form of infra-red sensitive diodes 9, 10. The cathode of infra-red sensitive diode 9 is connected to the inverting input of an operational amplifier 11, the non-inverting input of which is connected to earth, and the cathode of infra-red sensitive diode 10 is connected to the inverting input of an operational amplifier 12, non inverting input of which is connected to earth.

A pair of resistors 13 and 14 connected in series provide a feed-back connection between the output of amplifier 11 and its inverting input and a further pair of resistors 15 and 16 connected in series provide a feedback connection between the output of amplifier 12 and its non-inverting input. These resistors determine the amplification factor of amplifiers 11 and 12. The junction of resistors 13 and 14 and the junction of resistors 15 and 16 are connected to earth by capacitors 17 and 18 respectively. As the impedance of capacitors 17 and 18 decreases with increasing frequency, the amplification factor of the two amplifiers 11 and 12 increases with increasing frequency. It is preferred that the resistors 13 and 14 have identical values to the resistors 15 and 16, and also that the capacitors 17, 18 are of equal value.

The output of amplifier 11 is connected by a coupling capacitor 19 to the inverting input of an operational amplifier 20, the output of which is connected by a feed-back resistor 21 to its non-inverting input, and the non-inverting input is connected to earth by a resistor 22. The resistors 21 and 22 determine the amplification factor of this amplifier, which functions as an AC amplifier.

Likewise, the output of amplifier 12 is connected by a coupling capacitor 24 to the non-inverting input of an operational amplifier 23, the output of which is connected by a feed back resistor 25 to its non-inverting input and the non-inverting input of which is connected to earth by a resistor 26. The resistors 25 and 26

determine the amplification factor of this amplifier and this amplifier also functions as an AC amplifier.

The outputs of amplifiers 20 and 23 are connected respectively to switching elements 28 and 29 of a first multiplex stage 27. The output of switching elements 28 and 29 are commonly connected to the input of a high-pass active filter comprising an operational amplifier 30, resistors 31 and 32, and capacitors 33 and 34. The high-pass filter is arranged so that interference signals of mains frequency and also interference signals from incandescent and fluorescent lamps having a frequency which is double mains frequency are filtered out.

The high-pass filter 30 to 34 is connected by a coupling capacitor 35 to an AC amplifier consisting of an operational amplifier 36 and feed back resistors 37 and 38.

The output of the operational amplifier 36 is connected to the inputs of two switching elements 40 and 41 of a second multiplex stage 40. The output of switching element 40 is connected to a terminal B and the output of switching element 41 is connected to a terminal C.

The amplifiers 11, 12, 20, 23, 30 and 36 together with their associated elements form a signal processing circuit.

The system further includes a pulse generator circuit comprising a square wave pulse generator 42, the output of which is connected to the clock input of a counter 43. The output of pulse generator 42 and also the Q-four output counter 43 are connected to the two inputs of an AND-gate 34, the output of which is connected to the reset input R of counter 43. The Q-three output of counter 43 is connected to the clock input of a D-flip-flop 45, the Q-output of which is connected to its D input. The elements 43 and 44 thus function as a logic circuit dividing the output of pulse generator 42 and the D-flip-flop 45 functions as a frequency halving element.

The Q output of flip-flop 45 is connected to the control terminal of switching element 28 and also to one input of an AND-gate 46. The Q-output of flip-flop 45 is connected to the control terminal of switching element 29 and to one input of an AND-gate 47.

The remaining inputs of AND-gates 46 and 47 are connected commonly to the output of a delay circuit 48, having timing elements 49 and 50. The input of the delay circuit 48 to 50 is connected to the output of an AND-gate 51, one input of which is connected to the Q-four output of the counter 43 and the other input of which is connected to a timing circuit comprising a capacitor 52 and a resistor 53.

The output of AND-gate 51 is also connected by a resistor 54 to the base of a transistor 55, the emitter of which is connected to the base of an output transistor 56. The collector of transistor 56 is connected to the cathode of an infrared emitting diode 57, the anode of which is connected to the positive terminal of battery 1 through switch 2.

The emitter of transistor 56 is connected to the

negative supply rail by a resistor 58.

The infra-red emitting diode 57 forms a radiation emitting element and is arranged in the camera, so that, in use, it emits a measuring beam towards the subject to be photographed. The infra-red sensitive diodes 9 and 10 are arranged to receive the infra-red radiation reflected back from the subject to the camera. The diodes 9 and 10 are located behind a lens, not shown, which is coupled to the camera focussing system and which causes the received radiation to fall equally on the two diodes 9 and 10 when the main objective lens of the camera is focussed.

The output of AND-gate 47 is connected to the switching element 41 and the output of AND-gate 46 is connected to the switching element 40 of the second multiplex stage 39.

In order to regulate the intensity of the radiation emitted by the diode 57, a regulating circuit is provided. This regulating circuit comprises a pair of resistors 60 and 60' connected in series as a potential divider between the positive and negative supply lines, the junction of resistors 60 and 60' being connected by a capacitor 59 to the output of amplifier 36 and also to the anode of a diode 61, the cathode of which is connected to the negative supply line by a capacitor 62 and a resistor 63, connected in parallel, and also to the base of a transistor 64. The collector of transistor 64 is connected to the positive supply line and the emitter is connected to the base of a transistor 65. The collector of transistor 65 is connected to the base of transistor 55 and the emitter of transistor 65 is connected to the negative supply line.

In the regulating circuit, the transistor 65, and consequently the transistor 56, is controlled in accordance with the intensity of the radiation falling on the diodes 9 and 10. Within the close-up range of the camera, the regulating circuit ensures that the intensity of the radiation falling on the diodes 9 and 10 has an almost constant value, the actual value being controlled within a narrow tolerance range.

The output of switching element 40 is connected by terminal B to the input of an integration section, which forms one half of an integrator circuit, and which comprises an operational amplifier 66, a feed back integration capacitor 67 and a resistor 68. The output of the integration section 66 to 68 is connected to a voltage comparator comprising an operational amplifier 69 and a pair of resistors 70 and 71 connected in series between the positive supply line and earth and functioning as a potential divider, the junction of resistors 70 and 71 being connected to the non-inverting input of amplifier 69 so as to establish its threshold voltage. The output of amplifier 69 is connected to earth by a resistor 72. The output of amplifier 66 is connected to earth by the emitter-collector part of a transistor 73, the transistor 73 functioning as a semi-conductor switch element.

The output of the voltage capacitor 69 to 72 is connected to one input of an AND-gate 74.

The output AND-gate 74 is connected to the

clock input of a D-flip-flop 75. The D input of the flip-flop 75 is connected by terminal A to the positive supply line. The re-set input of the D-flip-flop 75 is connected to a delayed circuit consisting of gate 76 and 77, resistors 78 and 79, and capacitors 80 and 81.

The base of transistor 73 is connected by a resistor 82 to the same point on the delay circuit 76 to 79. The input of the delay circuit 76 to 79 is connected to the Qm of a counter 83, the reset input R of which is connected to the output of the delay circuit 76 to 79. The clock input of counter 83 is connected by way of terminal E to the output of the delay circuit 48 to 50.

The Qm output of counter 83 is connected to the clock input of a D-flip-flop 85, the D input of which is connected to the Q output of the flip-flop 75.

As will be explained, the counter 83 determines the duration of each measuring cycle of the focussing system.

The Qm output of counter 83 is also connected to the reset input of a counter 85.

The switching element 41 of the second multiplex stage 39 is connected by way of terminal C to the input of a second integrator section comprising an operational amplifier 86, a feed-back integration capacitor 76 and a resistor 88. The first and second integrator sections together form an integrator circuit. The resistor 88 is connected between the inverting input of amplifier 86 and terminal C and the non-inverting input of amplifier 86 is connected to earth. The capacitors 67 and 87 are of equal value, the resistors 68 and 88 are of equal value, and the amplifiers 66 and 86 are of identical structure. The output of amplifier 86 is connected to a voltage comparator comprising an amplifier 89, and a pair of resistors 90 and 91 connected in series between the positive supply line and earth and functioning as a potential divider, the junction of these two resistors being connected to the non-inverting input of amplifier 89 to establish its threshold value. A resistor 92 is connected between the output of amplifier 89 and earth. The voltage comparator 89 to 92 has the same threshold value as the voltage comparator 69 to 72. The output of amplifier 86 is connected to earth by the collector emitter path of transistor 93, which functions as a semi-conductor switch element.

The base of transistor 93 is connected by a resistor 94 to the delay circuit 76 to 81.

The output of amplifier 99 is connected to one input of an AND-gate 95.

The output of AND-gate 95 is connected to the clock input of a D-flip-flop 96, the reset input of which is connected to the delay circuit 76 to 81 and the D-input of which is connected to the positive supply line. The Q-output of the D-flip-flop 96 is connected to the D-input of a flip-flop 97, the clock input of which is connected to the Qm output of counter 83.

The two voltage comparators described above together with the flip-flops 75, 84, 96, and 97

form a threshold circuit, with the flip-flop acting as memory element.

The Q-output of flip-flop 75 and the Q-output of flip-flop 96 are connected to the two inputs of an OR-gate 98, the output of which is connected to one input of an AND-gate 99.

The second input of AND-gate 99 is connected by terminal F to the Q-output of D-flip-flop 45. The third input of AND-gate 99 is connected by an inverter 100 to the Qm output of counter 85. In addition, the output of inverter 100 is also connected to the second input of AND-gate 74 and 95.

The Q-output of flip-flop 84 is connected to one input of an AND-gate 101, the second input of which is connected to Q-output of flip-flop 97. The output of the AND-gate 101 is connected by a resistor 102 to the base of a transistor 103, the collector of which is connected by a light-emitting diode 104 and a resistor 105 to the positive supply line, and the emitter of which is connected to the negative supply line. The light emitting diode 104 indicates to the user of the camera, when it is energised, that the lens must be rotated in the direction of the arrow in order to focus it.

The Q-output of flip-flop 84 is connected to one input of an AND-gate 106, the second input of which is connected by a switch 107 and a resistor to the negative supply line. The output of AND-gate 106 is connected by a resistor 108 to the base of a transistor 109, the collector of which is connected by a light-emitting diode 110 and a resistor 111 to the positive supply line, and the collector of which is connected through a resistor to the negative supply line. The light emitting diode 101 indicates to the user of the camera, when it is energised, that the lens must be rotated in the direction indicated in order to obtain focus.

During each measuring cycle, pulses generated by the infra-red sensitive diodes 9 and 10 are processed in the signal processing circuit and then transmitted alternately by the second multiplex stage 39 to the two integrator sections 66 to 68 and 86 to 88, the pulses being integrated at the outputs of these two sections. After receiving a number of pulses, the number depending on the amplitude of the pulses, the output of one of the integrator sections 66 to 68 or 86 to 88 will reach the threshold value of its associated voltage comparator 69 to 72 or 89 to 92. For example, if the output of the integrator section 66 to 68 reaches the threshold value of voltage comparator 69 to 72, this comparator will apply a logic "one" signal to AND-gate 74, which consequently applies a clock pulse to the clock-input of D-flip-flop 75, thereby setting this flip-flop.

Consequently, the OR-gate 98 applies a logic "one" signal to the associated input of AND-gate 99. As the Qm output of counter 85 is "zero" the inverter 100 applies a logic "one" signal to its associated input of AND-gate 99. Consequently, each time the Q-output of flip-flop 45 changes from logic "nought" to logic "one" a clock pulse is applied to counter 85, counter 85 subsequently counting these pulses.

If the threshold voltage of voltage comparator 89 to 92 is reached before counter 85 completes its counting cycle, the D-flip-flop 96 receives a clock pulse thereby setting the flip-flop. When the counter 85 reaches the end of its counting cycle, a logic "one" signal appears at its Qm-output and inverter 100 applies a blocking signal to AND-gate 74 and 95. This prevents the counter 85 from receiving further clock pulses and it also prevents further clock pulses being applied to flip-flops 75 and 96.

At the end of each measuring cycle, counter 83 applies a control signal to the clock input of flip-flops 84 and 97, thereby setting these flip-flops. A logic "nought" signal is applied to the input of both AND-gates 101 and 106 with the result that both transistors 103 and 109 are turned off. Consequently, diodes 105 and 110 are not energised and this indicates to the camera user that the lens is in focus.

Switch 107 is closed when the lens is at its infinity setting. When switch 107 is open, the associated input of AND-gate 106 is connected by a resistor 102 to the positive supply line.

In general, if one of the flip-flops 75 or 96 is first set and then the other flip-flop is set before the counter 85 has completed its counting cycle, this indicates that the lens is in focus. If the other flip-flop is not set before the counter 85 completes its counting cycle the AND-gates 74 and 95 will be blocked and prevent clock pulses being applied to the flip-flop 75 and 96. Consequently, the end of the counting cycle of the counter 83, one of the AND-gates 101 and 106 receives a logic "one" signal and consequently one of the diodes 105 to 110 is energised.

On reaching the end of the measuring cycle as determined by counter 83, transistors 73 and 93 are turned on and so the integration capacitors 67 and 87 are discharged. Also, a reset pulse is applied, after a short delay, to the flip-flop 75 and 96. Counter 85 is also reset by a reset pulse from counter 83.

Since at least in the close up range of the camera the intensity of a signal falling on the diodes 9 and 10 is maintained at a substantially constant value, one of the voltage comparators 69 to 72 or 89 to 92 will reach its threshold value within a period which has a substantially constant value. After one of the voltage comparators has reached its threshold value, the other voltage comparator had a tolerance period, as determined by the counter 85, in which it may or may not reach its threshold value.

In an alternative embodiment of the present invention, not shown, the radiation intensity of the diode 57 is not controlled. In this embodiment, the number of pulses counted by the counter 85 before it issues its blocking signal to AND-gates 74 and 95 is varied in accordance with the amplitude of the output signals of the diodes 9 and 10 by a coding circuit in such a manner that, in each measuring cycle, the ratio of the number of pulses counted by the counter 85 before issuing a blocking signal to the number of measuring pulses

emitted by the diode 57 before one of the voltage comparators 69 to 72 or 89 to 92 reaches its threshold value does not exceed a predetermined value.

Although in the examples hereinbefore described, the output stage which includes the AND-gates 101 and 106 and the transistors 103 and 109 controls the two light-emitting diodes 105 and 110, this output stage could alternatively or in addition be used to control a servo-motor which adjusts the focus of the lens.

CLAIMS

1. A focussing system for adjusting a photographic or cinematographic camera lens in accordance with the distance between a subject to be photographed and the camera and/or for indicating when the lens is focussed, the system including a pulse generator circuit, a radiation emitting element driven by the pulse generator circuit for producing a measuring beam, radiation receiving means for receiving, in use, radiation produced by the radiation emitting elements and reflected back from the subject to be focussed, a signal processing circuit responsive to the radiation receiving means, an integrator circuit responsive to the output of the signal processing circuit, and a threshold circuit responsive to the output of the integrator circuit and including at least one memory element, the threshold circuit being set to a predetermined threshold value, the integrator circuit being reset at the end of each measuring cycle, and each measuring cycle including a number of pulses produced by the pulse generator circuit.

2. A system as claimed in Claim 1 in which the radiation receiving means comprises a pair of radiation receiving elements.

3. A system as claimed in Claim 2 in which the integrator circuit comprises two individual integrator sections, each section being associated with a respective one of the receiving elements, and under the control of pulses produced by the pulse generator circuits, each integrator section being rendered responsive to the output of the signal processing circuit when a pulse is expected from its associated receiving element.

4. A system as claimed in Claim 3 in which each individual integrator section comprises an operational amplifier having a feedback integration capacitor and in which the threshold circuit comprises a pair of voltage comparators, each of which is associated with a respective integrator section.

5. A system as claimed in Claim 4 in which said at least one memory element comprises at least one flip-flop responsive to the output signal of each voltage comparator and transfers said output signal to an output stage upon receiving a control signal at the end of each measuring cycle.

6. A system as claimed in any one of the preceding claims in which the pulse generator circuit includes a logic circuit clocked at a predetermined frequency.

7. A system as claimed in any one of the



(17)

If the threshold voltage of voltage comparator 89 to 92 is reached before counter 85 completes its counting cycle, the D-flip-flop 96 receives a clock pulse thereby setting the flip-flop. When the counter 85 reaches the end of its counting cycle, a logic "one" signal appears at its Qm-output and inverter 100 applies a blocking signal to AND-gate 74 and 95. This prevents the counter 85 from receiving further clock pulses and it also prevents further clock pulses being applied to flip-flops 75 and 96.

At the end of each measuring cycle, counter 83 applies a control signal to the clock input of flip-flops 84 and 97, thereby setting these flip-flops. A logic "nought" signal is applied to the input of both AND-gates 101 and 106 with the result that both transistors 103 and 109 are turned off. Consequently, diodes 105 and 110 are not energised and this indicates to the camera user that the lens is in focus.

Switch 107 is closed when the lens is at its infinity setting. When switch 107 is open, the associated input of AND-gate 106 is connected by a resistor 102 to the positive supply line.

In general, if one of the flip-flops 75 or 96 is first set and then the other flip-flop is set before the counter 85 has completed its counting cycle, this indicates that the lens is in focus. If the other flip-flop is not set before the counter 85 completes its counting cycle the AND-gates 74 and 95 will be blocked and prevent clock pulses being applied to the flip-flop 75 and 96. Consequently, the end of the counting cycle of the counter 83, one of the AND-gates 101 and 106 receives a logic "one" signal and consequently one of the diodes 105 to 110 is energised.

On reaching the end of the measuring cycle as determined by counter 83, transistors 73 and 93 are turned on and so the integration capacitors 67 and 87 are discharged. Also, a reset pulse is applied, after a short delay, to the flip-flop 75 and 96. Counter 85 is also reset by a reset pulse from counter 83.

Since at least in the close up range of the camera the intensity of a signal falling on the diodes 9 and 10 is maintained at a substantially constant value, one of the voltage comparators 69 to 72 or 89 to 92 will reach its threshold value within a period which has a substantially constant value. After one of the voltage comparators has reached its threshold value, the other voltage comparator had a tolerance period, as determined by the counter 85, in which it may or may not reach its threshold value.

In an alternative embodiment of the present invention, not shown, the radiation intensity of the diode 57 is not controlled. In this embodiment, the number of pulses counted by the counter 85 before it issues its blocking signal to AND-gates 74 and 95 is varied in accordance with the amplitude of the output signals of the diodes 9 and 10 by a coding circuit in such a manner that, in each measuring cycle, the ratio of the number of pulses counted by the counter 85 before issuing a blocking signal to the number of measuring pulses

emitted by the diode 57 before one of the voltage comparators 69 to 72 or 89 to 92 reaches its threshold value does not exceed a predetermined value.

Although in the examples hereinbefore described, the output stage which includes the AND-gates 101 and 106 and the transistors 103 and 109 controls the two light-emitting diodes 105 and 110, this output stage could alternatively or in addition be used to control a servo-motor which adjusts the focus of the lens.

CLAIMS

1. A focussing system for adjusting a photographic or cinematographic camera lens in accordance with the distance between a subject to be photographed and the camera and/or for indicating when the lens is focussed, the system including a pulse generator circuit, a radiation emitting element driven by the pulse generator circuit for producing a measuring beam, radiation receiving means for receiving, in use, radiation produced by the radiation emitting elements and reflected back from the subject to be focussed, a signal processing circuit responsive to the radiation receiving means, an integrator circuit responsive to the output of the signal processing circuit, and a threshold circuit responsive to the output of the integrator circuit and including at least one memory element, the threshold circuit being set to a predetermined threshold value, the integrator circuit being reset at the end of each measuring cycle, and each measuring cycle including a number of pulses produced by the pulse generator circuit.

2. A system as claimed in Claim 1 in which the radiation receiving means comprises a pair of radiation receiving elements.

3. A system as claimed in Claim 2 in which the integrator circuit comprises two individual integrator sections, each section being associated with a respective one of the receiving elements, and under the control of pulses produced by the pulse generator circuits, each integrator section being rendered responsive to the output of the signal processing circuit when a pulse is expected from its associated receiving element.

4. A system as claimed in Claim 3 in which each individual integrator section comprises an operational amplifier having a feedback integration capacitor and in which the threshold circuit comprises a pair of voltage comparators, each of which is associated with a respective integrator section.

5. A system as claimed in Claim 4 in which said at least one memory element comprises at least one flip-flop responsive to the output signal of each voltage comparator and transfers said output signal to an output stage upon receiving a control signal at the end of each measuring cycle.

6. A system as claimed in any one of the preceding claims in which the pulse generator circuit includes a logic circuit clocked at a predetermined frequency.

7. A system as claimed in any one of the



preceding claims in which the duration of each measuring cycle is determined by a first counter receiving clock pulses derived from the pulse generator circuit the counter producing a control signal each time it receives a predetermined number of clock pulses.

8. A system as claimed in Claim 7 in which the pulse generator circuit is connected to the input of a delay circuit, the output of which provides the clock pulses for the first counter, and in which the integrator circuit is rendered responsive to the output of the signal processing circuit under the control of the output signal of the delay circuit.

9. A system as claimed in Claim 5 or any one of Claims 6 to 8 when dependent on Claim 5 including a second counter receiving clock pulses derived from the pulse generator circuit and responsive to said flip-flops, each flip-flop being connected to its associated voltage comparator by a gate, during each measuring cycle the second counter being enabled upon receiving a signal from one of the flip-flops corresponding to the input of its associated voltage comparator exceeding the threshold value, and thereafter upon counting a predetermined or variable number of pulses issuing a blocking signal to said gates.

10. A system as claimed in Claim 9 in which the second counter issues a blocking signal after counting a predetermined number of pulses and in which a regulating circuit is provided for controlling the radiation emitting element, the regulating circuit reducing the radiation intensity of the radiation emitting element in at least the close-up range of the camera in accordance with the intensity of the radiation incident on the receiving elements so that this intensity does not exceed a predetermined value.

11. A system as claimed in Claim 10 in which the variation in the intensity of the radiation incident of the receiving elements is less than or equal to a predetermined tolerance value.

12. A system as claimed in Claim 9 in which when the radiation intensity of the radiation emitting element is uncontrolled, the number of pulses counted by the second counter before issuing a blocking signal is varied in accordance with the amplitude of the signals of the receiving elements by a coding circuit in such a manner that, during each measuring cycle, the ratio of the

number of pulses counted by the second counter before issuing a blocking signal to the number of pulses produced by the pulse generator circuit before the output of one of the integrator sections exceeds a threshold value does not exceed a predetermined tolerance value.

13. A focussing system as claimed in Claim 2 or any one of Claims 3 to 12 when dependent on Claim 2 in which the integrator circuit comprises a pair of individual integrator sections, each section being associated with a respective one of the receiving elements, and in which said at least one memory element comprises a pair of D-flip-flops associated with each integrator section in each pair the first flip-flop having its clock input responsive to the output of the associated integrator section and its Q-output connected to the D-input of the second flip-flop, the clock input of the second flip-flop receiving a control signal at the end of each measuring cycle.

14. A focussing system as claimed in Claim 13 when dependent on Claim 9 in which the Q-outputs of the first flip-flops of each pair are connected by an OR-gate to the first input of a further gate the second input of which is responsive to the pulse generator circuit and the third input of which is connected by an inverter to the output of the second counter, the output of the further gate being connected to the clock input of the second counter.

15. A system as claimed in Claim 9 in which the signal processing circuit includes sections common to both radiation receiving elements, the common section being connected between first and second multiplex stages controlled by the pulse generator circuit and in which the clock input of the second counter is connected to the pulse generator circuit via a frequency halving element.

16. A system as claimed in Claim 4 or any one of Claims 5 to 15 when dependent on Claim 4 in which in each integrator section the feed back capacitor is discharged at the end of each measuring cycle by a semi-conductor switch element.

17. In a photographic or cinematographic camera a focussing system substantially as hereinbefore described with reference to and as shown in Figures 1 and 2 of the accompanying drawings.