

NROM FLASH MEMORY DEVICES ON ULTRATHIN SILICON**Abstract**

An NROM flash memory cell is implemented in an ultra-thin silicon-on-insulator structure. In a planar device, the channel (200) between the source/drain (220, 221) areas is normally fully depleted. An oxide layer (210, 211) provides an insulation layer between the source/drain areas and the gate insulator layer (207) on top. A control gate (230) is formed on top of the gate insulator layer. In a vertical device, an oxide pillar (310) extends from the substrate with a source/drain area (330, 331) on either side of the pillar side. Epitaxial regrowth is used to form ultra-thin silicon body regions (300, 301) along the sidewalk of the oxide pillar. Second source/drain areas (320, 321) are formed on top of this structure. The gate insulator (307) and control gate (330) are formed on top.

Figure 2