WHAT IS CLAIMED IS:

1. A silicon-on-insulator chip comprising:

an insulator layer;

a first silicon island with a surface of a first crystal orientation, the first silicon island overlying the insulator layer; and

a second silicon island with a surface of a second crystal orientation, the second silicon island overlying the insulator layer.

2. The silicon-on-insulator chip of claim 1 and further comprising a first transistor of a first conduction type formed on the first silicon island, and a second transistor of a second conduction type formed on the second silicon island.

3. The silicon-on-insulator chip of claim 2 wherein the first crystal orientation is (110) and the first transistor is a p-channel transistor, and wherein the second crystal orientation is (100) and the second transistor is a n-channel transistor.

4. The silicon-on-insulator chip of claim 2 wherein the first crystal orientation is (023) and the first transistor is a p-channel transistor, second crystal orientation is (100) and the second transistor is a n-channel transistor.

5. The silicon-on-insulator chip of claim 1 wherein the first silicon island comprises a plurality of silicon layers, each with a different crystal orientation.

6. The silicon-on-insulator chip of claim 5 wherein the plurality of silicon layers comprises a (110) silicon layer overlying a (100) silicon layer.

7. The silicon-on-insulator chip of claim 6 wherein the (110) silicon layer has a thickness of about 10 to about 500 angstroms.

8. The silicon-on-insulator chip of claim 1 wherein the first and second silicon islands each have a thickness in the range of about 10 angstroms to about 1000 angstroms.

9. The silicon-on-insulator chip of claim 1 wherein the first and second silicon islands have different thicknesses.

10. The silicon-on-insulator chip of claim 1 wherein the first and second silicon islands each have rounded or faceted corners.

11. The silicon-on-insulator chip of claim 1 wherein the insulator layer comprises a dielectric.

12. The silicon-on-insulator chip of claim 11 wherein the insulator layer comprises a crystalline dielectric.

13. The silicon-on-insulator chip of claim 1 wherein the insulator layer has a crystalline layer at the interface with the silicon islands.

14. The silicon-on-insulator chip of claim 1 wherein the insulator layer comprises silicon oxide.

15. The silicon-on-insulator chip of claim 1 wherein the insulator layer comprises aluminum oxide.

16. A silicon-on-insulator chip comprising:

an insulator layer;

a first silicon island with a surface of the (110) crystal orientation, the first silicon island overlying the insulator layer; and

a second silicon island with a surface of the (100) crystal orientation, the second silicon island overlying the insulator layer.

17. The silicon-on-insulator chip of claim 16 and further comprising a p-channel transistor formed on the first silicon island, and a n-channel transistor formed on the second silicon island.

18. The silicon-on-insulator chip of claim 16 wherein the first and second silicon islands each have a thickness in the range of about 10 angstroms to about 1000 angstroms.

19. The silicon-on-insulator chip of claim 16 wherein the first and second silicon islands have different thicknesses.

20. The silicon-on-insulator chip of claim 16 wherein the first and second silicon islands each have rounded or faceted corners.

21. The silicon-on-insulator chip of claim 16 wherein the insulator layer comprises a crystalline dielectric.

22. The silicon-on-insulator chip of claim 16 wherein the insulator layer has a crystalline layer at the interface with the first and second silicon islands.

23. The silicon-on-insulator chip of claim 16 wherein the insulator layer comprises silicon oxide.

24. The silicon-on-insulator chip of claim 16 wherein the insulator layer comprises aluminum oxide.

25. A method of forming silicon-on-insulator chip, the method comprising:

providing a silicon-on-insulator substrate including a silicon layer of a first crystal orientation overlying an insulator layer with a crystalline surface, the silicon layer including a first and a second region;

forming an amorphous silicon region over the second region of the silicon layer; and

recrystallizing the amorphous silicon region to form a region with a second crystal orientation.

26. The method of claim 25 and further comprising, after the recrystallizing the amorphous silicon region:

forming a first silicon island of the first crystal orientation and a second silicon island of the second orientation; and

forming a transistor of the first conduction type on the first silicon island and a transistor of the second conduction type on the second silicon island.

27. The method of claim 25 wherein the first crystal orientation is (110) and the second crystal orientation is (100) and wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

28. The method of claim 25 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

29. The method of claim 25 wherein the insulator layer comprises aluminum oxide.

30. The method of claim 29 wherein the aluminum oxide has a crystal orientation of (0, 1, -1, 2).

31. The method of claim 25 wherein the silicon layer has a thickness in the range of about 10 angstroms to about 500 angstroms.

32. A method of forming semiconductor device, the method comprising:

providing a workpiece including a first silicon layer of a first crystal orientation overlying a second silicon layer of a second crystal orientation, the second silicon layer overlying a semiconductor layer; and

removing a portion of the first silicon layer to expose the second silicon layer in a predetermined region.

33. The method of claim 32 wherein the semiconductor device comprises a silicon-on-insulator device, and wherein the insulator layer overlies a semiconductor substrate.

34. The method of claim 33, further comprising:

forming a first silicon island with a surface of the first crystal orientation and a second silicon island with a surface of the second orientation; and

forming a transistor of the first conduction type on the first silicon island and a transistor of the second conduction type on the second silicon island.

35. The method of claim 34 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

36. The method of claim 35 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

37. The method of claim 33 wherein the first silicon layer has a thickness in the range of about 10 angstroms to about 100 angstroms.

38. The method of claim 33 wherein the second silicon layer has a thickness in the range of about 10 angstroms to about 1000 angstroms.

39. The method of claim 33 wherein the insulator layer comprises a dielectric.

40. The method of claim 33 wherein the insulator layer comprises silicon oxide.

41. The method of claim 33, wherein the first silicon layer is formed by epitaxial growth of silicon on the second silicon layer, the method further comprising:

forming a first silicon island with a surface of the first crystal orientation and second silicon island with a surface of the second orientation; and

forming a transistor of the first conduction type on the first silicon island and a transistor of the second conduction type on the second silicon island.

42. The method of claim 41 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

43. The method of claim 42 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

44. The method of claim 32 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

45. A method of forming silicon-on-insulator chip, the method comprising:

providing a silicon-on-insulator substrate including a first silicon layer of a first crystal orientation overlying a second silicon layer of a second crystal orientation, said second silicon layer overlying an insulator layer;

amorphosizing a portion of the first silicon layer in a predetermined region to form an amorphous silicon region; and

recrystallizing the amorphous silicon region to form a region with a second crystal orientation.

46. The method of claim 45, further comprising:

forming a first silicon island with a surface of the first crystal orientation and a second silicon island with a surface of the second orientation; and

forming a transistor of a first conduction type on the first silicon island and a transistor of a second conduction type on the second silicon island.

47. The method of claim 46 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

48. The method of claim 47 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

49. The method of claim 45 wherein the first silicon layer has a thickness in the range of about 10 angstroms to about 100 angstroms.

50. The method of claim 45 wherein the second silicon layer has a thickness in the range of about 10 angstroms to about 1000 angstroms.

51. The method of claim 45 wherein the insulator layer comprises a dielectric.

52. The method of claim 45 wherein the insulator layer comprises silicon oxide.

53. A method of forming silicon-on-insulator chip, comprising:

providing a silicon-on-insulator substrate including a silicon layer of a first crystal orientation overlying an insulator layer with a crystalline surface, the silicon layer including a first region and a second region;

removing a portion of the silicon layer in the second region to expose the insulator layer; and

performing epitaxial growth of silicon of a second crystal orientation on the insulator layer.

54. The method of claim 53 further comprising, after performing the epitaxial growth of silicon:

forming a first silicon island of the first crystal orientation and a second silicon island of the second orientation; and

forming a transistor of the first conduction type on the first silicon island and a transistor of the second conduction type on the second silicon island.

55. The method of claim 54 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

56. The method of claim 55 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

57. The method of claim 53 wherein the insulator layer comprises of aluminum oxide.

58. The method of claim 57 wherein the aluminum oxide has a crystal orientation of (0, 1, -1, 2).

59. The method of claim 53 wherein the silicon layer has a ~~thickness in the~~ range of about 10 angstroms to ~~about 500~~ angstroms.

WHAT IS CLIAMED IS:

1. A method of forming a silicon-on-insulator chip, the method comprising:

providing a silicon-on-insulator substrate including a silicon layer of a first crystal orientation overlying an insulator layer, the silicon layer including a first and a second region;

forming an amorphous silicon region in the second region of the silicon layer; and

recrystallizing the amorphous silicon region to form a region with a second crystal orientation.

2. The method of claim 1 and further comprising, after the recrystallizing the amorphous silicon region:

forming a first silicon island of the first crystal orientation and a second silicon island of the second orientation; and

forming a transistor of a first conduction type on the first silicon island and a transistor of a second conduction type on the second silicon island.

3. The method of claim 1 wherein the first crystal orientation is (110) and the second crystal orientation is (100) and wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

4. The method of claim 1 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

5. The method of claim 1 wherein the insulator layer comprises aluminum oxide.

6. The method of claim 5 wherein the aluminum oxide has a crystal orientation of (0, 1, 1, 2).

7. The method of claim 1 wherein the silicon layer has a thickness in the range of about 10 angstroms to about 500 angstroms.

8. The method of claim 1 wherein the forming the amorphous silicon region comprises implanting ions into the second region of the silicon layer.

9. The method of claim 8 wherein implanting ions comprises implanting silicon ions.

10. The method of claim 8 wherein the silicon layer has a thickness and wherein implanting ions comprises implanting ions to a depth of about half of the thickness of the silicon layer.

11. The method of claim 1 wherein providing a silicon-on-insulator substrate comprises providing a silicon-on-insulator substrate with a silicon layer overlying an insulator layer that includes a crystalline surface.

12. The method of claim 11 wherein recrystallizing the amorphous silicon region comprises recrystallizing using the crystalline surface of the insulator layer as a seed.

13. The method of claim 1 wherein providing a silicon-on-insulator substrate comprises providing a silicon-on-insulator substrate with a first silicon layer overlying a second silicon layer, the second silicon layer overlying the insulator layer and wherein forming an amorphous silicon region comprises amorphosizing a portion of the first silicon layer.

14. The method of claim 13 wherein recrystallizing the amorphous silicon region comprises recrystallizing using the second silicon layer as a seed.

15. A method of forming a silicon-on-insulator chip, the method comprising:

providing a silicon-on-insulator substrate including a first silicon layer of a first crystal orientation overlying a second silicon layer of a second crystal orientation, said second silicon layer overlying an insulator layer;

amorphosizing a portion of the first silicon layer in a predetermined region to form an amorphous silicon region; and

recrystallizing the amorphous silicon region to form a region with the second crystal orientation.

16. The method of claim 15, further comprising:

forming a first silicon island with a surface of the first crystal orientation and a second silicon island with a surface of the second crystal orientation; and

forming a transistor of a first conduction type on the first silicon island and a transistor of a second conduction type on the second silicon island.

17. The method of claim 16 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

18. The method of claim 17 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

19. The method of claim 15 wherein the first silicon layer has a thickness in the range of about 10 angstroms to about 100 angstroms.

20. The method of claim 15 wherein the second silicon layer has a thickness in the range of about 10 angstroms to about 1000 angstroms.

21. The method of claim 15 wherein the insulator layer comprises a dielectric.

22. The method of claim 15 wherein the insulator layer comprises silicon oxide.

23. A method of fabricating a silicon-on-insulator chip, the method comprising:

providing a substrate with an insulator layer disposed thereon;

forming a first silicon layer over the insulator layer, the first silicon layer having a thickness of less than 50 angstroms, the first silicon layer having a first crystal orientation;

forming a second silicon layer over the first silicon layer, the second silicon layer having a thickness of less than 50 angstroms, the second silicon layer having a second crystal orientation that is different than the first crystal orientation;

forming a first silicon island with a surface of the first crystal orientation, the first silicon island overlying the insulator layer and being formed from the first silicon layer; and

forming a second silicon island with a surface of the second crystal orientation, the second silicon island overlying the insulator layer and being formed from the second silicon layer.

24. The method of claim 23 wherein the first crystal orientation is (023), and wherein the second crystal orientation is (100).

25. The method of claim 24 and further comprising forming a p-channel transistor in the first silicon island and forming an n-channel transistor in the second silicon island.

26. The method of claim 23 wherein the forming of the second silicon layer comprises forming a (110) silicon layer overlying a (100) silicon layer.

27. The method of claim 23 wherein the first and second silicon islands each have rounded or faceted corners.

28. The method of claim 23 wherein the insulator layer comprises a crystalline dielectric.

29. The method of claim 23 wherein the insulator layer has a crystalline layer at the interface with the first and second silicon islands.

30. The method of claim 23 wherein the insulator layer comprises silicon oxide.

31. The method of claim 23 wherein the insulator layer comprises aluminum oxide.

32. A method of fabricating a silicon-on-insulator chip, the method comprising:

providing a substrate with an insulator layer disposed thereon;

forming a first silicon island with a surface of a first crystal orientation, the first silicon island overlying the insulator layer; and

forming a second silicon island with a surface of a second crystal orientation, the second silicon island overlying the insulator layer, wherein the first and second silicon islands have different thicknesses;

wherein forming the first silicon island comprises forming a plurality of silicon layers overlying one another using a wafer bonding technique that includes a hydrogen implant step, and wherein forming a plurality of silicon layers comprises forming a (110) silicon layer overlying (100) silicon layer.

33. The method of claim 32 and further comprising:

forming a first transistor of a first conduction type on the first silicon island; and

forming a second transistor of a second conduction type on the second silicon island.

34. The method of claim 33 wherein the first crystal orientation is (110) and the first transistor is a p-channel transistor, and wherein the second crystal orientation is (100) and the second transistor is a n-channel transistor.

35. The method of claim 32 wherein the (110) silicon layer has a thickness of about 10 to about 500 angstroms.

36. A method of forming semiconductor chip, the method comprising:

providing a silicon substrate having a first crystal orientation;

forming a silicon layer of a second crystal orientation on the silicon substrate, the silicon layer including a first and a second region;

forming an amorphous silicon region in the second region of the silicon layer; and

recrystallizing the amorphous silicon region to form a region with the first crystal orientation.

37. The method of claim 36 and further comprising, after the recrystallizing the amorphous silicon region:

forming a first silicon island of the first crystal orientation and a second silicon island of the second crystal orientation; and

forming a transistor of a first conduction type on the first silicon island and a transistor of a second conduction type on the second silicon island.

38. The method of claim 37 wherein the first crystal orientation is (110) and the second crystal orientation is (100) and wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

39. The method of claim 36 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

40. The method of claim 36 wherein the silicon layer has a thickness in the range of about 10 angstroms to about 500 angstroms.

41. A method of forming a semiconductor device, the method comprising:

providing a substrate including a semiconductor layer overlying the substrate, the semiconductor layer having a first crystal orientation;

implanting ions into a portion of the semiconductor layer; and

recrystallizing the portion of the semiconductor layer so that the portion has a second crystal orientation that is different than the first crystal orientation.

42. The method of claim 41 wherein the semiconductor layer comprises a silicon layer and wherein implanting ions comprises implanting silicon ions.

43. The method of claim 41 wherein the semiconductor layer comprises a silicon layer and wherein implanting ions comprises implanting germanium ions.

44. The method of claim 41 wherein the semiconductor layer comprises a silicon layer and wherein implanting ions comprises implanting argon ions.

45. The method of claim 41 wherein recrystallizing comprises recrystallizing the semiconductor layer using an underlying semiconductor layer as a seed layer.

46. The method of claim 41 wherein recrystallizing comprises recrystallizing the semiconductor layer using an underlying insulating layer as a seed layer.

47. The method of claim 41 and further comprising, after the recrystallizing:

forming a first silicon island of the first crystal orientation and a second silicon island of the second orientation; and

forming a transistor of a first conduction type on the first silicon island and a transistor of a second conduction type on the second silicon island.

48. The method of claim 47 wherein the first crystal orientation is (110) and the second crystal orientation is (100) and wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

49. The method of claim 41 wherein the first crystal orientation is (110) and the second crystal orientation is (100).