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ABSTRACT OF THE DISCLOSURE

MULTICHIP WAFER LEVEL SYSTEM PACKAGES AND METHODS OF FORMING SAME

The present invention defines a packaging implementation providing a multichip multilayer system on a chip solution. Greater integration of a plurality and variety of known good die contained within cavities formed in a separate substrate is achieved. Additional redistribution and interconnect layers above the multichip configuration may be formed with the redistribution layers terminating in electrical connections such as conductive bumps or balls. In one embodiment, the cavities of the substrate receive signal device connections, such as conductive bumps, of a plurality of semiconductor dice in a flip-chip configuration. A portion of the back surface of the substrate is then removed to a depth sufficient to expose the conductive bumps. In another embodiment, the cavities receive the semiconductor dice with the active surface of the semiconductor dice facing up wherein metal layer connections are formed and coupled to bond pads or other electrical connectors of the semiconductor dice.

FIG. 3F



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