THIS SHEET HAS BEEN REPLACED

TRENCH DEPLETION MOSFET

ABSTRACT OF THE DISCLOSURE

A vertical trench power MOS transistor with low on-resistance is obtained by eliminating the inversion region of a conventional structure. In one embodiment, a deep-depletion region is formed between the trench gates to provide forward blocking capability. In another embodiment, forward blocking is achieved by depletion from the trench gates and a junction depletion from a P diffusion between the gates. Both embodiments are preferably fabricated in a cellular geometry. The device may also be provided in a horizontal conduction configuration in which the MOS gate is disposed on the upper surface of the semiconductor wafer over the deep-depletion region.

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