device 114 can also be in a wire-bonded configuration, or a hybrid or combination of stacked devices.

The integrated circuit device 114 can include an interconnect side 116 for attachment to the top trace 112 of the base substrate 102. The interconnect side 116 of the integrated circuit device 114 can include contacts, fabricated thereon. The integrated circuit device 114 can also include an inactive side 118, which is a side opposite the interconnect side 116.

The integrated circuit packaging system 100 can include a chip interconnect 120. The chip interconnect 120 provides an electrical connection and can include a solder ball, a bond wire, or solder as examples. The chip interconnect 120 provides electrical connectivity between the integrated circuit device 114 and the base substrate 102. The chip interconnect 120 can be attached to the interconnect side 116 of the integrated circuit device 114.

The integrated circuit packaging system 100 can include a top encapsulation 122, which is defined as a cover for hermetically sealing a semiconductor device and for providing mechanical and environmental protection. The top encapsulation 122 can be formed covering or over the integrated circuit device 114, the chip interconnect 120, the top trace 112, and the conductive stud 110. The top encapsulation 122 can fill in the top recess 132, which provides a mold lock between the top encapsulation 122 and the base substrate 102.

The integrated circuit packaging system 100 can include a system interconnect 124 mounted to the conductive stud 110 at the bottom surface 108. The system interconnect 124 provides an electrical connection and can include a solder ball, a solder bump, or a solder joint as examples. The system interconnect 124 is in direct contact with the conductive stud 110 and is in direct contact with the base encapsulation 104 with a portion of the system interconnect 124 embedded within the base encapsulation 104. The system interconnect 124 provides electrical connectivity between the top trace 112 and an external components or systems (not shown).

It has been discovered that the configuration and composition of the base substrate 102 with the base encapsulation 104 simplifies construction and reduces material cost over substrates comprised of single semi-conductive materials. For example, the use of laminate, epoxy, or screen printing materials for the base encapsulation 104 can simplify construction and provide protection for the top trace 112 and the conductive stud 110. The base substrate 102 with the base encapsulation 104 and embedded traces and studs removes the need for time consuming semiconductor printing methods.

It has been found that the conductive stud 110 having the bottom recess 130 reduces overall package height, resulting in a thinner and slimmer package. It has been discovered that the conductive stud 110 having the top recess 132 provides a mold locking feature with

What is claimed is:

1. A method for manufacturing an integrated circuit packaging system comprising:

forming a base substrate including:

providing a sacrificial carrier,

mounting a metallic sheet on the sacrificial carrier,

applying a top trace to the metallic sheet,

forming a conductive stud on the top trace,

forming a base encapsulation over the metallic sheet, the top trace, and the conductive stud, the top trace exposed from a top surface of the base encapsulation, and

removing the sacrificial carrier and the metallic sheet;

mounting an integrated circuit device on the base substrate; and

encapsulating the integrated circuit device and the base substrate with a top encapsulation.

2. The method as claimed in claim 1 wherein forming the conductive stud includes forming a bottom recess in the conductive stud.

3. The method as claimed in claim 1 wherein forming the conductive stud includes forming the conductive stud coplanar with the top trace.

4. The method as claimed in claim 1 further comprising forming a redistribution layer between the integrated circuit device and the base substrate.

5. The method as claimed in claim 1 wherein mounting the integrated circuit device includes attaching a chip interconnect between the integrated circuit device and the base substrate.

6. The method as claimed in claim 1 further comprising mounting a stacked device on the integrated circuit device.

7. The method as claimed in claim 1 wherein forming the base encapsulation includes covering the top trace and the conductive stud with a lamination or screen printing material.

8. The method as claimed in claim 1 wherein forming the conductive stud includes forming a top recess in the conductive stud.

~~9. The method as claimed in claim 1 wherein forming the base encapsulation include forming a flange, the flange laterally extending beyond the top encapsulation.~~

~~10. The method as claimed in claim 1 wherein forming the base encapsulation include forming an overlap rim on the base encapsulation, the overlap rim laterally extending beyond the top encapsulation.~~

~~11. A method for manufacturing a semiconductor package comprising:~~

~~forming a base substrate includes:~~

~~providing a sacrificial carrier,~~

~~mounting a metallic sheet on the sacrificial carrier,~~

~~applying a top trace to the metallic sheet,~~

~~forming a conductive stud on the top trace,~~

~~forming a base encapsulation over the metallic sheet, the top trace, and the conductive stud, the top trace exposed from a top surface of the base encapsulation, and~~

~~removing the sacrificial carrier and the metallic sheet; and~~

~~mounting an integrated circuit device on the base substrate;~~

~~encapsulating the integrated circuit device and the base substrate with a top encapsulation;~~

~~processing a bottom surface of the base substrate for exposing the conductive stud; and~~

~~attaching a system interconnect to the conductive stud at the bottom surface.~~

~~12. The method as claimed in claim 11 wherein forming the conductive stud includes forming a bottom recess and a top recess in the conductive stud.~~

~~13. The method as claimed in claim 11 wherein mounting the integrated circuit device includes mounting the integrated circuit device directly on the top trace.~~

~~14. The method as claimed in claim 11 wherein forming the conductive stud includes forming a peripheral groove in the conductive stud, the peripheral groove surrounds a portion of the top trace in contact with the conductive stud.~~

~~15. The method as claimed in claim 11 wherein forming the base encapsulation includes:~~

~~forming a flange on the base encapsulation, the flange laterally extending beyond the top encapsulation; and~~

~~forming a mold overlap covering a lateral side of the top encapsulation.~~

~~16.~~1. An integrated circuit packaging system comprising:

a base substrate, the base substrate includes:

a base encapsulation,

a top trace embedded in the base encapsulation, the top trace coplanar with a top surface of the base encapsulation, and

a conductive stud on the top trace, the conductive stud embedded in the base encapsulation, the conductive stud coplanar with the top trace;

a system interconnect in direct contact with the conductive stud and in direct contact with the base encapsulation, a portion of the system interconnect embedded within the base encapsulation;

an integrated circuit device on the base substrate; and

a top encapsulation encapsulating the base substrate and the integrated circuit device.

~~17.~~2. The system as claimed in claim 1~~6~~ wherein the conductive stud includes a bottom recess and a peripheral groove.

~~18.~~3. The system as claimed in claim 1~~6~~ further comprising a redistribution layer between the base substrate and the integrated circuit device.

~~19.~~4. The system as claimed in claim 1~~6~~ further comprising a stacked device mounted on the integrated circuit device.

~~20.~~5. The system as claimed in claim 1~~6~~ further comprising a mold overlap between the base substrate and the top encapsulation.