

ABSTRACT

A repair method of a semiconductor memory device which includes a memory cell array including a main and a redundant cell array and error correction code (ECC) logic includes detecting a fail bit of each of a main repair unit of the main cell array and a redundant repair unit of the redundant cell array, determining whether the fail bit detected from each of the main and redundant repair units is correctable, by using the ECC logic and determining a first or a second correctable status, calculating a first cumulative correctable fail bit count of each of the main repair unit and the redundant repair unit, and determining whether to replace the main repair unit with the redundant repair unit depending on the first correctable status, the second correctable status, and the first and second cumulative correctable fail bit counts and performing a repair operation depending on the determination result.

15

FIG. 6