COLUMN REDUNDANCY CIRCUIT FOR DYNAMIC RANDOM ACCESS MEMORY

The present invention relates to semiconductor integrated circuit memories, and more particularly, to circuits for providing redundant columns in such memories when other portions of the memory are found defective.

In integrated circuit memories, a single defect in any portion of the array of memory cells may render the entire memory useless. Furthermore, as improvements in the design and fabrication of integrated circuits are made, greater numbers of memory cells are being placed on a single chip and as a result, very large scale integrated circuits are made. In such cases, the probability of producing one or more defective memory cells may be readily increased, to such an extent as to render the entire memory useless.

As a prior proposal to solve such problems, integrated circuit memories have been designed and fabricated in such a manner that spare memory cells in addition to normal memory cells are arranged on the same chip in order to substitute defect-free spare memory cells for defective normal memory cells. To achieve such substitution, integrated circuit memories need decoder circuits: normal decoders which may use address signals to selectively disable a row or a column associated with defective memory cells; and spare decoders which may address a row or a column associated with defect-free spare memory cells with said address signals.

After fabrication of such an integrated circuit memory, it would be tested to determine whether or not normal memory cells are defective. If rows or columns

including normal memory cells are determined as defective, then the integrated circuit memories would be programmed in such a manner that a spare decoder including defect-free spare memory cells may be enabled by address signals selecting the defective normal memory cells and also, a normal decoder selecting a row or a column corresponding to defective normal memory cells may be disabled by said address signals.

There are two ways of programming in that manner; one using nonvolatile memory elements, and the other by blowing polysilicon fuses. Again, the method of blowing fuses can be divided into the use of laser spots and the use of electrical current.

Currently, according to the development of semiconductor device manufacturing processes, there has been a redundancy scheme with which blocks including defective normal memory cells may be replaced with spare blocks including defect-free spare memory cells. For example, assuming that 64K normal memory cells are divided into 4 blocks of 16K memory cells, a fault of one cell of 16K memory cells constituting each block requires the replacement of the defective block with a defect-free 16K spare memory cell block.

In a dynamic random access memory, the row redundancy of substituting the faulty normal row line by the defect-free spare row line can be accomplished relatively easily. However, the column redundancy raises some problems. Particularly, when a spare decoder as disclosed in U.S. Patent No. 4,228,528 is used in a semiconductor dynamic random access memory device, such a device needs to include circuits for detecting the column address transition at a static column mode operation. As

a result, such on-chip addition of column address transition detection circuits incurs the drawback of increased chip size.

For example, Figures 1 and 2 are circuit diagrams illustrative of the normal decoder and spare decoder respectively of a prior art circuit performing column redundancy by way of laser fusing.

A column line (or bit line) of the normal memory cell array is connected to a line 8 of Figure 1. A column line of the spare memory cell array is connected to a line 18 of Figure 2.

To substitute the column line of the normal memory cell array, the operation of the column normal decoder will be disabled by the blowing of fuse 7, while fuses 15 and 16 of the column spare decoder of Figure 2 are programmed by fusing so that the spare decoder may be enabled with the input of column address signals input to the normal decoder. On the other hand, the use of the normal decoder means blowing of fuse 17 in the spare decoder.

Figure 3 is a waveform diagram illustrative of selecting a spare column in connection with the use of the spare decoder of Figure 2.

In DRAM devices, when $\overline{RAS}$ (Row Address Strobe) is brought to a logic low state (ground level), row address signals are input. In the low state of $\overline{RAS}$, when $\overline{CAS}$ is rendered low in the static column mode, column address signals are input to the column spare decoder. In this case, whenever the transition of column address signals arises, such detected transition clock is a reset clock

RST shown in Figure 3. The reset clock RST is coupled to a gate of an N-channel MOS transistor 12 of Figure 2.

To produce such a clock, the column address transition detection circuit is inevitably required to be arranged on the same chip. This causes an increase of chip size.

Another problem is that of power consumption since, whenever the reset clock RST is input to the gate of the transistor 12, the transistor 12 and at least one of transistors 10A (or 10B) through 11A (or 11B) conduct.

Preferred embodiments of the present invention aim to provide the following:

- a CMOS integrated circuit for simply performing column redundancy;
- a CMOS integrated circuit for simply performing column redundancy in a static column mode;
- a CMOS integrated circuit for performing column redundancy by block replacement;
- a CMOS redundancy circuit which has relatively reduced power consumption and chip size;

According to the present invention, there is provided a dynamic random access memory comprising:

a plurality of normal blocks, each normal block including normal memory cells arranged in rows and columns, normal sense amplifiers connected to pairs of columns respectively and normal transmission transistors, each transmission transistor having a source, a drain and a gate, each source (or drain) of said transistors being connected to a respective column;

a spare block including spare memory cells having the same number of cells as said normal memory cells in rows and columns, spare sense amplifiers connected to pairs of columns respectively and spare transmission transistors, each spare transmission transistor having a source, a drain and a gate, each source (or drain) of said transistors being connected to a respective column;

an input/output means for transmitting data information, said means being connected to each drain (or source) of said transmission transistors;

a plurality of normal column lines, each normal column line being connected to the gates of said normal transmission transistors of each normal block;

a spare column line connected to the gates of said spare transmission transistors of the spare block;

latch means for providing first and second logic signals in dependants upon whether said normal blocks are determined defect-free or defective, respectively;

a spare column decoding means connected to said latch means and said spare column line, for providing a spare block disabling signal with the input of said first logic signal when there are not defective normal blocks and a spare block enabling signal with said second logic signal and the input of true and complement column address signals when there are defective normal blocks; and

normal column decoding means connected to said normal column lines and said spare column decoding means, for addressing a specified normal block with the input of column address signals under the control of said spare

block disabling signal when there are no defective normal blocks and disabling said normal column decoding means so as to not select said normal blocks with the input of said spare block enabling signal when there are defective normal blocks.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to Figures 4 to 6 of the accompanying diagrammatic drawings, in which:

Figure 4 is a circuit diagram illustrative of an embodiment of the invention for performing block column redundancy in a semiconductor dynamic RAM;

Figure 5 is a detailed circuit diagram of a latch circuit, a spare column decoder and logic circuit and a normal column decoder, used as parts of the embodiment of Figure 4; and

Figure 6 is a timing diagram of a reset clock used in the embodiment of Figures 4 and 5.

In the semiconductor DRAM device of Figure 4, R1 and R2 represent row (or word) lines, MC a memory cell, reference numerals 71 through 78 sense amplifiers, reference numerals 81 through 84 input/output switching circuits, reference numerals 91 and 92 input/output sense amplifiers, reference numeral 100 a latch circuit, reference numeral 200 a spare column decoder and logic circuit, and reference numeral 47 a normal column decoder which is coupled to the output terminal of the spare column decoder 200 and inputs column address signals CA1 (or $\overline{CA1}$) through CAn-1 (or $\overline{CAn-1}$). Memory cells MC are

associated with each of sense amplifiers 71 through 78 in known folded bit line type. The sense amplifier 71 in a normal block BL1 is connected to the respective input/output bus lines I/O and $\overline{\text{I/O 1}}$ via a pair of transmission transistors 101 and 102. The other sense amplifier 72 in the block BL1, and the remaining sense amplifiers 73 to 78 in blocks $\overline{\text{BL1}}$, SBL and $\overline{\text{SBL}}$, are connected to the respective input/output bus lines I/O 0 and $\overline{\text{I/O 0}}$ through I/O 3 and $\overline{\text{I/O 3}}$ via transmission transistors 105 through 116 as shown in Figure 4. Input/output bus line pairs I/O 0 and $\overline{\text{I/O 0}}$ through I/O 3 and $\overline{\text{I/O 3}}$ are connected to the respective input/output switching circuits 81 through 84. Output lines of the input/output switching circuits 83 and 84 are coupled to input/output sense amplifiers 91 and 92 respectively.

The output terminal of the latch circuit 100 is coupled to the spare column decoder 200. The output terminal of the spare column decoder 200 is coupled to a spare column line 60 connected to the spare blocks SBL and $\overline{\text{SBL}}$ and also is coupled to the normal decoder 47 connected to normal blocks BL1 and $\overline{\text{BL1}}$ and normal decoders connected to other abbreviated normal blocks respectively. Each of normal blocks BL, $\overline{\text{BL1}}$ ..... etc. includes a pair of sense amplifiers and two pairs of transmission transistors, as does each of spare blocks SBL, $\overline{\text{SBL}}$.

Now let us assume that there are normal memory cells of 256K bits in the normal blocks of Figure 4, and an eight bit row address and a ten bit column address CA0 through CA9 are needed.

One of the column address CA0 and CA9 and one of its complements $\overline{\text{CA0}}$ and $\overline{\text{CA9}}$ are supplied to input/output

switching circuits 81 through 84 respectively and they are used as switching control signals for transferring data signals between input/output pairs I/O 0 and $\overline{\text{I/O 0}}$ through I/O 3 and $\overline{\text{I/O 3}}$ and input/output sense amplifiers 91 and 92 respectively. Therefore, there are 512 ($=2^8$ x 2) normal blocks with the array split into two halves, that is, the left half and the right half, of 256 blocks each. There are 512 ($=2^8$ x 2) memory cells in the respective normal block. There are similar respective spare blocks SBL and $\overline{\text{SBL}}$ on each lower portion of the left and right halves of Figure 4.

256 normal column decoders connected to the respective normal column lines 70 for simultaneously selecting normal blocks of two halves and one spare column decoder 200 connected to the spare column line 60 for selecting spare blocks SBL and $\overline{\text{SBL}}$ are arranged at the centre of the memory array. The latch circuit 100 functions to latch low or high due to the input of clock RST, as will be mentioned below, when $\overline{\text{RAS}}$ is at a low level state in a static column mode operation.

Now, if one or more memory cells of one of the normal blocks, that is, the normal block BL1, are failed, normal blocks BL1 and $\overline{\text{BL1}}$ will be replaced with spare blocks SBL and $\overline{\text{SBL}}$ including defect-free memory cells with a low state output of the normal column decoder 47 and a high state output of the spare column decoder 200.

Figure 5 represents a detailed circuit diagram of the normal column decoder 47, the spare column decoder 200 and the latch circuit 100.

Referring to Figure 5, the latch circuit 100 is composed of a pair of N-channel MOS driver transistors 31

and 32 of which each gate is connected to the drain 400 or 500 of the other, and both sources of which are connected to the ground source; an N-channel MOS transistor 30 whose drain-source current path is connected between the drain 400 and the ground source, a masterfuse MF connected between supply voltage source Vcc and the drain 400; a P-channel MOS transistor 33 whose source-drain current path is connected between the supply voltage source and the drian 500 and whose gate is connected to the drain 400; and an inverter 34 connected to the drain 500.

A gate terminal 48 of the N-channel MOS transistor 30 is coupled to the clock RST as will be mentioned hereinafter.

The spare column decoder and logic circuit 200 is composed of transmission gates T1 to T8 for transferring the column address CA1 through CA8 respectively; transmission gates $\overline{T1}$ to $\overline{T8}$ for transferring the column address $\overline{CA1}$ through $\overline{CA8}$ respectively; fuses F1 to F8 respectively connected to the output of transmission gates T1 through T8; fuses $\overline{F1}$ to $\overline{F8}$ respectively connected to output lines of transmission gates $\overline{T1}$ through $\overline{T8}$; a NAND gate 45 whose input terminals are connected to connection nodes of fuse pairs F1 and $\overline{F1}$ to F8 and $\overline{F8}$; N-channel MOS transistors 51 to 58 whose drains are respectively connected to input terminals of the NAND gate 45 and whose sources are connected to the ground source; and an inverter 46 whose input is connected to the output line of the NAND gate 45. Transmission gate pairs T1 and $\overline{T1}$ to T8 and $\overline{T8}$ are each composed of N-channel and P-channel MOS transistor pairs 35 and 36 as shown in Figure 5. Gates of N-channel MOS transistors 35 are connected to a line 49, and gates of

P-channel MOS transistors 36 are connected to a line 50. The lines 49 and 50 are connected to the input terminal and the output terminal of the inverter 34 respectively.

The output terminal of the inverter 46 is connected to the spare column line 60 and to the input terminal of the normal column decoder 47 formed of a known NOR gate. It should be noted that the output terminal of the inverter 46 may be respectively connected to input terminals of remaining normal column decoders. The normal column decoder 47 received the column address signals CA1 (or $\overline{CA1}$) to CA8 (or $\overline{CA8}$) and the output signal of the inverter 46, and the output terminal thereof is connected to the normal column line 70, being coupled to gates of transmission transistors 101 to 108.

Figure 6 represents a timing diagram of a reset clock RST applied to the input terminal 48 of Figure 5 in a static column mode operation.

Referring to Figure 6, the reset clock RST has a pulse of high state after $\overline{RAS}$ goes low but before column address signals COL ADD are received into the column decoders.

The operation of the circuit of Figures 4 and 5 will now be described in more detail.

In the case where the spare blocks $\overline{SBL}$ and SBL are not selected, all fuses are not blown. Even if the reset pulse RST of Figure 6 is applied to the terminal 48, the potential of node 400 is always kept at a high state. Therefore, the P-channel MOS transistor 33 remains at an OFF state and the N-channel MOS transistor 32 keeps an ON state, whereby the node 500 is latched to

a low state and the output line 50 of the inverter 34 maintains a high state. Then, transmission gates T1 to T8 and $\overline{T1}$ to $\overline{T8}$ become OFF.

However, N-channel MOS transistors 51 to 58 are all turned on, whereby the output of the NAND gate 45 is at a high state and the output of the inverter 46 is at a low state. Therfore, the spare column line 60 becomes low and transmission transistors 109 to 116 become OFF so that spare memory cells of spare blocks SBL and $\overline{SBL}$ are not selected.

The output of the inverter 46 is applied to the normal column decoder 47 formed by the NOR gate along with column address signals CA1 ($\overline{CA1}$) to CA8 (or $\overline{CA8}$). When the normal column line 70 is selected by the input signals of the normal column decoder 47, the line 70 becomes high and then transmission transistors 101 to 108 of Figure 4 are all turned on. Therefore, one normal memory cell of normal blocks BL1 and $\overline{BL1}$ may be selected by row selection signal on a row line R1 or R2.

Now, the case where the column redundancy is performed due to one or more defective normal memory cells will be described in detail.

Now, let us assume that one or more memory cells of normal block BL1 or/and $\overline{BL1}$ are defective and column address signals CA1 to CA2 are all low (the complement signals $\overline{CA1}$ to $\overline{CA2}$ are all high).

At this time, fuses F1 to F8 corresponding to the lines for transferring the column address signal of a low state and the master fuse MF are all blown by laser spots. Therefore, the node 400 is in a floating state

and the node 500 is in an indeterminate state. As the reset clock RST having a high state pulse, after $\overline{RAS}$ is low, is applied to the terminal 48, the node 400 becomes low due to the conduction of N-channel MOS transistor 30 and then the P-channel MOS transistor 33 is rendered conductive, while the N-channel MOS transistor 32 becomes OFF. Therefore, the node 500 is latched to a high state and the output line 50 of the inverter 34 to a low state. Due to the high state of the line 49 and the low state of the line 50, transmission gates T1 to T8 are all rendered conductive and N-channel transistors 57 to 58 become OFF.

Therefore, complement column address signals $\overline{CA1}$ to $\overline{CA8}$ which are all high states are applied to the NAND gate 45 via transmission gates $\overline{T1}$ to $\overline{T8}$ and unblown fuses $\overline{F1}$ to $\overline{F8}$. As a result, the output of the inverter 46 becomes high.

Therefore, transmission transistors 109 to 116 connected to the spare column line 60 become conductive, whereby spare blocks SBL and $\overline{SBL}$ are selected. On the other hand, due to the high state of the output of the inverter 46, outputs of all normal decoders become low and all transmission transistors in the respective normal blocks become nonconductive. Therefore, in a read operation, if column address signals CA0 and CA9 are all low states and a row (or word) line $\overline{R1}$ is selected, a data signal stored in a memory cell 600 of the spare block $\overline{SBL}$ is delivered to the input/output sense amplifier 92 via the sense amplifier 77, the transmission transistor 114, the input/output bus line $\overline{I/O\ 3}$ and the input/output switching circuit 84.

As mentioned above, although the above embodiment has been described for a column redundancy scheme of 256K

dynamic RAM, it will be appreciated by those skilled in the art that it may readily be applied to a 1 Megabyte dynamic RAM by the use of four 256K dynamic RAMs of Figure 4.

Therefore, the illustrated embodiment may achieve a reduced chip size because the above-mentioned address transition detection circuits are not needed, and accomplish low power consumption due to the use of the latch circuit and transmission gates.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification and/or drawings, or to any novel one, or any novel combination, of the steps of any method or process disclosed herein.

CLAIMS:

1. A dynamic random access memory comprising:

a plurality of normal blocks, each normal block including a number of normal memory cells arranged in rows and columns, normal sense amplifiers connected to pairs of columns respectively and normal transmission transistors, each transmission transistor having a source, a drain and a gate, each source (or drain) of said transistors arranged to be connected to a respective column;

a spare block including spare memory cells arranged in rows and columns, the spare memory cells of the spare block being substantially the same in number as the said number of normal memory cells included in a said normal block, spare sense amplifiers connected to pairs of columns respectively and spare transmission transistors, each spare transmission transistor having a source, a drain and a gate, each source (or drain) of said transistors arranged to be connected to a respective column;

an input/output means for transmitting data information, said means being connected to each drain (or source) of said transmission transistors;

a plurality of normal column lines, each normal column line being connected to the gates of said normal transmission transistors of one or more corresponding said normal blocks;

a spare column line connected to the gates of said spare transmission transistors of the spare block;

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latch means for providing first and second logic signals depending upon whether said normal blocks are determined defect-free or defective, respectively;

a spare column decoding means connected to said latch means and said spare column line, for providing a spare block disabling signal in response to an input of a said first logic signal when there are not defective normal blocks and for providing a spare block enabling signal in response to said second logic signal and the input of true and complement column address signals when there are defective normal blocks; and

normal column decoding means connected to said normal column lines and spare column decoding means, for addressing a specified normal block in response to an input of column address signals under the control of said spare block disabling signal when there are no defective normal blocks and for disabling said normal column decoding means so as to not select said normal blocks in response to said spare block enabling signal when there are defective normal blocks.

2. A dynamic random access memory according to Claim 1, wherein said latch means includes a first input terminal receiving a supply voltage, a master fuse connected to said first input terminal, and a second input terminal for receiving a reset clock which is arranged to activate after an activation of a row address strobe signal but before an activation of column address signals, said latch means for providing said first logic signal in response to an input of said supply voltage if said master fuse is not blown when said normal blocks are determined to be defect-free, and said latch means arranged to provide said second logic signal in response to said reset clock if said

master fuse is blown when one of said normal blocks is determined to be defective.

3. A dynamic random access memory according to Claim 2, wherein said latch means comprises a clamping node connected to said master fuse, an output node, a ground source node, a first transistor whose channel path is connected between said clamping node and said ground source node and whose gate is connected to said second input terminal, a first inverter connected between said clamping node and said output node, and a second transistor whose channel path is connected between said clamping node and said ground source node and whose gate is connected to said output terminal.

4. A dynamic random access memory according to Claim 3, wherein said first and second transistors are N-channel MOS transistors and said first inverter is a CMOS inverter.

5. A dynamic random access memory according to Claim 3 or 4, wherein said spare column decoding means comprises:

a plurality of true and complement column address input terminals inputting true and complement column address signals of each column address signal;

a plurality of true and complement transmitting paths connected to said true and complement column address input terminals respectively;

a plurality of transmission means associated in series on said transmitting paths respectively, for transmitting true and/or complement column address signal in response to said output logic signal of latch means;

a plurality of fuses associated in series on said transmitting paths respectively, said fuses being not blown when there is no defective normal block but blown so as to transmit selected signals of either said true column address signals or said complement column address signals when there are defective normal blocks;

a plurality of connecting nodes commonly connected at the end terminals of true and complement transmitting paths of each column address signal;

a plurality of transistors whose channel paths are connected in parallel between said connecting nodes and said ground source node and whose gates are coupled to the complement of said output logic signal of latch means; and

a logic gate connected to said connecting nodes.

6. A dynamic random access memory according to Claim 5, wherein each said transmission means comprises a pair of P-channel MOS transistor and N-channel MOS transistor whose channel paths are connected in parallel, the gate of the P-channel MOS transistor being coupled to the complement of said output logic signal of the latch means and the gate of the N-channel MOS transistor being coupled to said output logic signal of latch means.

7. A dynamic random access memory according to any preceding claim, wherein normal and spare memory cells are arranged in a folded bit line configuration.

8. A dynamic random access memory according to any preceding claim, wherein the or each said fuse is made of polycrystalline silicon.

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9. A dynamic random access memory according to Claim 5 or 6, or to Claim 7 or 8 as appendant to Claim 5 or 6, wherein said logic gate is an AND gate and each of said transmitting paths is programmed so as to transmit the true column address signal.

10. A dynamic random access memory substantially as hereinbefore described with reference to any one or more of Figures 4, 5 or 6 of the accompanying drawings.

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