

Description

The invention concerns a voltage offset producing fail safe circuit for use with a line receiver or the like.

Data transmission line receivers for use applications in accordance with in EIA (Electronic Industries Association) standard RS422/423 are well known. Typically, a line receiver is operated from a single power supply to receive the transmission of digital data on a differential, balanced twisted-pair transmission line. The line receiver generally includes a differential amplifier having a pair of inputs coupled to inputs of the line receiver through an attenuation circuit.

A problem can arise, due to input signal failure, which may cause the output of the line receiver to oscillate. This is undesirable because the oscillations may be treated by the end user equipment which is connected with the line receiver as digital data to create erroneous information. The signal failure may happen, for example, by the input to the line receiver being either open or short circuited.

Hence, there arises a need for providing a fail safe circuit which can guarantee that the output of the line receiver will go to a predetermined output state if the input thereof is either open or short circuited to thereby inhibit oscillations at the output of the receiver.

In addition, it is desirable to provide a fail safe circuit which allows the use of a termination resistance for matching of the receiver to the transmission line while providing the aforementioned fail safe feature.

A fail safe circuit in accordance with the prior art portion of claim 1 is disclosed in US-A-3,617,771.

The present invention seeks to provide an improved circuit for producing a voltage offset between first and second outputs thereof.

The invention also seeks to provide a fail safe circuit for use with EIA RS422/423 type line receivers.

The above objects are achieved by providing the circuitry including a bias circuit connected between first and second power supply conductors having first and second output terminals at which first and second bias signals are respectively provided, first and second transistor circuitry each respectively including a first and a second transistor of opposite conductivity types, said first and second transistors each having first, second and control electrodes, said control electrodes of said first transistors and said second transistors being coupled respectively to said first and second output terminals, said first electrodes of said first and second transistors of said first transistor circuitry being coupled to the first terminal, said first electrodes of said first and second transistors of said second transistor circuitry being coupled to the second terminal, said second electrodes of each of said first transistors being coupled to said first power supply conductor and said second electrodes of each of

said second transistors being coupled to said second power supply conductor.

The single feature is a schematic illustrating the voltage offset producing circuit of the preferred embodiment.

Turning to the single figure there is shown fail safe circuit 10 of the present invention which is suited to be manufactured in monolithic integrated circuit form and which, in the preferred embodiment, may be utilized in the input stage of a line receiver for guaranteeing that the output of the line receiver goes to a known logic output state when there is no signal applied at the input thereof. Fail safe circuit 10 produces a voltage offset between output nodes 12 and 14 as will be later explained. A bias circuit including resistor 16, diode 18, diode 20 and resistor 22 connected in series in the order mentioned between first and second power supply conductors 24 and 26 produces first and second bias signals at output nodes 28 and 30. By matching of the circuit elements of the bias circuit, the center point between diodes 18 and 20 is at a voltage level

$$\frac{V_{cc} + V}{2} \quad (1)$$

Thus, the bias signals appearing at the outputs 28 and 30 are at a known voltage level.

A pair of transistor circuits 32 and 34 are coupled between the power supply conductors to the outputs 28 and 30 of the bias circuit which establishes the voltage levels appearing at nodes 12 and 14. Each of the transistor circuits include a pair of transistors 36, 38; 40, 42 respectively having the emitters thereof interconnected through respective series connected resistors 44, 46; 48, 50. The collectors of each pair of transistors are connected between the respective power supply conductors with output nodes 12 and 14 being connected between the series connected resistors of the particular transistor circuit. The base electrodes of transistors 36 and 40 are connected to output 28 of the bias circuit. Likewise, the base electrodes of transistors 38 and 42 are connected to output 30 of the bias circuit.

Resistors 44, 46, 48 and 50 are matched and are of equal resistance value. If the transistors of the respective transistor circuits were matched and had equal geometries, the voltage levels appearing at nodes 12 and 14 (assuming no input signal at inputs 52 and 54) would be substantially identical, i.e. equal to the value of

$$\frac{V_{cc} + V}{2}$$

However, the emitter area of transistor 42, in the preferred embodiment, is made less than the emitter area of transistor 38 wherein the emitter contact potential of the former is therefore greater than that of the latter. Hence, a predeter-

mined voltage offset of the polarity shown is produced between nodes 12 and 14.

A feature of the present invention is that circuit 10 can be utilized in the attenuation input stage of a line receiver to guarantee that the output of the line receiver goes to a predetermined logic output stage when there is no signal applied at the input of the receiver. As illustrated, a typical line receiver includes a differential amplifier 56 having differential inputs coupled through an attenuation circuit comprising resistors 58 and 60 to inputs 52 and 54 of the line receiver. The differential amplifier 56 has outputs 62 and 64 which drive further stages of the receiver (not shown). For example, the fail safe circuit 10 can be utilised in a monolithic integrated line receiver circuit of the type MC3486 which is manufactured by Motorola, Inc.

In operation, as long as there is digital data transmission signals supplied to inputs 52 and 54, the offset voltage produced between terminals 12 and 14 is overridden and the line receiver will function in a normal manner. However, when there is no signal appearing at inputs 52 and 54, the voltage offset produced by circuit 10, at terminals 12 and 14, is sufficient in magnitude to drive one of the outputs of differential amplifier 56 to a high output state which, in turn, causes the output of the line receiver to go to a predetermined output logic state to indicate a signal failure.

The circuit structure of fail safe circuit 10 is such that a termination resistor, for example, typically 200 ohms can be placed across input terminals 52 and 54. This allows the twisted pair transmission line to be terminated in its characteristic impedance for maximum transfer of energy.

Hence, what has been described above is a novel circuit that provides a predetermined amount of voltage offset between a pair of output terminals and which is suited to be utilized in a line receiver circuit to guarantee that the output of the line receiver will go to a predetermined output logic state whenever there is signal failure at the input thereof.

Claims

1. A fail safe circuit (10) including circuitry for providing a voltage offset between first and second terminals (12, 14) characterized by the circuitry including a bias circuit (16, 18, 20, 22) connected between first (24) and second (26) power supply conductors the said bias circuit having first (28) and second (30) output terminals at which first and second bias signals are respectively provided, first (32) and second (34) transistor circuit means each respectively including a first (36, 40) and a second (38, 42) transistor of opposite conductivity types, said first and second transistors each having first, second and control electrodes, said control electrodes of said first transistors (36, 40) and said second transistors (38, 42) being coupled respectively to said first (28) and second (30) output terminals, said first electrodes of said first (36) and second (38)

transistors of said first (32) transistor circuitry means (32) being coupled to the first terminal (12), said first electrodes of said first (40) and second (42) transistors of said second (34) transistor circuitry means being coupled to the second terminal (14), said second electrodes of each of said first transistors (36, 40) being coupled to said first power supply conductor and said second electrodes of each of said second (38, 42) transistors being coupled to said second power supply conductor.

2. The circuit of claim 1 wherein: said second transistors (38, 42) are bipolar transistors and said second transistor (38) of said first transistor circuit means (32) has an emitter area different from the emitter area of said second transistor (42) of said second transistor circuit means (34); and each of said first and second transistor circuit means include resistive circuit means (44, 46, 48, 50) coupled between said first electrodes of said first and second transistors thereof.

Patentansprüche

1. Ausfallsicherungsschaltung (10) mit einem Schaltkreis zur Erzeugung eines Spannungsversatzes zwischen ersten und zweiten Anschlüssen (12, 14), dadurch gekennzeichnet, daß der Schaltkreis enthält: eine Vorspannungsschaltung (16, 18, 20, 22), die zwischen erste (24) und zweite (26) Stromversorgungsleiter geschaltet ist und erste (28) und zweite (30) Ausgangsanschlüsse aufweist, an denen erste und zweite Vorspannungssignale jeweils geliefert werden, eine erste (32) und eine zweite (34) Transistor-schaltung, die jeweils einen ersten (36, 40) und einen zweiten (38, 42) Transistor entgegengesetzter Leitfähigkeitstypen aufweisen, wobei die ersten und zweiten Transistoren jeweils erste, zweite und Steuerelektroden aufweisen, wobei die Steuerelektroden der ersten Transistoren (36, 40) und der zweiten Transistoren (38, 42) jeweils mit den ersten (28) und zweiten (30) Ausgangsanschlüssen verbunden sind, die ersten Elektroden zu ersten (36) und des zweiten (38) Transistors der ersten Transistorschaltung (32) mit dem ersten Anschluß (12) verbunden sind, die ersten Elektroden der ersten (40) und zweiten (42) Transistoren der zweiten Transistorschaltung (34) mit dem zweiten Anschluß (14) verbunden sind, die zweiten Elektroden von jedem der ersten Transistoren (36, 40) mit dem ersten Stromversorgungsleiter und die zweiten Elektroden eines jeden der zweiten Transistoren (38, 42) mit dem zweiten Stromversorgungsleiter verbunden sind.

2. Schaltung nach Anspruch 1, bei der: die zweiten Transistoren (38, 42) bipolare Transistoren sind und der zweite Transistor (38) der ersten Transistorschaltung (32) eine Emittierfläche aufweist, die sich von der Emittierfläche des zweiten Transistors (42) der zweiten Transistorschaltung (34) unterscheidet; und daß jede der ersten und zweiten Transistorschaltungen eine Widerstandserschaltung zwischen-

mined voltage offset of the polarity shown is produced between nodes 12 and 14.

A feature of the present invention is that circuit 10 can be utilized in the attenuation input stage of a line receiver to guarantee that the output of the line receiver goes to a predetermined logic output stage when there is no signal applied at the input of the receiver. As illustrated, a typical line receiver includes a differential amplifier 56 having differential inputs coupled through an attenuation circuit comprising resistors 58 and 60 to inputs 52 and 54 of the line receiver. The differential amplifier 56 has outputs 62 and 64 which drive further stages of the receiver (not shown). For example, the fail safe circuit 10 can be utilised in a monolithic integrated line receiver circuit of the type MC3486 which is manufactured by Motorola, Inc.

In operation, as long as there is digital data transmission signals supplied to inputs 52 and 54, the offset voltage produced between terminals 12 and 14 is overridden and the line receiver will function in a normal manner. However, when there is no signal appearing at inputs 52 and 54, the voltage offset produced by circuit 10, at terminals 12 and 14, is sufficient in magnitude to drive one of the outputs of differential amplifier 56 to a high output state which, in turn, causes the output of the line receiver to go to a predetermined output logic state to indicate a signal failure.

The circuit structure of fail safe circuit 10 is such that a termination resistor, for example, typically 200 ohms can be placed across input terminals 52 and 54. This allows the twisted pair transmission line to be terminated in its characteristic impedance for maximum transfer of energy.

Hence, what has been described above is a novel circuit that provides a predetermined amount of voltage offset between a pair of output terminals and which is suited to be utilized in a line receiver circuit to guarantee that the output of the line receiver will go to a predetermined output logic state whenever there is signal failure at the input thereof.

Claims

1. A fail safe circuit (10) including circuitry for providing a voltage offset between first and second terminals (12, 14) characterized by the circuitry including a bias circuit (16, 18, 20, 22) connected between first (24) and second (26) power supply conductors the said bias circuit having first (28) and second (30) output terminals at which first and second bias signals are respectively provided, first (32) and second (34) transistor circuit means each respectively including a first (36, 40) and a second (38, 42) transistor of opposite conductivity types, said first and second transistors each having first, second and control electrodes, said control electrodes of said first transistors (36, 40) and said second transistors (38, 42) being coupled respectively to said first (28) and second (30) output terminals, said first electrodes of said first (36) and second (38)

transistors of said first (32) transistor circuitry means (32) being coupled to the first terminal (12), said first electrodes of said first (40) and second (42) transistors of said second (34) transistor circuitry means being coupled to the second terminal (14), said second electrodes of each of said first transistors (36, 40) being coupled to said first power supply conductor and said second electrodes of each of said second (38, 42) transistors being coupled to said second power supply conductor.

2. The circuit of claim 1 wherein: said second transistors (38, 42) are bipolar transistors and said second transistor (38) of said first transistor circuit means (32) has an emitter area different from the emitter area of said second transistor (42) of said second transistor circuit means (34); and each of said first and second transistor circuit means include resistive circuit means (44, 46, 48, 50) coupled between said first electrodes of said first and second transistors thereof.

Patentansprüche

1. Ausfallsicherungsschaltung (10) mit einem Schaltkreis zur Erzeugung eines Spannungsversatzes zwischen ersten und zweiten Anschlüssen (12, 14), dadurch gekennzeichnet, daß der Schaltkreis enthält: eine Vorspannungsschaltung (16, 18, 20, 22), die zwischen erste (24) und zweite (26) Stromversorgungsleiter geschaltet ist und erste (28) und zweite (30) Ausgangsanschlüsse aufweist, an denen erste und zweite Vorspannungssignale jeweils geliefert werden, eine erste (32) und eine zweite (34) Transistor-schaltung, die jeweils einen ersten (36, 40) und einen zweiten (38, 42) Transistor entgegengesetzter Leitfähigkeitstypen aufweisen, wobei die ersten und zweiten Transistoren jeweils erste, zweite und Steuerelektroden aufweisen, wobei die Steuerelektroden der ersten Transistoren (36, 40) und der zweiten Transistoren (38, 42) jeweils mit den ersten (28) und zweiten (30) Ausgangsanschlüssen verbunden sind, die ersten Elektroden zu ersten (36) und des zweiten (38) Transistors der ersten Transistorschaltung (32) mit dem ersten Anschluß (12) verbunden sind, die ersten Elektroden der ersten (40) und zweiten (42) Transistoren der zweiten Transistorschaltung (34) mit dem zweiten Anschluß (14) verbunden sind, die zweiten Elektroden von jedem der ersten Transistoren (36, 40) mit dem ersten Stromversorgungsleiter und die zweiten Elektroden eines jeden der zweiten Transistoren (38, 42) mit dem zweiten Stromversorgungsleiter verbunden sind.

2. Schaltung nach Anspruch 1, bei der: die zweiten Transistoren (38, 42) bipolare Transistoren sind und der zweite Transistor (38) der ersten Transistorschaltung (32) eine Emitterfläche aufweist, die sich von der Emitterfläche des zweiten Transistors (42) der zweiten Transistorschaltung (34) unterscheidet; und daß jede der ersten und zweiten Transistorschaltungen eine Widerstandsschaltungseinrich-



tung (44, 46, 48, 50) aufweist, die zwischen die ersten Elektroden der ersten und zweiten Transistoren derselben geschaltet ist.

Revendications

1. Circuit de sécurité (10) comportant un circuit permettant de fournir un décalage de tension entre une première et une deuxième borne (12, 14), caractérisé en ce que le circuit comporte un circuit de polarisation (16, 18, 20, 22) connecté entre un premier et un deuxième conducteur d'alimentation électrique (24, 26), ledit circuit de polarisation possédant une première et une deuxième borne de sortie (28, 30) au niveau desquelles un premier et un deuxième signal de polarisation sont respectivement produits, un premier et un deuxième circuit à transistors (32, 34) comportant respectivement chacun un premier transistor (36, 40) et un deuxième transistor (38, 42) de types de conductivité opposés, lesdits premiers et deuxièmes transistors possédant chacun une première électrode, une deuxième électrode et une électrode de commande, lesdites électrodes de commande desdits premiers transistors (36, 40) et desdits deuxièmes transistors (38, 42) étant

respectivement couplées auxdites première et deuxième bornes de sortie (28, 30), lesdites premières électrodes desdits premier et deuxième transistors (36, 38) dudit premier circuit à transistor (32) étant couplées à la première borne (12), lesdites premières électrodes desdits premier et deuxième transistors (40, 42) dudit deuxième circuit à transistors (34) étant couplées à la deuxième borne (14), ladite deuxième électrode de chacun desdits premiers transistors (36, 40) étant couplée audit premier conducteur d'alimentation électrique et ladite deuxième électrode de chacun desdits deuxièmes transistors (38, 42) étant couplé audit deuxième conducteur d'alimentation électrique.

2. Circuit selon la revendication 1, où:

lesdits deuxièmes transistors (38, 42) sont des transistors bipolaires et ledit deuxième transistor (38) dudit premier circuit à transistors (32) possède une aire d'émetteur différente de l'aire d'émetteur dudit deuxième transistor (42) dudit deuxième circuit à transistors (34); et

chacun desdits premier et deuxième circuits à transistors comporte un circuit résistif (44, 46; 48, 50) couplé entre lesdites premières électrode de ses premier et deuxième transistors.

